FAIRCHILD
A Schlumberger Company

Bipolar Division

93419
64 x 9-Bit Static Random Access Memory

TTL Bipolar Memory

Description

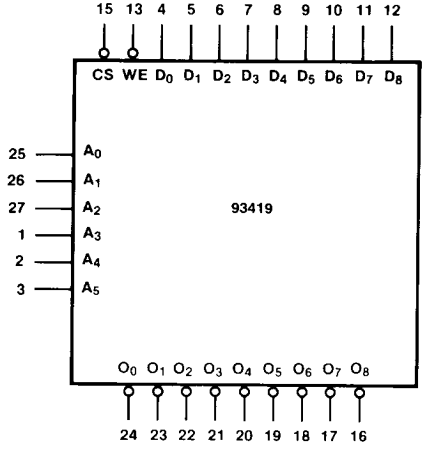
The 93419 is a 576-bit read/write Random Access Memory (RAM), organized 64 words by nine bits per word with open collector outputs. It is ideally suited for scratchpad, small buffer and other applications where the number of required words is small and where the number of required bits per word is relatively large. The ninth bit can provide parity for 8-bit word systems. The commercial version of the 93419 is available in two speeds "standard" speed and an 'A' grade.

- **Commercial Address Access Time**
  93419 — 45 ns Max
  93419A — 35 ns Max
- **Military Address Access Time — 60 ns Max**
- **Fully TTL Compatible**
- **Features Open Collector Outputs**
- **Data Output is the Complement of Data Input**
- **Power Dissipation — 0.87 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

Pin Names

A_0-A_5	Address Inputs
D_0-D_8	Data Inputs
$\overline{O}_0$-$\overline{O}_8$	Inverting Data Outputs
$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{CS}$	Chip Select Input (Active LOW)

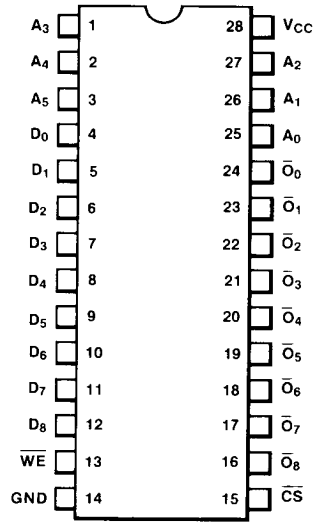
Logic Symbol



V_{CC} = Pin 28
GND = Pin 14

Connection Diagram

28-Pin DIP (Top View)



(Top View)

Note:
The 28-Pin Flatpak and the 28-Pin Leadless Chip Carrier have the same pinout as the 28-Pin DIP.

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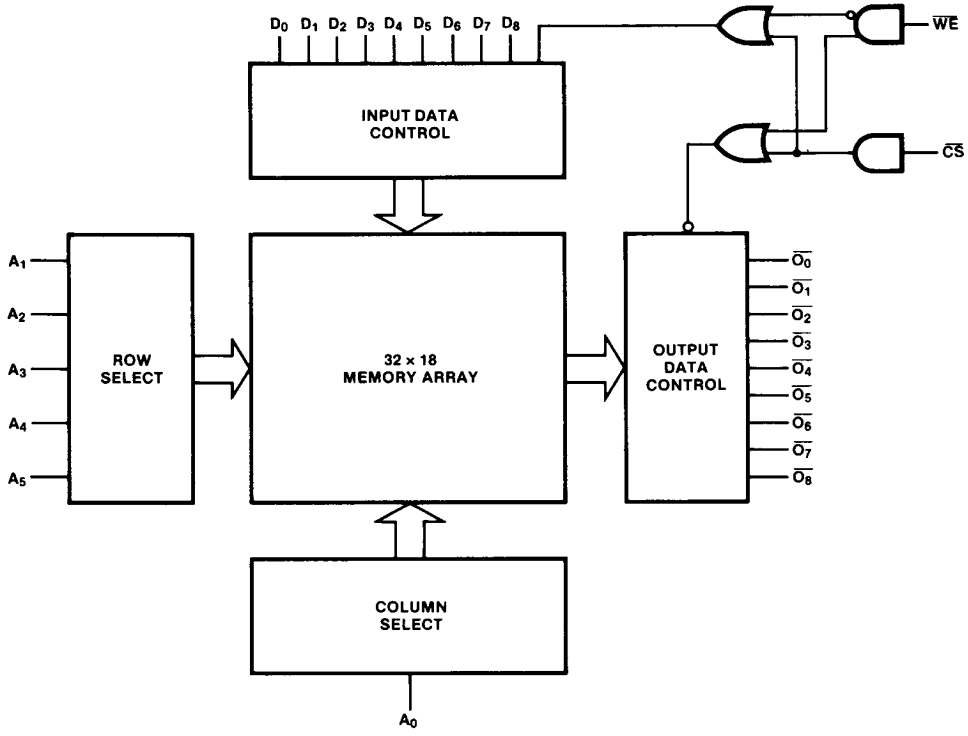
Logic Diagram



Functional Description

The 93419 is a fully decoded 576-bit random access memory organized 64 words by nine bits. Word selection is achieved by means of a 6-bit address, A_0 through A_5.

One Chip Select input is provided for easy memory array expansion of up to 128 words without the need for external decoding. For larger memories, the fast chip select access time permits decoding without an increase in overall memory access time.

The read and write functions of the 93419 are controlled by the state of the active LOW Write Enable ($\overline{WE}$) input. When $\overline{WE}$ is held LOW and the chip is selected, the data $D_0 - D_5$ is written into the location specified by the binary address present at A_0 through A_5. Since the write function is level triggered, data must be held stable at the data input for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. When $\overline{WE}$ is held HIGH and the chip selected, inverted data is read from the addressed location and presented at the outputs ($\overline{O}_0 - \overline{O}_8$).

Open collector outputs are provided to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many 93419s can be tied together. In other applications the wired-OR is not used. In either case an external pull-up resistor of R_L value must be used to provide a HIGH at the output when it is off. Any R_L value within the range specified below may be used.

$$\frac{V_{CC}(Max)}{I_{OL} - FO(1.6)} \leq R_L \leq \frac{V_{CC}(Min) - V_{OH}}{n(I_{CEX}) + FO(0.04)}$$

R_L is in kΩ
n = number of wired-OR outputs tied together
FO = number of TTL Unit Loads (UL) driven
I_{CEX} = Memory Output Leakage Current
V_{OH} = Required Output HIGH Level at Output Node
I_{OL} = Output LOW Current

The minimum R_L value is limited by the output current sinking ability. The maximum R_L value is determined by the output and input leakage current which must be supplied to hold the output at V_{OH}.
One Unit Load = 40 μA HIGH/1.6 mA LOW.

Truth Table

Inputs			Output	
$\overline{CS}$	$\overline{WE}$	D	Open Collector	Mode
H	X	X	H	Not Selected
L	L	L	H	Write "0"*
L	L	H	H	Write "1"*
L	H	X	$\overline{D_{OUT}}$*	Read

H = HIGH Voltage Level (2.4 V)
L = LOW Voltage Level (.5 V)
X = Don't Care (HIGH or LOW)
*Memory inverts from Data In to Data Out

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DC Characteristics: Over operating temperature ranges (Notes 1, 2)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition	
V_{OL}	Output LOW Voltage		0.3	0.5	V	V_{CC} = Min, I_{OL} = 12 mA	
V_{IH}	Input HIGH Voltage	2.1	1.6		V	Guaranteed Input HIGH Voltage for All Inputs[6]	
V_{IL}	Input LOW Voltage		1.5	0.8	V	Guaranteed Input LOW Voltage for All Inputs[6]	
I_{IL}	Input LOW Current		−200	−400	μA	V_{CC} = Max, V_{IN} = 0.4 V	
I_{IH}	Input HIGH Current		1.0	40 1.0	μA mA	V_{CC} = Max, V_{IN} = 4.5 V V_{CC} = Max, V_{IN} = 5.25 V	
I_{CEX}	Output Leakage Current		1.0	−100	μA	V_{CC} = Max, V_{OUT} = 4.5 V	
V_{IC}	Input Clamp Diode Voltage		−1.0	−1.5	V	V_{CC} = Max, I_{IN} = −10 mA, *Note 4*	
I_{CC}	Power Supply Current		100	150 170	mA mA	Commercial Military	V_{CC} = Max All Inputs Grounded

Notes
1. Operating specification with adequate time for temperature stabilization and transverse airflow exceeding 400 linear feet per minute. Conformance testing performed instantaneously where $T_A = T_J = T_C$. Correlated temperatures, typically 25°C and 100°C, and limits may be used to guarantee performance.
2. Typical values are at V_{CC} = 5.0 V, T_A = +25°C and maximum loading.
3. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
4. Short circuit to ground not to exceed one second.
5. Tw measured at t_{WSA} = Min, t_{WSA} measured at tw = Min.
6. Static condition only.

Commercial
AC Characteristics: V_{CC} = 5.0 V ± 5%, GND = 0 V, T_A = 0°C to +75°C (Notes 1, 3)

Symbol	Characteristic	"A" Min	"A" Max	Std Min	Std Max	Unit	Condition
	Read Timing						
t_{ACS}	Chip Select Access Time		30		40	ns	
t_{ZRCS}	Chip Select to HIGH Z		30		40	ns	*Figures 3a, 3b*
t_{AA}	Address Access Time		35		45	ns	
	Write Timing						
t_W	Write Pulse Width to Guarantee Writing[5]	25		35		ns	
t_{WSD}	Data Setup Time Prior to Write	5		5		ns	
t_{WHD}	Data Hold Time after Write	5		5		ns	
t_{WSA}	Address Setup Time Prior to Write[5]	5		5		ns	*Figure 4*
t_{WHA}	Address Hold Time after Write	5		5		ns	
t_{WSCS}	Chip Select Setup Time Prior to Write	5		5		ns	
t_{WHCS}	Chip Select Hold Time after Write	5		5		ns	
t_{ZWS}	Write Disable to HIGH Z		30		40	ns	
t_{WR}	Write Recovery Time		35		40	ns	

Military
AC Characteristics: V_{CC} = 5.0 V ± 10%, GND = 0 V, T_A = −55°C to +125°C (Notes 1, 3)

Symbol	Characteristic	Min	Max	Unit	Condition
	Read Timing				
t_{ACS}	Chip Select Access Time		40	ns	
t_{ZRCS}	Chip Select to HIGH Z		40	ns	*Figures 3a, 3b*
t_{AA}	Address Access Time		60	ns	
	Write Timing				
t_W	Write Pulse Width to Guarantee Writing[5]	45		ns	
t_{WSD}	Data Setup Time Prior to Write	5		ns	
t_{WHD}	Data Hold Time after Write	5		ns	
t_{WSA}	Address Setup Time Prior to Write[5]	10		ns	*Figure 4*
t_{WHA}	Address Hold Time after Write	5		ns	
t_{WSCS}	Chip Select Setup Time Prior to Write	5		ns	
t_{WHCS}	Chip Select Hold Time after Write	5		ns	
t_{ZWS}	Write Disable to HIGH Z		45	ns	
t_{WR}	Write Recovery Time		55	ns	

Notes on preceeding page

Fig. 1 AC Test Load

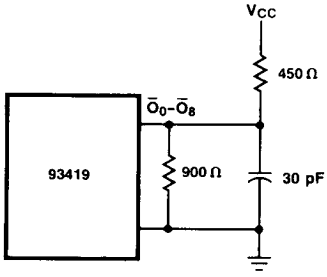


Fig. 2 Input Levels

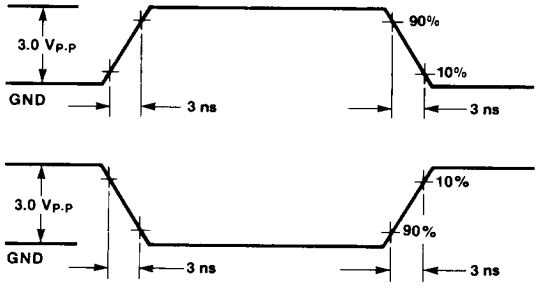
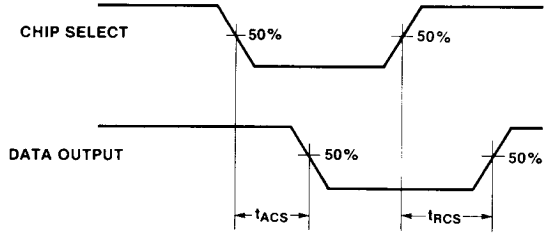


Fig. 3 Read Mode Timing

a. Read Mode Propagation Delay from Chip Select



b. Read Mode Propagation Delay from Address Inputs

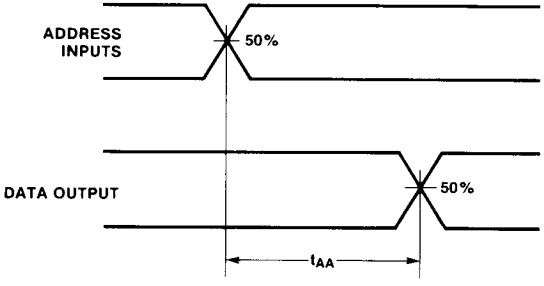


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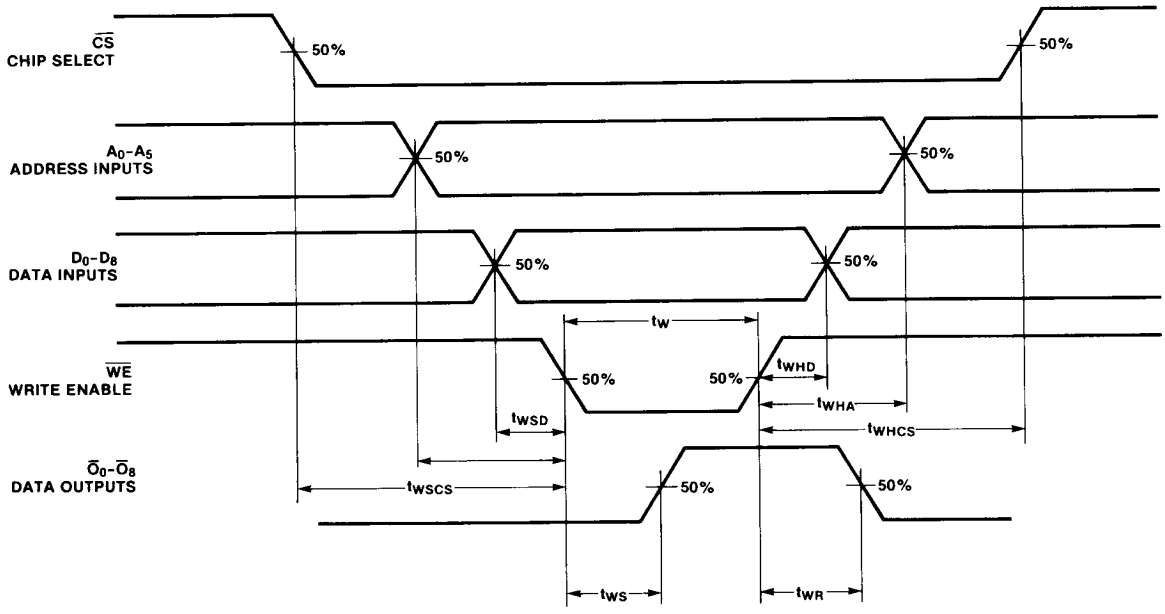
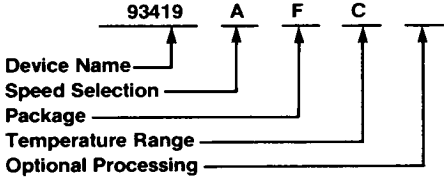
Fig. 4 Write Mode Timing



Note:
Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

Ordering Information



Speed Selection
Blank = Standard Speed
A = 'A' Grade (Commercial Only)

Packages and Outlines (See Section 10)
D = Ceramic DIP
F = Flatpak
L = Leadless Chip Carrier
P = Plastic DIP

Temperature Range
C = 0°C to +75°C
M = −55°C to +125°C

Optional Processing
QB = Mil Std 883
Method 5004 and 5005, Level B
QC = Mil Std 883
Method 5004 and 5005, Level C
QR = Commercial Device with
160 Hour Burn In