

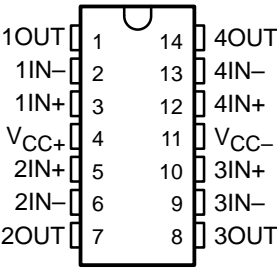
# MC3303, MC3403

## QUADRUPLE LOW-POWER OPERATIONAL AMPLIFIERS

SLOS101C – FEBRUARY 1979 – REVISED FEBRUARY 2002

- Wide Range of Supply Voltages, Single Supply . . . 3 V to 36 V or Dual Supplies
- Class AB Output Stage
- True Differential Input Stage
- Low Input Bias Current
- Internal Frequency Compensation
- Short-Circuit Protection
- Designed to Be Interchangeable With Motorola MC3303, MC3403

MC3303 . . . D, N, OR PW PACKAGE  
MC3403 . . . D, DB, N, NS, OR PW PACKAGE  
(TOP VIEW)



### description

The MC3303 and the MC3403 are quadruple operational amplifiers similar in performance to the  $\mu$ A741, but with several distinct advantages. They are designed to operate from a single supply over a range of voltages from 3 V to 36 V. Operation from split supplies also is possible, provided the difference between the two supplies is 3 V to 36 V. The common-mode input range includes the negative supply. Output range is from the negative supply to  $V_{CC} - 1.5$  V. Quiescent supply currents are less than one-half those of the  $\mu$ A741.

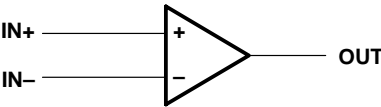
The MC3303 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ , and the MC3403 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

### AVAILABLE OPTIONS

$T_A$	$V_{IO\text{MAX}}$ AT $25^{\circ}\text{C}$	PACKAGE			
		PLASTIC SMALL OUTLINE (D, NS)	PLASTIC SHRINK SMALL OUTLINE (DB)	PLASTIC DIP (N)	PLASTIC THIN SHRINK SMALL OUTLINE (PW)
$0^{\circ}\text{C}$ to $70^{\circ}\text{C}$	10 mV	MC3403D MC3403NS	MC3403DB	MC3403N	MC3403PW
$-40^{\circ}\text{C}$ to $85^{\circ}\text{C}$	8 mV	MC3303D	—	MC3303N	MC3303PW

The D package is available taped and reeled. Add R suffix to the device type (e.g., MC3403DR). The DB, NS, and PW packages are only available taped and reeled.

### logic diagram (each amplifier)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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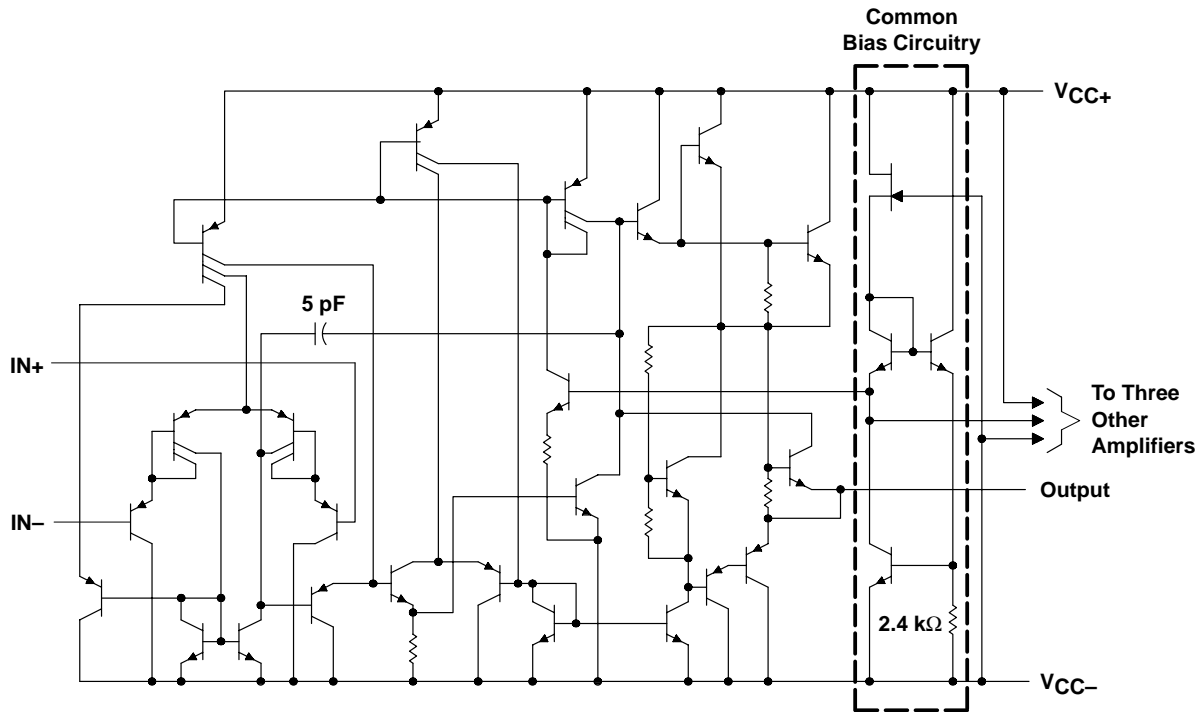
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# MC3303, MC3403

## QUADRUPLE LOW-POWER OPERATIONAL AMPLIFIERS

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### schematic (each amplifier)



Component values shown are nominal.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (see Note 1):	$V_{CC+}$	18 V
	$V_{CC-}$	–18 V
Supply voltage, $V_{CC+}$ with respect to $V_{CC-}$		36 V
Differential input voltage (see Note 2)		±36 V
Input voltage (see Notes 1 and 3)		±18 V
Package thermal impedance, $\theta_{JA}$ (see Note 4):	D package	86°C/W
	DB package	96°C/W
	N package	80°C/W
	NS package	76°C/W
	PW package	113°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C
Storage temperature range, $T_{stg}$		–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. These voltage values are with respect to the midpoint between  $V_{CC+}$  and  $V_{CC-}$ .
  2. Differential voltages are at IN+ with respect to IN–.
  3. Neither input must ever be more positive than  $V_{CC+}$  or more negative than  $V_{CC-}$ .
  4. The package thermal impedance is calculated in accordance with JESD 51-7.

# MC3303, MC3403

## QUADRUPLE LOW-POWER OPERATIONAL AMPLIFIERS

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### recommended operating conditions

				MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage			5	30	V
Dual-supply voltage		V <sub>CC+</sub>		2.5	15	V
		V <sub>CC–</sub>		–2.5	–15	V
T <sub>A</sub>	Operating free-air temperature	MC3303		–40	85	°C
		MC3403		0	70	

**electrical characteristics at specified free-air temperature, V<sub>CC+</sub> = 14 V, V<sub>CC–</sub> = 0 V for MC3303, V<sub>CC±</sub> = ±15 V for MC3403 (unless otherwise noted)**

PARAMETER	TEST CONDITIONS†		MC3303			MC3403			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>IO</sub> Input offset voltage	See Note 5	25°C		2	8		2	10	mV
		Full range			10			12	
α <sub>VIO</sub> Temperature coefficient of input offset voltage	See Note 5	Full range		10			10		μV/°C
I <sub>IO</sub> Input offset current	See Note 5	25°C		30	75		30	50	nA
		Full range			250			200	
α <sub>IIO</sub> Temperature coefficient of input offset current	See Note 5	Full range		50			50		pA/°C
I <sub>IB</sub> Input bias current	See Note 5	25°C		–0.2	–0.5		–0.2	–0.5	μA
		Full range			–1			–0.8	
V <sub>ICR</sub> Common-mode input voltage range‡		25°C	V <sub>CC–</sub> to 12	V <sub>CC–</sub> to 12.5		V <sub>CC–</sub> to 13	V <sub>CC–</sub> to 13.5		V
V <sub>OM</sub> Peak output voltage swing	R <sub>L</sub> = 10 kΩ	25°C	12	12.5		±12	±13.5		V
	R <sub>L</sub> = 2 kΩ	25°C	10	12		±10	±13		
	R <sub>L</sub> = 2 kΩ	Full range	10			±10			
A <sub>VD</sub> Large-signal differential voltage amplification	V <sub>O</sub> = ±10 V, R <sub>L</sub> = 2 kΩ	25°C	20	200		20	200		V/mV
		Full range	15			15			
B <sub>OM</sub> Maximum-output-swing bandwidth	V <sub>OPP</sub> = 20 V, A <sub>VD</sub> = 1, THD ≤ 5%, R <sub>L</sub> = 2 kΩ	25°C		9			9		kHz
B <sub>1</sub> Unity-gain bandwidth	V <sub>O</sub> = 50 mV, R <sub>L</sub> = 10 kΩ	25°C		1			1		MHz
φ <sub>m</sub> Phase margin	C <sub>L</sub> = 200 pF, R <sub>L</sub> = 2 kΩ	25°C		60°			60°		
r <sub>i</sub> Input resistance	f = 20 Hz	25°C	0.3	1		0.3	1		MΩ
r <sub>o</sub> Output resistance	f = 20 Hz	25°C		75			75		Ω
CMRR Common-mode rejection ratio	V <sub>IC</sub> = V <sub>ICRmin</sub>	25°C	70	90		70	90		dB
k <sub>SVS</sub> Supply voltage sensitivity (ΔV <sub>IO</sub> /ΔV <sub>CC</sub> )	V <sub>CC±</sub> = ±2.5 to ±15 V	25°C		30	150		30	150	μV/V
I <sub>OS</sub> Short-circuit output current§		25°C	±10	±30	±45	±10	±30	±45	mA
I <sub>CC</sub> Total supply current	No load, See Note 5	25°C		2.8	7		2.8	7	mA

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified. Full range for T<sub>A</sub> is –40°C to 85°C for MC3303, and 0°C to 70°C for MC3403.

‡ The V<sub>ICR</sub> limits are linked directly, volt-for-volt, to supply voltage; the positive limit is 2 V less than V<sub>CC+</sub>.

§ Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

NOTE 5: V<sub>IO</sub>, I<sub>IO</sub>, I<sub>IB</sub>, and I<sub>CC</sub> are defined at V<sub>O</sub> = 0 for MC3403 and V<sub>O</sub> = 7 V for MC3303.



# MC3303, MC3403

## QUADRUPLE LOW-POWER OPERATIONAL AMPLIFIERS

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electrical characteristics,  $V_{CC+} = 5\text{ V}$ ,  $V_{CC-} = 0\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MC3303			MC3403			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_O = 2.5\text{ V}$			10		2	10	mV
$I_{IO}$ Input offset current	$V_O = 2.5\text{ V}$			75		30	50	nA
$I_{IB}$ Input bias current	$V_O = 2.5\text{ V}$			–0.5		–0.2	–0.5	$\mu\text{A}$
$V_{OM}$ Peak output voltage swing‡	$R_L = 10\text{ k}\Omega$	3.3	3.5		3.3	3.5		V
	$R_L = 10\text{ k}\Omega$ , $V_{CC+} = 5\text{ V to } 30\text{ V}$	$V_{CC+} - 1.7$			$V_{CC+} - 1.7$			
$A_{VD}$ Large-signal differential voltage amplification	$V_O = 1.7\text{ V to } 3.3\text{ V}$ , $R_L = 2\text{ k}\Omega$	20	200		20	200		V/mV
$k_{SVS}$ Supply-voltage sensitivity ( $\Delta V_{IO}/\Delta V_{CC\pm}$ )	$V_{CC\pm} = \pm 2.5\text{ V to } \pm 15\text{ V}$			150			150	$\mu\text{V/V}$
$I_{CC}$ Supply current	$V_O = 2.5\text{ V}$ , No load		2.5	7		2.5	7	mA
$V_{O1}/V_{O2}$ Crosstalk attenuation	$f = 1\text{ kHz to } 20\text{ kHz}$		120			120		dB

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified.

‡ Output will swing essentially to ground.

operating characteristics,  $V_{CC+} = 14\text{ V}$ ,  $V_{CC-} = 0\text{ V}$  for MC3303,  $V_{CC\pm} = \pm 15\text{ V}$  for MC3403,  $T_A = 25^\circ\text{C}$ ,  $A_{VD} = 1$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS				TYP	UNIT
SR Slew rate at unity gain	$V_I = \pm 10\text{ V}$ ,	$C_L = 100\text{ pF}$ ,	$R_L = 2\text{ k}\Omega$ ,	See Figure 1	0.6	V/ $\mu\text{s}$
$t_r$ Rise time	$\Delta V_O = 50\text{ mV}$ ,	$C_L = 100\text{ pF}$ ,	$R_L = 10\text{ k}\Omega$ ,	See Figure 1	0.35	$\mu\text{s}$
$t_f$ Fall time	$\Delta V_O = 50\text{ mV}$ ,	$C_L = 100\text{ pF}$ ,	$R_L = 10\text{ k}\Omega$ ,	See Figure 1	0.35	$\mu\text{s}$
Overshoot factor	$\Delta V_O = 50\text{ mV}$ ,	$C_L = 100\text{ pF}$ ,	$R_L = 10\text{ k}\Omega$ ,	See Figure 1	20	%
Crossover distortion	$V_{I(PP)} = 30\text{ mV}$ ,	$V_{OPP} = 2\text{ V}$ ,	$f = 10\text{ kHz}$		1	%

### PARAMETER MEASUREMENT INFORMATION

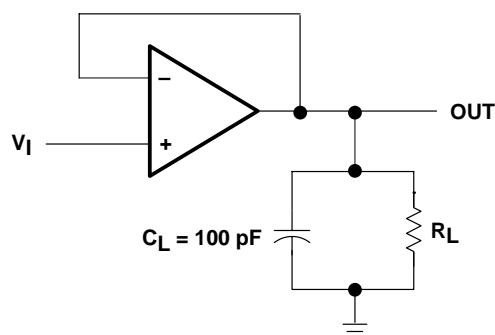


Figure 1. Unity-Gain Amplifier

# MC3303, MC3403 QUADRUPLE LOW-POWER OPERATIONAL AMPLIFIERS

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## TYPICAL CHARACTERISTICS†

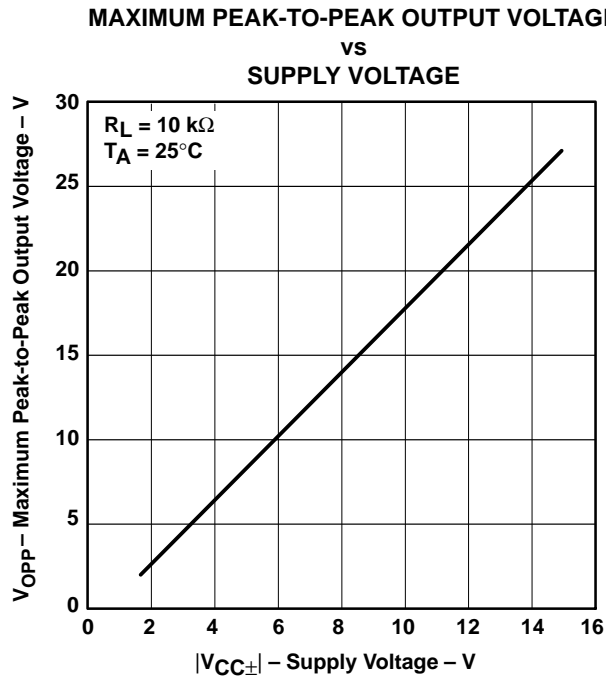


Figure 2

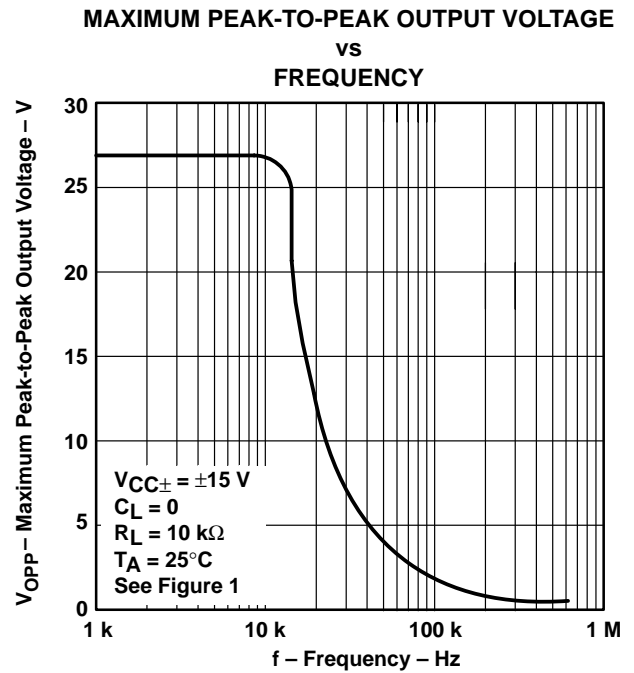


Figure 3

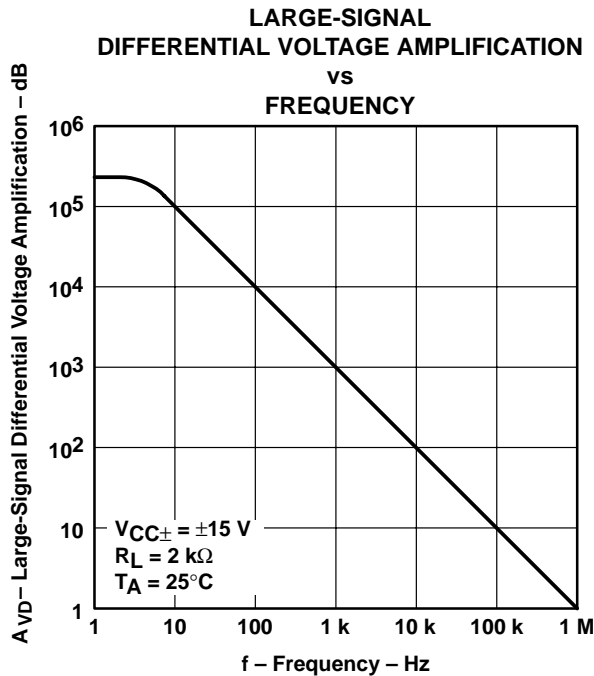


Figure 4

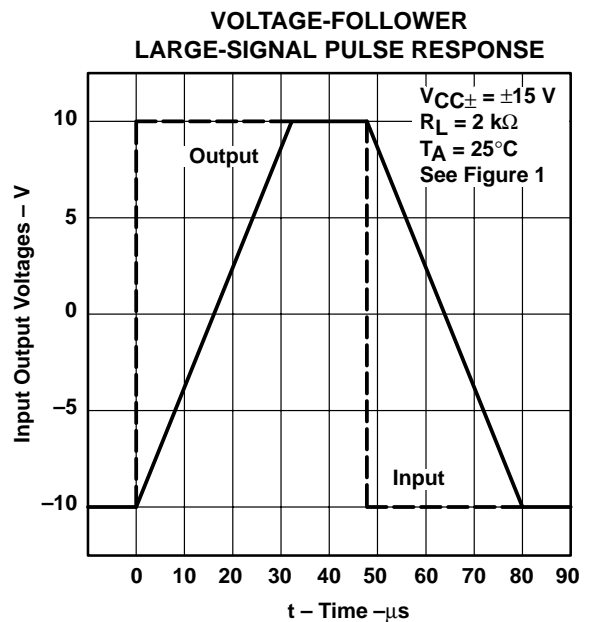


Figure 5

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

MC3303, MC3403  
QUADRUPLE LOW-POWER OPERATIONAL AMPLIFIERS

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TYPICAL CHARACTERISTICS†

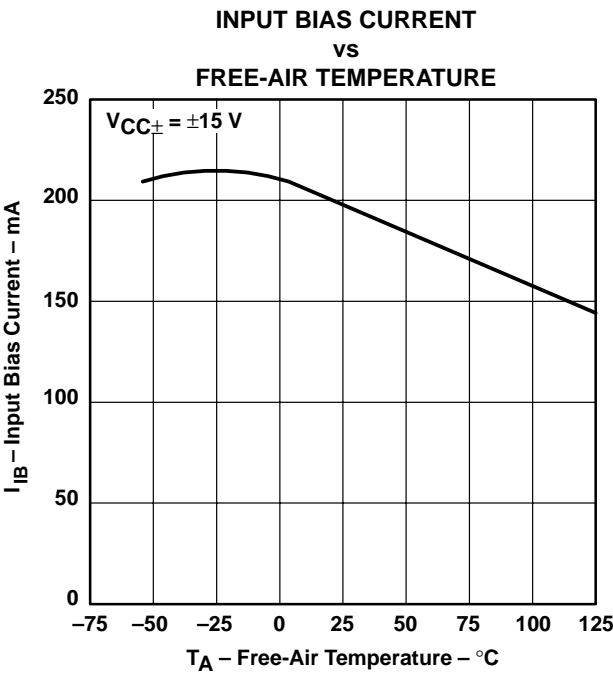


Figure 6

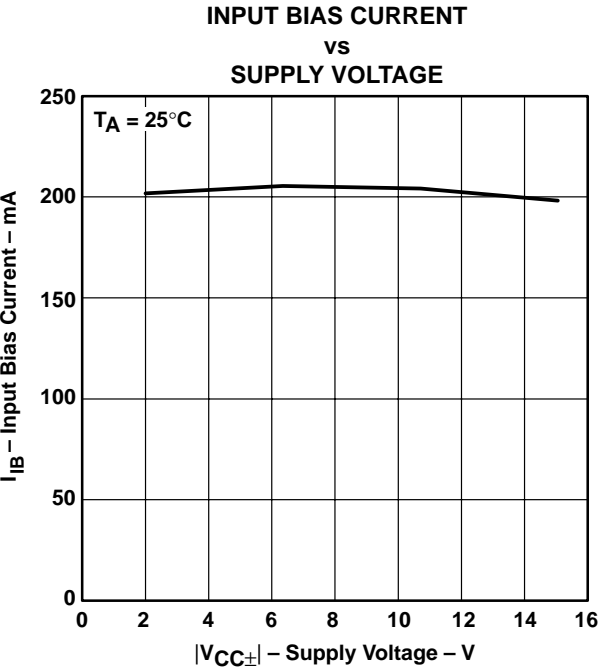


Figure 7

† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">MC3303D</a>	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	-40 to 85	MC3303
<a href="#">MC3303DR</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MC3303
<a href="#">MC3303N</a>	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	MC3303N
<a href="#">MC3303PW</a>	Obsolete	Production	TSSOP (PW)   14	-	-	Call TI	Call TI	-40 to 85	M3303
<a href="#">MC3303PWR</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	M3303
<a href="#">MC3403D</a>	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	0 to 70	MC3403
<a href="#">MC3403DR</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU   NIPDAU	Level-1-260C-UNLIM	0 to 70	MC3403
<a href="#">MC3403N</a>	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	MC3403N
<a href="#">MC3403NSR</a>	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	MC3403
<a href="#">MC3403PWR</a>	Obsolete	Production	TSSOP (PW)   14	-	-	Call TI	Call TI	0 to 70	M3403

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MC3303DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
MC3303PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MC3303PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MC3403DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
MC3403DR	SOIC	D	14	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
MC3403NSR	SOP	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MC3303DR	SOIC	D	14	2500	356.0	356.0	35.0
MC3303PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
MC3303PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
MC3403DR	SOIC	D	14	2500	353.0	353.0	32.0
MC3403DR	SOIC	D	14	2500	340.5	336.1	25.0
MC3403NSR	SOP	NS	14	2000	356.0	356.0	35.0

## TUBE



\*All dimensions are nominal

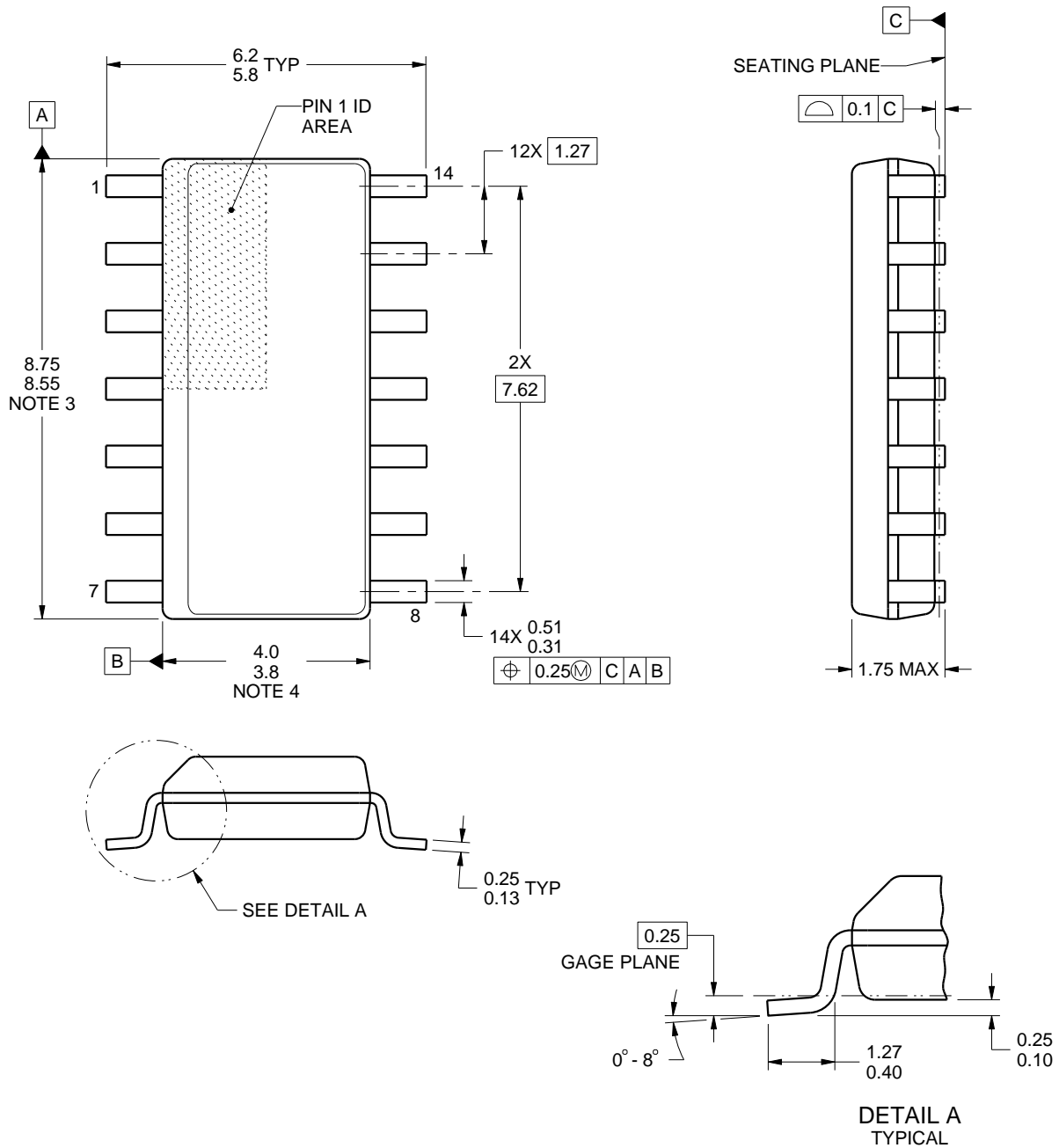
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
MC3303N	N	PDIP	14	25	506	13.97	11230	4.32
MC3303N	N	PDIP	14	25	506	13.97	11230	4.32
MC3403N	N	PDIP	14	25	506	13.97	11230	4.32
MC3403N	N	PDIP	14	25	506	13.97	11230	4.32

**D0014A**

## PACKAGE OUTLINE

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.





4220202/B 12/2023

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

**PW0014A**

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



## SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.  
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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