TMS27C510 524288-BIT UV ERASABLE PROGRAMMABLE
TMS27PC510 524288-BIT PROGRAMMABLE
READ-ONLY MEMORY

SMLS510B – AUGUST 1990 – REVISED JUNE 1995

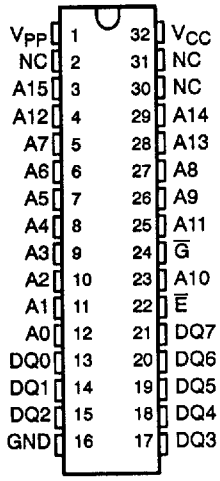
- **Organization . . . 64K × 8**
- **Single 5-V Power Supply**
- **Pin Compatible With Existing 1 Meg MOS ROMs, PROMs, and EPROMs**
- **All Inputs/Outputs Fully TTL Compatible**
- **Max Access / Min Cycle Times**

  V_{CC} ± 10%

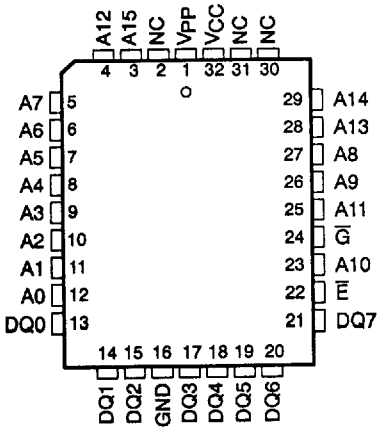
'27C510-12	120 ns
'27C/PC510-15	150 ns
'27C/PC510-17	170 ns
'27C/PC510-20	200 ns
'27C/PC510-25	250 ns

- **Power Saving CMOS Technology**
- **Very High Speed SNAP! Pulse Programming**
- **3-State Output Buffers**
- **400 mV Guaranteed DC Noise Immunity With Standard TTL Loads**
- **Latchup Immunity of 250 mA on All Input and Output Lines**
- **Low Power Dissipation (V_{CC} = 5.5 V)**
  - **Active . . . 165 mW Worst Case**
  - **Standby . . . 1.4 mW Worst Case (CMOS-Input Levels)**
- **PEP4 Version Available With 168-Hour Burn-In, and Choices of Operating Temperature Range**
- **512K EPROM Available With MIL-STD-883C Class B High Reliability Processing (SMJ27C510)**

J AND N PACKAGES
(TOP VIEW)



FM PACKAGE
(TOP VIEW)



description

The TMS27C510 series are 524288-bit, ultraviolet-light erasable, electrically programmable read-only memories.

The TMS27PC510 series are 524288-bit, one-time electrically programmable read-only memories.

These devices are fabricated using power saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors. Each output can drive one Series 74 TTL circuit without external resistors.

PIN NOMENCLATURE	
A0–A15	Address Inputs
$\overline{E}$	Chip Enable
DQ0–DQ7	Inputs (programming) / Outputs
$\overline{G}$	Output Enable
GND	Ground
NC	No Internal Connection
V_{CC}	5-V Power Supply
V_{PP}	12-13 V Power Supply

TEXAS INSTRUMENTS
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description (continued)

The data outputs are three-state for connecting multiple devices to a common bus. The TMS27C510 and the TMS27PC510 are pin compatible with 32-pin 1-megabit MOS ROMs, PROMs, and EPROMs.

The TMS27C510 EPROM is offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting-hole rows on 15,2-mm (600-mil) centers. The TMS27C510 is available with two choices of temperature ranges of 0°C to 70°C (JL suffix) and – 40°C to 85°C (JE suffix). The TMS27C510 is also offered with 168-hour burn-in on both temperature ranges (JL4 and JE4 suffixes). (See table below.)

The TMS27PC510 PROM is offered in a dual-in-line plastic package (N suffix) designed for insertion in mounting-hole rows on 15,2-mm (600-mil) centers. The TMS27PC510 is also supplied in a 32-lead plastic leaded chip-carrier package using 1,25-mm (50-mil) lead spacing (FM suffix). The TMS27PC510 is specified for operation from 0°C to 70°C, and – 40°C to 85°C.

All package styles conform to JEDEC standards.

EPROM	SUFFIX FOR OPERATING TEMPERATURE RANGES WITHOUT PEP4 BURN-IN		SUFFIX FOR PEP4 168-HR. BURN-IN VS TEMPERATURE RANGES	
	0°C TO 70°C	– 40°C TO 85°C	0°C TO 70°C	– 40°C TO 85°C
TMS27C510-XXX	JL	JE	JL4	JE4
TMS27PC510-XXX	NL, FML	NE, FME	—	NE4, FME4

These EPROMs and PROMs operate from a single 5-V supply (in the read mode), thus are ideal for use in microprocessor-based systems. One other (13-V) supply is needed for programming. All programming signals are TTL level. These devices are programmable by a SNAP! Pulse programming algorithm. The SNAP! Pulse programming algorithm uses a V_{PP} of 13.0 V and a V_{CC} of 6.5 V for a nominal programming time of seven seconds. For programming outside the system, existing EPROM programers can be used. Locations can be programmed singly, in blocks, or at random.

operation

The seven modes of operation are in the following table. Read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (13.0 V for SNAP! Pulse), and 12 V on A9 for the signature mode.

FUNCTION	MODE†							
	READ	OUTPUT DISABLE	STANDBY	PROGRAMMING	VERIFY	PROGRAM INHIBIT	SIGNATURE MODE	
$\overline{E}$	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	
$\overline{G}$	V_{IL}	V_{IH}	X	V_{IH}	V_{IL}	X	V_{IL}	
V_{PP}	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}	
V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9	X	X	X	X	X	X	V_H‡	V_H‡
A0	X	X	X	X	X	X	V_{IL}	V_{IH}
DQ0–DQ7	Data Out	Hi-Z	Hi-Z	Data In	Data Out	Hi-Z	CODE	
							MFG	DEVICE
							97	15

† X can be V_{IL} or V_{IH}.
‡ V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more TMS27C510s or TMS27PC510s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of a single device, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins DQ0 to DQ7.

latchup immunity

Latchup immunity on the TMS27C510 and TMS27PC510 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the EPROM is interfaced to industry standard TTL or MOS logic devices. Input/output layout approach controls latchup without compromising performance or packing density.

powerdown

Active I_{CC} current can be reduced from 30 mA to 500 μA by applying a high TTL input on $\overline{E}$ and to 100 μA by applying high CMOS input on $\overline{E}$. In this mode all outputs are in the high-impedance state.

erasure (TMS27C510)

Before programming, the TMS27C510 EPROM is erased by exposing the chip through the transparent lid to high intensity ultraviolet light (wavelength 2537 Å). The recommended minimum exposure dose (UV intensity × exposure time) is 15-W s/cm^2. A typical 12-mW/cm^2, filterless UV lamp erases the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C510, the window should be covered with an opaque label. After erasure (all bits in logic 1 state), logic 0s are programmed into the desired locations. A programmed zero can be erased only by ultraviolet light.

initializing (TMS27PC510)

The one-time programmable TMS27PC510 PROM is provided with all bits in logic 1 state, then logic 0s are programmed into the desired locations. Logic 0s programmed into a PROM cannot be erased.

SNAP! Pulse programming

The 512K EPROM and PROM can be programmed using the TI SNAP! Pulse programming algorithm as illustrated by the flowchart in Figure 1, which can reduce programming time to a nominal 7 seconds. Actual programming time varies as a function of the programmer used.

The SNAP! Pulse programming algorithm uses initial pulses of 100 microseconds (μs) followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to 10 (ten) 100-μs pulses per byte are provided before a failure is recognized.

The programming mode is achieved when V_{PP} = 13.0 V, V_{CC} = 6.5 V, $\overline{G} = V_{IH}$, and $\overline{E} = V_{IL}$. Data is presented in parallel (eight bits) on pins DQ0 to DQ7. Once addresses and data are stable, $\overline{E}$ is pulsed.

More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with $V_{CC} = V_{PP}$ = 5 V.

program inhibit

Programming can be inhibited by maintaining a high level input on the $\overline{E}$ pin.

program verify

Programmed bits can be verified with V_{PP} = 13.0 V when $\overline{G} = V_{IL}$ and $\overline{E} = V_{IH}$.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 is forced to 12 V ± 0.5 V. Two identifier bytes are accessed by A0; i.e., A0 = V_{IL} accesses the manufacturer code which is output on DQ0–DQ7; A0 = V_{IH} accesses the device code which is output on DQ0–DQ7. All other addresses must be held at V_{IL}. The manufacturer code for these devices is 97, and the device code is 15.

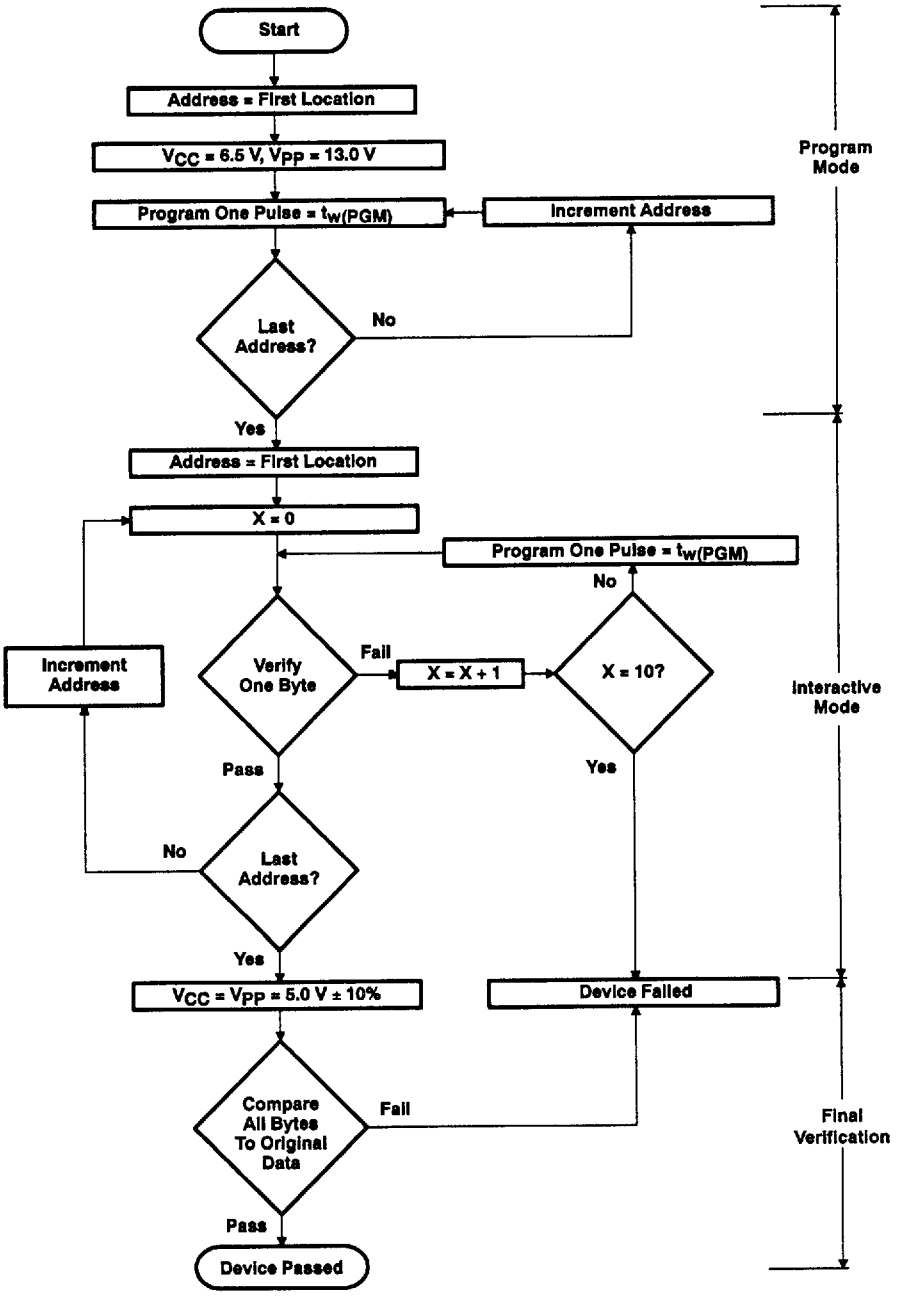
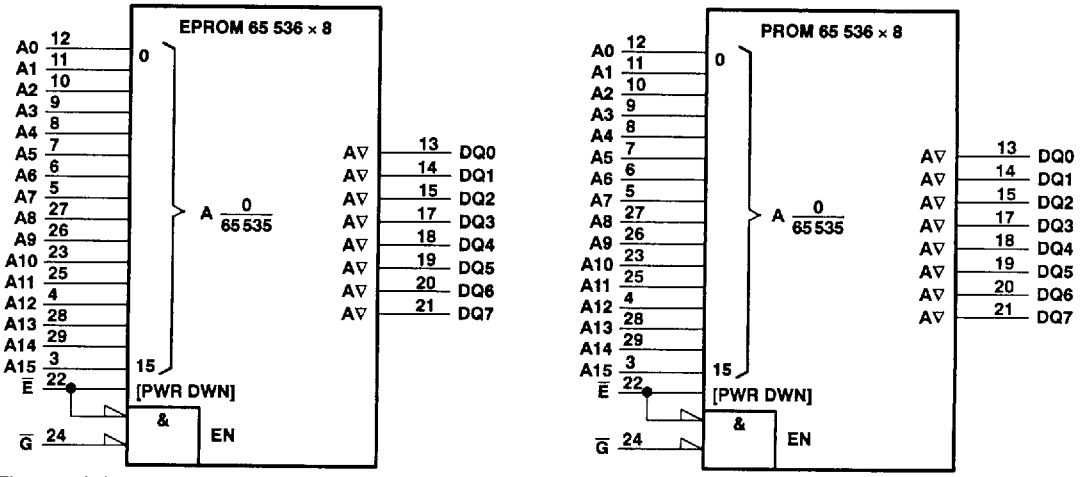


Figure 1. SNAP! Pulse Programming Flowchart

logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
J and N packages illustrated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1) ..... – 0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 1) ..... – 0.6 V to 14 V
Input voltage range (see Note 1): All inputs except A9 ..... – 0.6 V to 6.5 V
A9 ..... – 0.6 V to 13.5 V
Output voltage range (see Note 1) ..... – 0.6 V to V_{CC} + 1 V

Operating free-air temperature range ('27C510- _ _ JL and JL4;
'27PC510- _ _ NL, FML, NE, and FME) ..... 0°C to 70°C
Operating free-air temperature range ('27C510- _ _ JE, JE4, NE4, and FME4) ..... – 40°C to 85°C
Storage temperature range, T_{stg} ..... – 65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings, voltage values are with respect to GND.

recommended operating conditions

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	Read mode (see Note 2)		4.5	5	5.5	V
		SNAP! Pulse programming algorithm		6.25	6.5	6.75	
V_{PP}	Supply voltage	Read mode		$V_{CC}-0.6$		$V_{CC}+0.6$	V
		SNAP! Pulse programming algorithm		12.75	13	13.25	
V_{IH}	High-level dc input voltage		TTL	2		$V_{CC}+1$	V
			CMOS	$V_{CC}-0.2$		$V_{CC}+1$	
V_{IL}	Low-level dc input voltage		TTL	−0.5		0.8	V
			CMOS	−0.5		0.2	
T_A	Operating free-air temperature			(see Table, page 2)			°C

NOTE 2: V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		$I_{OH}=-2.5$ mA	3.5			V
			$I_{OH}=-20$ µA	$V_{CC}-0.1$			
V_{OL}	Low-level output voltage		$I_{OL}=2.1$ mA			0.4	V
			$I_{OL}=20$ µA			0.1	
I_I	Input current (leakage)		$V_I=0$ V to 5.5 V			±1	µA
I_O	Output current (leakage)		$V_O=0$ V to V_{CC}			±1	µA
I_{PP1}	V_{PP} supply current		$V_{PP}=V_{CC}=5.5$ V		1	10	µA
I_{PP2}	V_{PP} supply current (during program pulse)		$V_{PP}=13$ V		35	50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	$V_{CC}=5.5$ V, ... $\overline{E}=V_{IH}$		250	500	µA
		CMOS-input level	$V_{CC}=5.5$ V, $\overline{E}=V_{CC}$		100	250	
I_{CC2}	V_{CC} supply current (active)		$V_{CC}=5.5$ V, $\overline{E}=V_{IL}$, t_{cycle} = minimum cycle time, outputs open		15	30	mA

† Typical values are at $T_A=25°C$ and nominal voltages.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz‡

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
C_i	Input capacitance	$V_I=0$ V, f = 1 MHz		6	10	pF
C_o	Output capacitance	$V_O=0$ V, f = 1 MHz		10	14	pF

† Typical values are at $T_A=25°C$ and nominal voltages.
‡ Capacitance measurements are made on sample basis only.

switching characteristics over recommended ranges of operating conditions

PARAMETER		TEST CONDITIONS (SEE NOTES 3 AND 4)	'27C510-12 '27PC510-12		'27C510-15 '27PC510-15		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \le 20$ ns, Input $t_f \le 20$ ns		120		150	ns
$t_{a(E)}$	Access time from chip enable			120		150	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			55		75	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	45	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		ns

PARAMETER		TEST CONDITIONS (SEE NOTES 3 AND 4)	'27C510-17 '27PC510-17		'27C510-20 '27PC510-20		'27C510-25 '27PC510-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \le 20$ ns, Input $t_f \le 20$ ns		170		200		250	ns
$t_{a(E)}$	Access time from chip enable			170		200		250	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			75		75		100	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	60	0	60	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		0		ns

† Value calculated from 0.5 V delta to measured output level. This parameter is only sampled and not 100% tested.

switching characteristics for programming: V_{CC} = 6.5 V and V_{PP} = 13.0 V (SNAP! Pulse), T_A = 25°C (see Note 3)

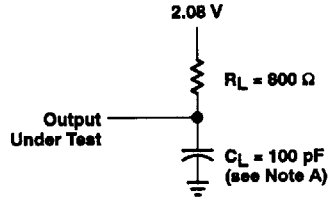
PARAMETER		MIN	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{G}$	0	130	ns
$t_{en(G)}$	Output enable time from $\overline{G}$		150	ns

recommended timing requirements for programming, V_{CC} = 6.5 V and V_{PP} = 13.0 V (SNAP! Pulse), T_A = 25°C (see Note 3)

			MIN	NOM	MAX	UNIT
$t_{w(PGM)}$	Pulse duration, program	SNAP! Pulse programming algorithm	95	100	105	µs
$t_{su(A)}$	Setup time, address		2			µs
$t_{su(G)}$	Setup time, $\overline{G}$		2			µs
$t_{su(E)}$	Setup time, $\overline{E}$		2			µs
$t_{su(D)}$	Setup time, data		2			µs
$t_{su(VPP)}$	Setup time, V_{PP}		2			µs
$t_{su(VCC)}$	Setup time, V_{CC}		2			µs
$t_{h(A)}$	Hold time, address		0			µs
$t_{h(D)}$	Hold time, data		2			µs

NOTES: 3. For all switching characteristics, the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic 1 and 0.8 V for logic 0. (Reference page 9.)
4. Common test conditions apply for the t_{dis} except during programming.

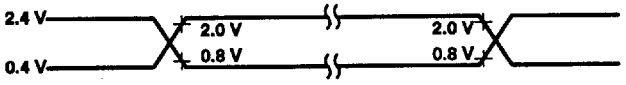
PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and fixture capacitance.

Figure 2. AC Testing Output Load Circuit

AC testing input/output wave forms



AC testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

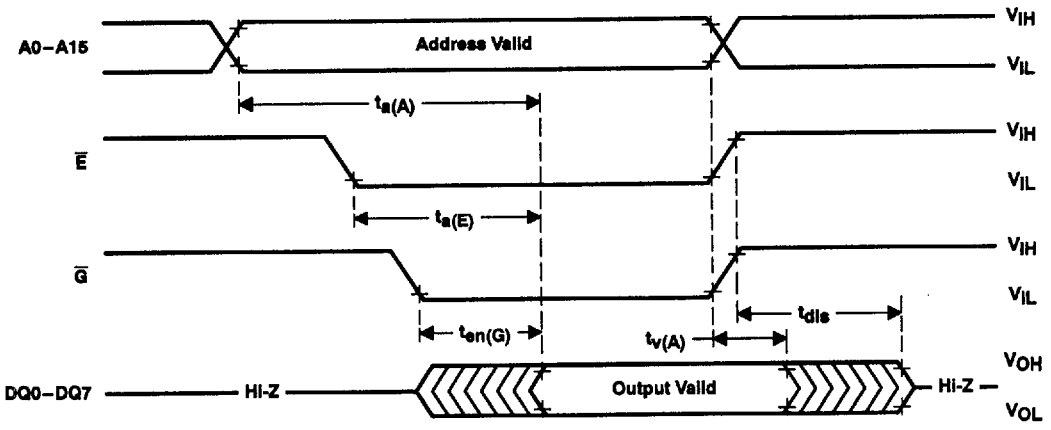
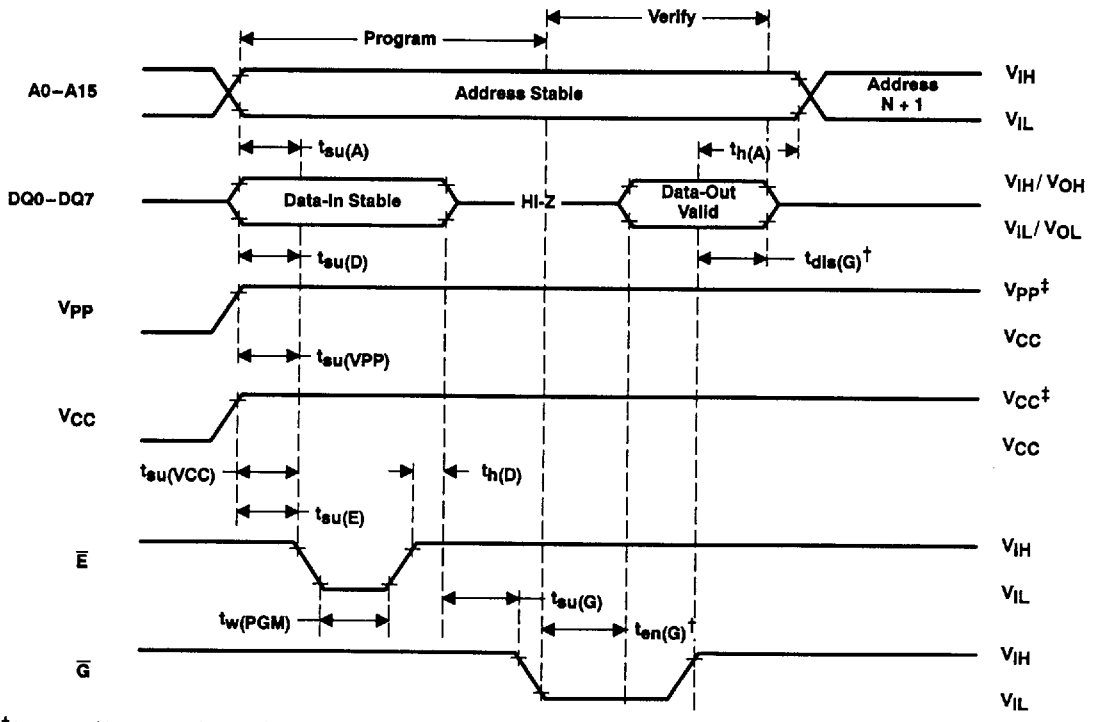


Figure 3. Read-Cycle Timing

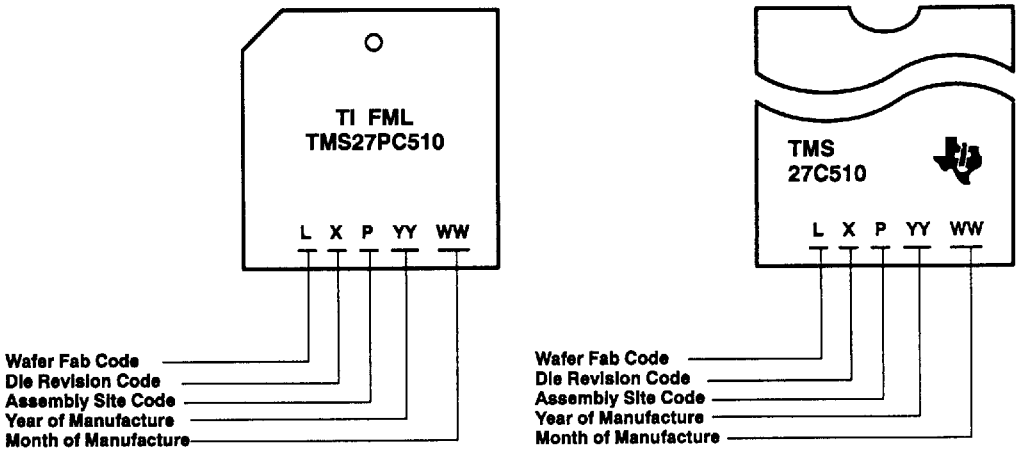
PARAMETER MEASUREMENT INFORMATION



† $t_{dis(G)}$ and $t_{en(G)}$ are characteristics of the device but must be accommodated by the programmer.
‡ 13.0-V V_{PP} and 6.5-V V_{CC} for SNAP! Pulse programming

Figure 4. Program-Cycle Timing

device symbolization



TYPICAL TMS27C/P0C510 CHARACTERISTICS