

# 1024 BIT (256 x 4) STATIC CMOS RAM

**\*Ultra Low Standby Current: 15 nA/Bit for the 5101**

- **Fast Access Time—650 ns**
- **Single +5 V Power Supply**
- **CE<sub>2</sub> Controls Unconditional Standby Mode**
- **Directly TTL Compatible—All Inputs and Outputs**
- **Three-State Output**

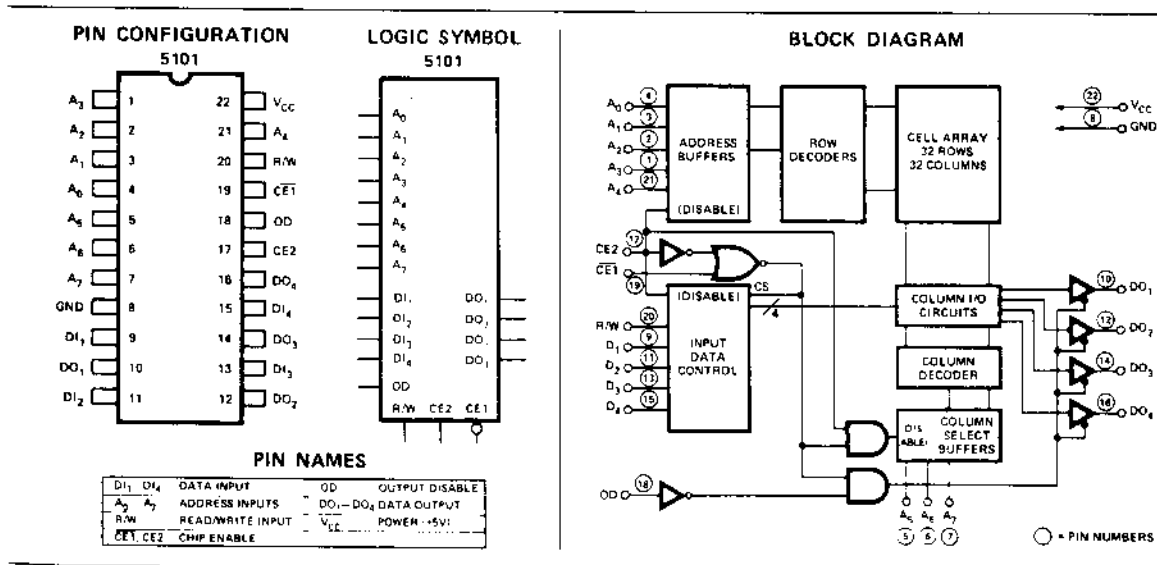
The Intel<sup>®</sup> 5101 and 5101-3 are ultra-low power 1024 bit (256 words x 4-bits) static RAMs fabricated with an advanced ion-implanted silicon gate CMOS technology. The devices have two chip enable inputs. When CE<sub>2</sub> is at a low level, the minimum standby current is drawn by these devices, regardless of any other input transitions on the addresses and other control inputs. Also, when CE<sub>1</sub> is at a high level and address and other control transitions are inhibited, the minimum standby current is drawn by these devices. When in standby the 5101 and 5101-3 draw from the single 5 volt supply only 15 microamps and 200 microamps, respectively. These devices are ideally suited for low power applications where battery operation or battery backup for non-volatility are required.

The 5101 and 5101-3 use fully DC stable (static) circuitry; it is not necessary to pulse chip select for each address transition. The data is read out non-destructively and has the same polarity as the input data. All inputs and outputs are directly TTL compatible. The 5101 and 5101-3 have separate data input and data output terminals. An output disable function is provided so that the data inputs and outputs may be wire OR-ed for use in common data I/O systems.

*The 5101L and 5101L-3 are identical to the 5101 and 5101-3, respectively, with the additional feature of guaranteed data retention at a power supply voltage as low as 2.0 volts.*

A pin compatible N-channel static RAM, the Intel 2101, is also available for low cost applications where a 256 x 4 organization is needed.

The Intel ion-implanted, silicon gate, complementary MOS (CMOS) allows the design and production of ultra-low power, high performance memories.



# SILICON GATE CMOS 5101, 5101-3, 5101L, 5101L-3

## Absolute Maximum Ratings \*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to +150°C
Voltage On Any Pin	
With Respect to Ground	-0.3V to V <sub>CC</sub> +0.3V
Maximum Power Supply Voltage	+7.0V
Power Dissipation	1 Watt

## \*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## D. C. and Operating Characteristics for 5101, 5101-3, 5101L, 5101L-3

T<sub>A</sub> = 0°C to 70°C, V<sub>CC</sub> = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Typ. <sup>[1]</sup>	Max.	Unit	Test Conditions
I <sub>LI</sub> <sup>[2]</sup>	Input Current		5		nA	V <sub>IN</sub> = 0 to 5.25V
I <sub>LOH</sub> <sup>[2]</sup>	Output High Leakage			1	μA	CE1 = 2.2V, V <sub>OUT</sub> = V <sub>CC</sub>
I <sub>LOL</sub> <sup>[2]</sup>	Output Low Leakage			1	μA	CE1 = 2.2V, V <sub>OUT</sub> = 0.0V
I <sub>CC1</sub>	Operating Current		9	22	mA	V <sub>IN</sub> = V <sub>CC</sub> Except CE1 ≤ 0.01V Outputs Open
I <sub>CC2</sub>	Operating Current		13	27	mA	V <sub>IN</sub> = 2.2V Except CE1 ≤ 0.65V Outputs Open
5101 I <sub>CCCL</sub> <sup>[2]</sup>	Standby Current			15	μA	V <sub>IN</sub> = 0 to V <sub>CC</sub> , Except CE2 ≤ 0.2V
5101-3 I <sub>CCCL</sub> <sup>[2]</sup>	Standby Current			200	μA	V <sub>IN</sub> = 0 to V <sub>CC</sub> , Except CE2 ≤ 0.2V
V <sub>IL</sub>	Input "Low" Voltage	-0.3		0.65	V	
V <sub>IH</sub>	Input "High" Voltage	2.2		V <sub>CC</sub>	V	
V <sub>OL</sub>	Output "Low" Voltage			0.4	V	I <sub>OL</sub> = 2.0mA
V <sub>OH</sub>	Output "High" Voltage	2.4			V	I <sub>OH</sub> = 1.0mA

## Low V<sub>CC</sub> Data Retention Characteristics (For 5101L and 5101L-3) T<sub>A</sub> = 0°C to 70°C

Symbol	Parameter	Min.	Typ. <sup>[1]</sup>	Max.	Unit	Test Conditions
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention	2.0			V	
5101L I <sub>CCDR</sub>	Data Retention Current			15	μA	CE2 ≤ 0.2V V <sub>DR</sub> = 2.0V
5101L-3 I <sub>CCDR</sub>	Data Retention Current			200	μA	
t <sub>CDR</sub>	Chip Deselect to Data Retention Time	0			ns	
t <sub>R</sub>	Operation Recovery Time	t <sub>RC</sub> <sup>[3]</sup>			ns	

NOTES: 1. Typical values are T<sub>A</sub> = 25°C and nominal supply voltage. 2. Current through all inputs and outputs included in I<sub>CCCL</sub> measurement. 3. t<sub>RC</sub> = Read Cycle Time.

# SILICON GATE CMOS 5101, 5101-3, 5101L, 5101L-3

## A.C. Characteristics for 5101, 5101-3, 5101L, 5101L-3

READ CYCLE  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5\text{V} \pm 5\%$ , unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$t_{RC}$	Read Cycle	650			ns	(See below)
$t_A$	Access Time			650	ns	
$t_{CO1}$	Chip Enable (CE1) to Output			600	ns	
$t_{CO2}$	Chip Enable (CE2) to Output			700	ns	
$t_{OD}$	Output Disable To Output			350	ns	
$t_{DF}$	Data Output to High Z State	0		150	ns	
$t_{OH1}$	Previous Read Data Valid with Respect to Address Change	0			ns	
$t_{OH2}$	Previous Read Data Valid with Respect to Chip Enable	0			ns	

### WRITE CYCLE

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$t_{WC}$	Write Cycle	650			ns	(See below)
$t_{AW}$	Write Delay	150			ns	
$t_{CW1}$	Chip Enable (CE1) To Write	550			ns	
$t_{CW2}$	Chip Enable (CE2) To Write	550			ns	
$t_{DW}$	Data Setup	400			ns	
$t_{DH}$	Data Hold	100			ns	
$t_{WP}$	Write Pulse	400			ns	
$t_{WR}$	Write Recovery	50			ns	
$t_{DS}$	Output Disable Setup	150			ns	

### A. C. CONDITIONS OF TEST

Input Pulse Levels: +0.65 Volt to 2.2 Volt

Input Pulse Rise and Fall Times: 20nsec

Timing Measurement Reference Level: 1.5 Volt

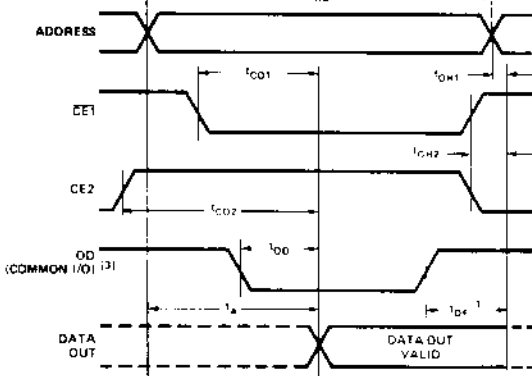
Output Load: 1 TTL Gate and  $C_L = 100\text{pF}$

### Capacitance<sup>[2]</sup> $T_A = 25^\circ\text{C}$ , $f = 1\text{MHz}$

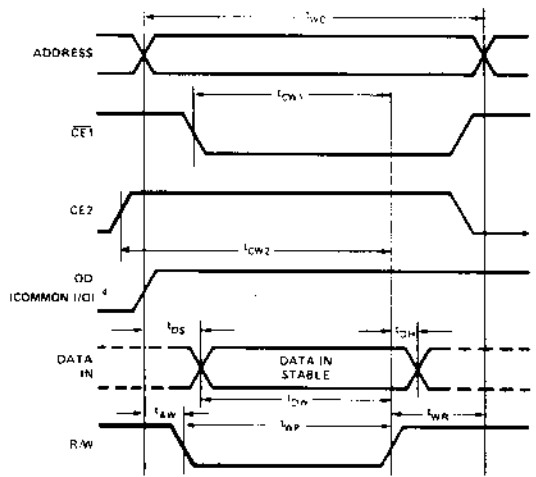
Symbol	Test	Limits (pF)	
		Typ.	Max.
$C_{IN}$	Input Capacitance (All Input Pins) $V_{IN} = 0\text{V}$	4	8
$C_{OUT}$	Output Capacitance $V_{OUT} = 0\text{V}$	8	12

Waveforms

READ CYCLE



WRITE CYCLE



- 1. Typical values are for  $T_A = 25^\circ\text{C}$  and nominal supply voltage.
- 2. This parameter is periodically sampled and is not 100% tested.
- 3. OD may be tied low for separate I/O operation.
- 4. During the write cycle, OD is "high" for common I/O and "don't care" for separate I/O operation.

Low  $V_{CC}$  Data Retention

