INTERSIL

IM7027/MK4027 Dynamic RAM 4096 Bit (4K x 1)

FEATURES

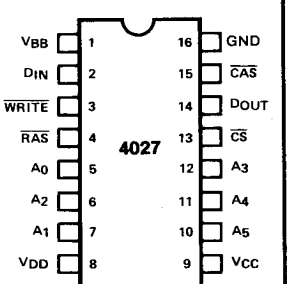
- 4096 X 1 Bit Organization
- Gated $\overline{CAS}$
- $\overline{RAS}$ Only Refresh
- All Inputs TTL Compatible
- On-Chip Latches for Addresses, Chip Select and Data In
- 10% Supply Tolerances (+12V, +5V, -5V)
- Three-State TTL Compatible Output
- Low Power Dissipation
  —470 mW Operating
  — 27 mW Standby
- Chip Select Decode Does Not Add to Access Time
- Output Data Latched and Valid Into Next Cycle
- N-Channel Silicon Gate Technology
- Pin and Performance Compatibility with Mostek MK4027

GENERAL DESCRIPTION

The IM7027 is a 4096 X 1 bit dynamic random access memory which is packaged in 16 pin DIP. The cell array is organized into 64 rows of 64 cells. Each of the 64 row addresses requires refreshing every 2 milliseconds. Any read cycle refreshes the selected row as does a refresh cycle using $\overline{RAS}$ only. A write, read/write or read/modify/write cycle also refreshes the selected row, but non-accessed chips should not be selected to avoid writing data into the selected row. A page-mode feature is included to reduce the access and/or cycle time for block data operations. Page-mode operation is useful in direct memory access (DMA) operations.

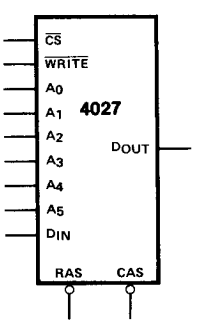
System oriented features include direct interfacing with TTL, on-chip registers which eliminate the need for interface registers, logic input levels selected for best noise immunity. Twelve address bits are required to decode 1 of 4096 cell locations, and are multiplexed onto 6 address pins and latched into the row and column address latches. The Row Address Strobe ($\overline{RAS}$) latches the 6 row address bits onto the chip. The Column Address Strobe ($\overline{CAS}$) latches the 6 column address bits and Chip Select ($\overline{CS}$) onto the chip. Since the Chip Select signal is not required until well into the cycle, its decoding time does not add to the system address or cycle time.

PIN CONFIGURATION

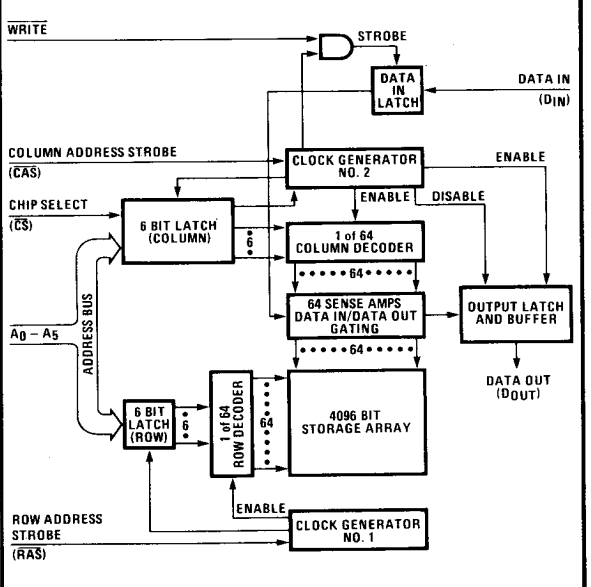


(outline dwg JE)

LOGIC SYMBOL



BLOCK DIAGRAM



ORDERING INFORMATION

ORDER NUMBER	ACCESS TIME	CYCLE TIME	PACKAGE
IM7027-1CJE	120 ns	250 ns	16 PIN CERDIP
MK4072P-2	150 ns	320 ns	16 PIN CERDIP
MK4027P-3	200 ns	375 ns	16 PIN CERDIP
MK4027P-4	250 ns	375 ns	16 PIN CERDIP

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ABSOLUTE MAXIMUM RATINGS

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . -55°C to +150°C
Voltage On Any Pin w/Respect to V_{BB} . . . . . -0.5V to +20.0V
Power Dissipation 1W

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

DC CHARACTERISTICS

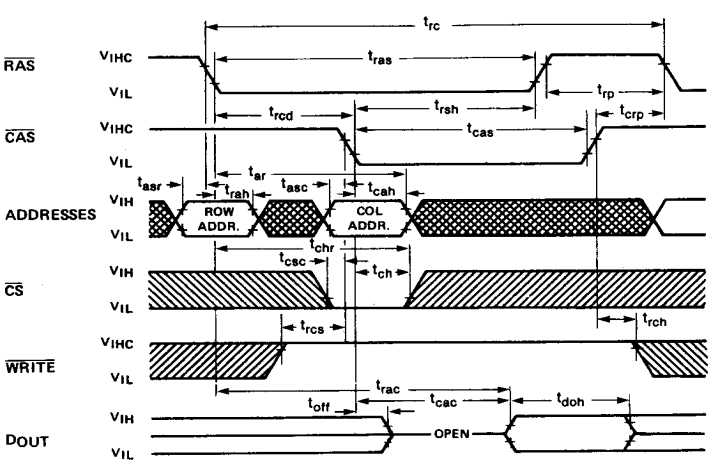
TEST CONDITIONS: V_{DD} = +12.0V ± 10%, V_{CC} = +5.0V ±10%, V_{BB} = -5.0V ±10%, T_A = 0°C to +70°C

	SYMBOL	PARAMETER		MIN	MAX	UNITS	NOTES
1	V_{IHC}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$ Voltage High		2.4	7.0	V	
2	V_{IH}	Input Voltage High		2.2	7.0	V	
3	V_{IL}	Input Voltage Low		-1.0	0.8	V	
4	I_{ILK}	Input Leakage Current			10	µA	4
5	I_{OLK}	Output Leakage Current			10	µA	5, 6
6	I_{DD1}	Average V_{DD} Power Supply Current			35	mA	2
7	I_{CC}	V_{CC} Power Supply Current					3
8	I_{BB}	Average V_{BB} Power Supply Current	-2, -3, -4		300	µA	
			-1		400	µA	
9	I_{DD2}	Standby V_{DD} Power Supply Current			2	mA	5
10	I_{DD3}	Average V_{DD} Current ("$\overline{RAS}$ Only" Refresh)			25	mA	
11	V_{OH}	Output Voltage High I_{OH} = -5 mA		2.4		V	
12	V_{OL}	Output Voltage Low I_{OL} = 3.2 mA			0.4	V	

NOTES:
1. V_{BB} must be applied before and removed after other supply voltages.
2. I_{DD1} (max) measured at ^tRC (min). I_{DD1} is proportional to cycle rate.
3. I_{CC} depends on output loading.
4. All pins except V_{BB} at 0V, V_{BB} = -5V and test pin = +10V.
5. Output disabled, $\overline{RAS}$ and $\overline{CAS} \geq V_{IHC}$ (min).
6. $0V \leq V_{OUT} \leq +10V$.

TIMING DIAGRAMS

READ AND REFRESH CYCLE



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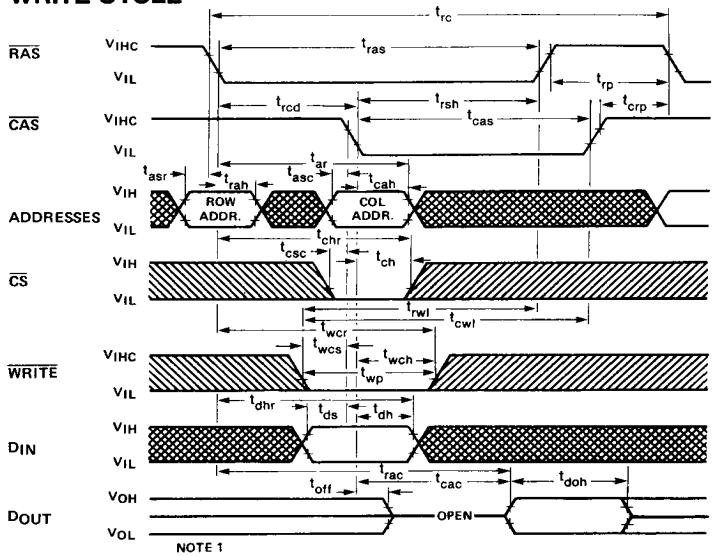
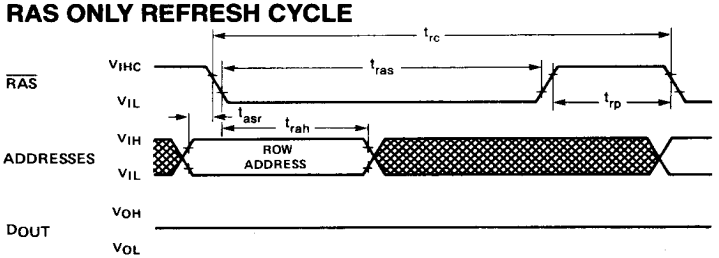
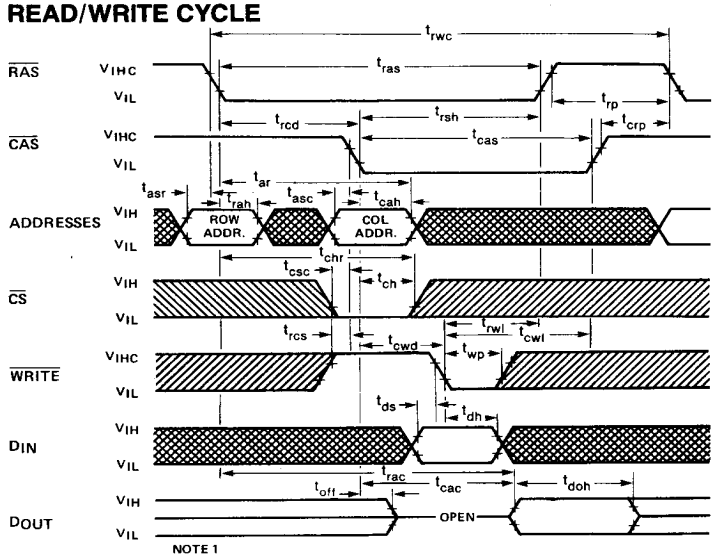
WRITE CYCLE



RAS ONLY REFRESH CYCLE



READ/WRITE CYCLE



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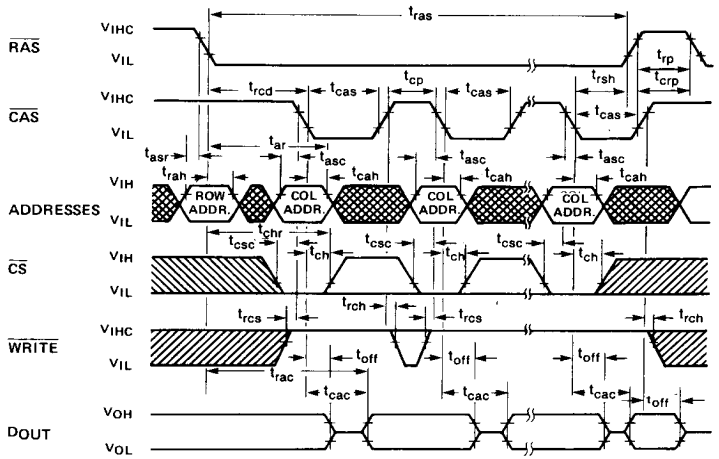
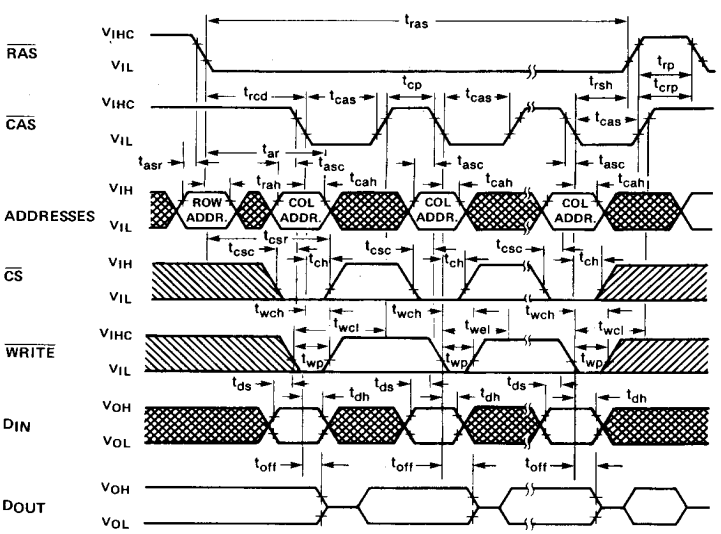
TIMING DIAGRAMS (Continued)

PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



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AC CHARACTERISTICS

TEST CONDITIONS: V_{DD} = +12.0V ± 10%, V_{CC} = +5.0V ± 10%, V_{SS} = 0V, V_{BB} = −5.0V ± 10%, T_A = 0°C to +70°C (NOTES 1, 5 and 8)

	SYMBOL	PARAMETER	IM7027-1CJE		MK4027 P-2		MK4027 P-3		MK4027 P-4		UNITS	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{rc}	Random Read or Write Cycle Time	250		320		375		375		ns	2
2	t_{rwc}	Read Write Cycle Time	325		330		420		480		ns	
3	t_{rac}	Access Time from Row Address Strobe		120		150		200		250	ns	3
4	t_{cac}	Access Time from Column Address Strobe		80		100		135		165	ns	3
5	t_{off}	Output Buffer Turn-off Delay		40		40		50		60	ns	
6	t_{rp}	Row Address Strobe Precharge Time	80		100		120		120		ns	
7	t_{ras}	Row Address Strobe Pulse Width	120	10,000	150	10,000	200	10,000	250	10,000	ns	
8	t_{rsh}	Row Address Strobe Hold Time	80		100		135		165		ns	
9	t_{cas}	Column Address Strobe Pulse Width	80		100		135		165		ns	
10	t_{rcd}	Row to Column Strobe Delay	20	40	20	50	25	65	35	85	ns	4
11	t_{asr}	Row Address Set-up Time	0		0		0		0		ns	
12	t_{rah}	Row Address Hold Time	20		20		25		35		ns	
13	t_{asc}	Column Address Set-up Time	0		−10		−10		−10		ns	
14	t_{cah}	Column Address Hold Time	45		45		55		75		ns	
15	t_{ar}	Column Address Hold Time Referenced to $\overline{RAS}$	95		95		120		160		ns	
16	t_{csc}	Chip Select Set-up Time	−10		−10		−10		−10		ns	
17	t_{ch}	Chip Select Hold Time	45		45		55		75		ns	
18	t_{chr}	Chip Select Hold Time Referenced to $\overline{RAS}$	95		95		120		160		ns	
19	t_t	Transition Time (Rise and Fall)	3	35	3	35	3	50	3	50	ns	
20	t_{rcs}	Read Command Set-up Time	0		0		0		0		ns	
21	t_{rch}	Read Command Hold Time	0		0		0		0		ns	
22	t_{wch}	Write Command Hold Time	45		45		55		75		ns	
23	t_{wcr}	Write Command Hold Time Referenced to $\overline{RAS}$	95		95		120		160		ns	
24	t_{wp}	Write Command Pulse Width	45		45		55		75		ns	
25	t_{rwl}	Write Command to Row Strobe Lead Time	50		50		70		85		ns	
26	t_{cwl}	Write Command to Column Strobe Lead Time	50		50		70		85		ns	
27	t_{ds}	Data in Set-up Time	0		0		0		0		ns	7
28	t_{dh}	Data in Hold Time	45		45		55		75		ns	7
29	t_{dhr}	Data in Hold Time Referenced to $\overline{RAS}$	95		95		120		160		ns	
30	t_{crp}	Column to Row Strobe Precharge Time	0		0		0		0		ns	
31	t_{cp}	Column Precharge Time	60		60		80		110		ns	
32	t_{rfsh}	Refresh Period		2		2		2		2	ms	
33	t_{wcs}	Write Command Set-up Time	0		0		0		0		ns	6
34	t_{cwd}	$\overline{CAS}$ to $\overline{WRITE}$ Delay	60		60		80		90		ns	6
35	t_{rwd}	$\overline{RAS}$ to $\overline{WRITE}$ Delay	110		110		145		175		ns	6
36	t_{doh}	Data Out Hold Time	10		10		10		10		ns	

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NOTES 1: t_t = 5 ns unless otherwise noted.
2: $t_{rc} > t_{ras} + t_{rp} + 2\,t_t$ to limit power dissipation.
3: Load = 2 TTL + 100 pF.
4: If t_{rcd} is greater than t_{rcd} (max) access time is controlled by t_{cac}.
5: V_{ihc} (min), V_{ih} (min) and V_{il} (max) are reference levels.
6: t_{wcs}, t_{cwd} and t_{rwd} are not restrictive parameters, they are electrical characteristics only as follows:
   a. $t_{cwd} + t_t \leq t_{cwd}$ minimum output latch contains data written into current address.
   b. $t_{cwd} \geq t_{cwd}$ (max) + t_t and $t_{rwd} \geq t_{rwd}$ (max) + t_t the data output latch contains data read from the current address.
   c. If t_{cwd} does not meet the above, data output state is indeterminate.
7: Referenced to latest of $\overline{CAS}$ or $\overline{WRITE}$.
8: Any 8 cycles that perform refresh are required after power is applied.

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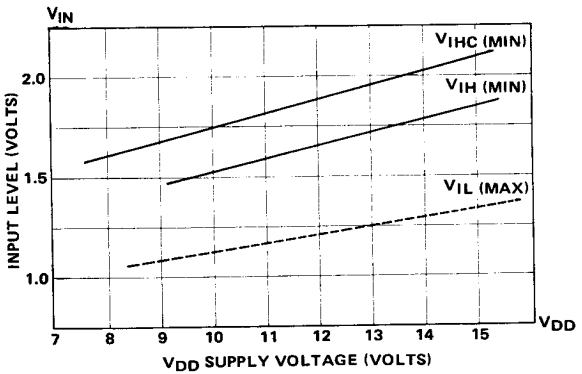
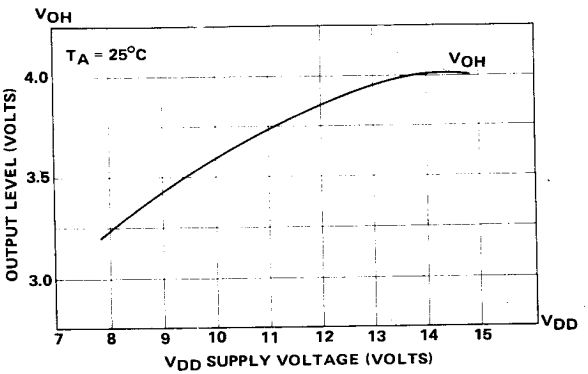
TYPICAL DEVICE CHARACTERISTICS

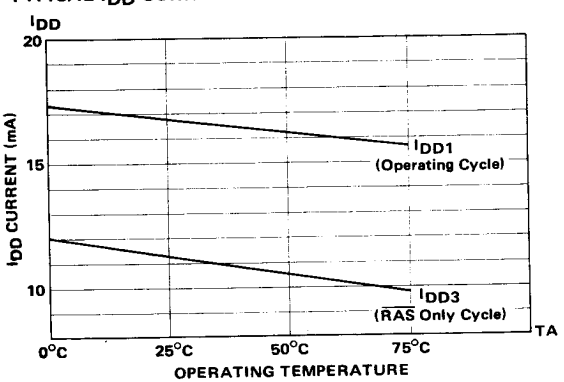
TYPICAL ADDRESS DATA INPUT LEVELS VS. V_{DD}



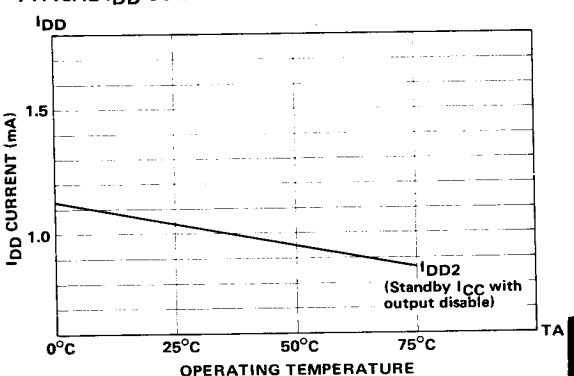
TYPICAL DATA OUTPUT LEVEL VS. V_{DD}



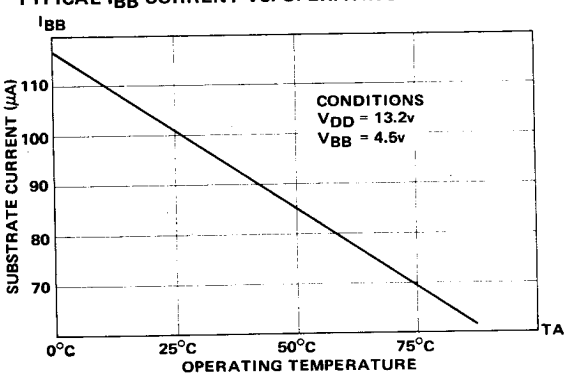
TYPICAL I_{DD} CURRENT VS. OPERATING TEMPERATURE



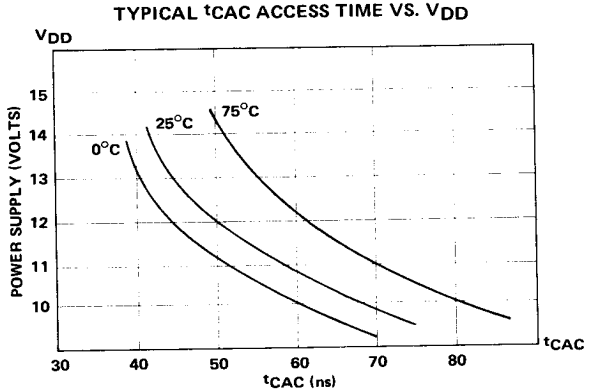
TYPICAL I_{DD} CURRENT VS. OPERATING TEMPERATURE



TYPICAL I_{BB} CURRENT VS. OPERATING TEMPERATURE



TYPICAL t_{CAC} ACCESS TIME VS. V_{DD}



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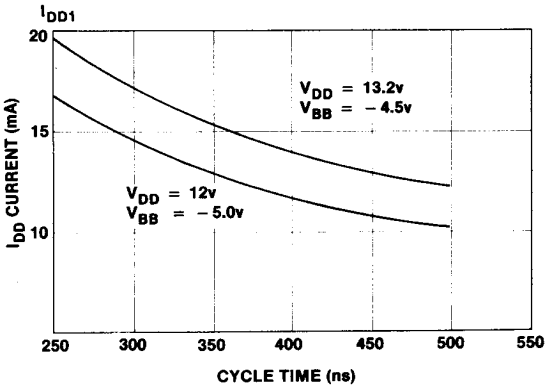
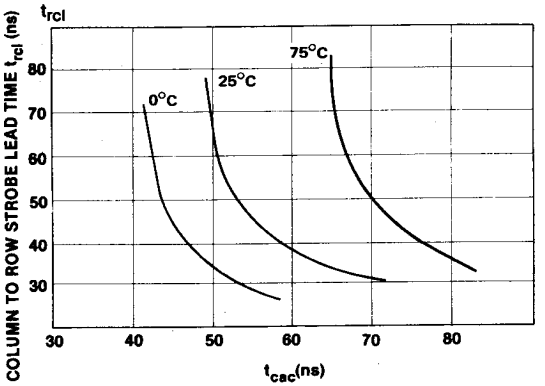
TYPICAL DEVICE CHARACTERISTICS (Continued)

TYPICAL I_{DD} CURRENT VS. CYCLE TIME

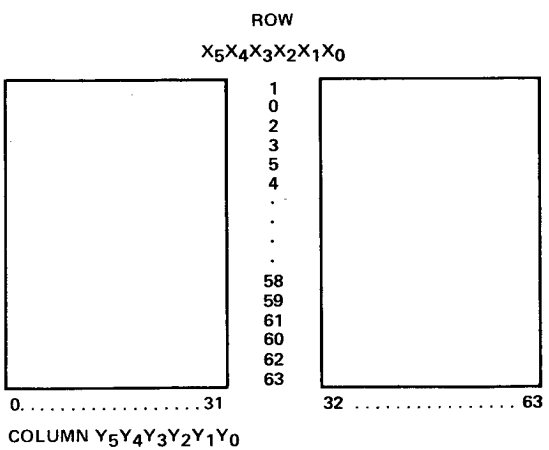


TYPICAL t_{cac} VS. t_{rcl}



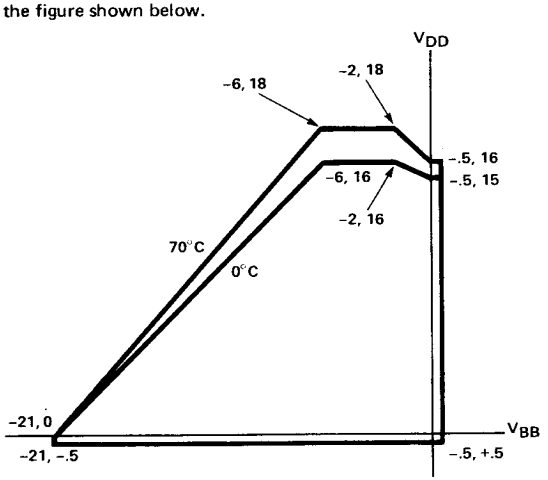
BIT MAP

The memory cells are divided into 2 groups each organized as 64 rows by 32 columns. The column addresses run in pure binary order for Y_5 Y_4 Y_3 Y_2 Y_1 Y_0, where Y_5 is most significant. The row addresses run in binary order for X_5 X_4 X_3 X_2 X_1 X_0 except for X_1 and X_0 which run 1, 0, 2, 3 and repeat. The folded bit line approach requires that data be be stored either true or false depending on the row selected. If X_0 is at logic "0", data is stored true. If X_0 is at logic "1", data is stored false.



MAXIMUM STRESS VOLTAGES

It is of interest to know worst case stress voltages for power supply failure and/or turn-on conditions. The 7027 can tolerate combinations of V_{BB}, V_{DD} that operate within the curves of the figure shown below.



CAPACITANCE

TEST CONDITIONS: V_{IN} = OV, f = 1 MHz (NOTE 1)

	SYMBOL	PARAMETER	TYP	MAX	UNIT
1	C_{I1}	D_{IN}, $\overline{CS}$ Input Capacitance A_0 - A_5	3	5	pF
2	C_{I2}	Input Capacitance, $\overline{RAS}$, $\overline{CAS}$ $\overline{WRITE}$	5	7	
3	C_O	Output Capacitance, D_{OUT}	5	7	

NOTE 1: These parameters are characterized and periodically sampled but not 100% tested.

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