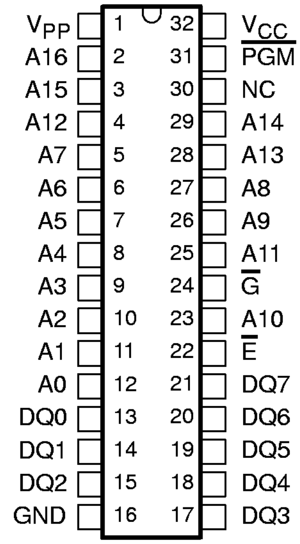
- **Organization . . . 131072 by 8 Bits**
- **Single 5-V Power Supply**
- **Operationally Compatible With Existing Megabit EPROMs**
- **Industry Standard 32-Pin Ceramic Dual-In-line Package (J Suffix)**
- **All Inputs/Outputs Fully TTL-Compatible**
- **Maximum Access/Minimum Cycle Time**
  V_{CC} ± 10%
  ’27C010A-12 120 ns
  ’27C010A-15 150 ns
  ’27C010A-20 200 ns
- **8-Bit Output for Use in Microprocessor-Based Systems**
- **Very High-Speed SNAP! Pulse Programming**
- **Power-Saving CMOS Technology**
- **3-State Output Buffers**
- **400-mV Minimum DC Noise Immunity With Standard TTL Loads**
- **Latchup Immunity of 250 mA on All Input and Output Pins**
- **No Pullup Resistors Required**
- **Low Power Dissipation (V_{CC} = 5.5 V)**
  - **Active . . . 165 mW Worst Case**
  - **Standby . . . 0.55 mW Worst Case (CMOS-Input Levels)**

J PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0–A16	Address Inputs
DQ0–DQ7	Inputs (programming)/ Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
NC	No Internal Connection
$\overline{PGM}$	Program
V_{CC}	5-V Power Supply
V_{PP}	13-V Power Supply†

† Only in program mode

description

The SMJ27C010A series are 131072 by 8-bit (1048576-bit), ultraviolet (UV) light erasable, electrically programmable read-only memories (EPROMs).

These devices are fabricated using power-saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 54 TTL circuits without the use of external pullup resistors. Each output can drive one Series 54 TTL circuit without external resistors.

The SMJ27C010A EPROM is offered in a ceramic dual-in-line package (J suffix) designed for insertion in mounting-hole rows on 15,2-mm (600-mil) centers.

These EPROMs operate from a single 5-V supply (in the read mode), and therefore, are ideal for use in microprocessor-based systems. One other 13-V supply is needed for programming. All programming signals are TTL level. These devices are programmable using the SNAP! Pulse programming algorithm. The SNAP! Pulse programming algorithm uses a V_{PP} of 13 V and a V_{CC} of 6.5 V for a nominal programming time of thirteen seconds. For programming outside the system, existing EPROM programmers can be used. Locations can be programmed singly, in blocks, or at random.

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operation

The seven modes of operation are listed in Table 1. The read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (13 V for SNAP! Pulse), and 12 V on A9 for signature mode.

Table 1. Modes of Operation

FUNCTION	MODE†							
	READ	OUTPUT DISABLE	STANDBY	PROGRAMMING	VERIFY	PROGRAM INHIBIT	SIGNATURE MODE	
$\overline{E}$	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	
$\overline{G}$	V_{IL}	V_{IH}	X	V_{IH}	V_{IL}	X	V_{IL}	
$\overline{PGM}$	X	X	X	V_{IL}	V_{IH}	X	X	
V_{PP}	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}	
V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9	X	X	X	X	X	X	V_H‡	V_H‡
A0	X	X	X	X	X	X	V_{IL}	V_{IH}
DQ0–DQ7	Data Out	Hi-Z	Hi-Z	Data In	Data Out	Hi-Z	CODE	
							MFG	DEVICE
							97	D6

† X can be V_{IL} or V_{IH}.
‡ V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more SMJ27C010As are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from competing outputs of the other devices. To read the output of a single device, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins.

latchup immunity

Latchup immunity on the SMJ27C010A is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the printed circuit board level when the devices are interfaced to industry-standard TTL or MOS logic devices. The input/output layout approach controls latchup without compromising performance or packing density.

power down

Active I_{CC} supply current can be reduced from 30 mA to 500 µA by applying a high TTL input on $\overline{E}$ and to 100 µA by applying a high CMOS input on $\overline{E}$. In this mode all outputs are in the high-impedance state.

erasure

Before programming, the SMJ27C010A EPROM is erased by exposing the chip through the transparent lid to a high-intensity ultraviolet light (wavelength 2537 Å). The recommended minimum exposure dose (UV intensity × exposure time) is 15 W·s/cm^2. A typical 12-mW/cm^2, filterless UV lamp erases the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure; therefore, when using the SMJ27C010A, the window should be covered with an opaque label. After erasure (all bits in a logic-high state), logic lows are programmed into the desired locations. A programmed low can be erased only by ultraviolet light.

SNAP! Pulse programming

The SMJ27C010A is programmed using the TI SNAP! Pulse programming algorithm as illustrated by the flowchart in Figure 1. This algorithm programs in a nominal time of thirteen seconds. Actual programming time varies as a function of the programmer used.

The SNAP! Pulse programming algorithm uses an initial pulse of 100 microseconds (µs) followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to ten 100-µs pulses per byte are provided before a failure is recognized.

The programming mode is achieved when V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{E}$ = V_{IL}, and $\overline{G}$ = V_{IH}. Data is presented in parallel (eight bits) on pins DQ0 through DQ7. Once addresses and data are stable, $\overline{PGM}$ is pulsed low.

More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with V_{CC} = V_{PP} = 5 V ± 10%.

program inhibit

Programming can be inhibited by maintaining a high-level input on the $\overline{E}$ pin or the $\overline{PGM}$ pin.

program verify

Programmed bits can be verified with V_{PP} = 13 V when $\overline{G}$ = V_{IL}, $\overline{E}$ = V_{IL}, and $\overline{PGM}$ = V_{IH}.

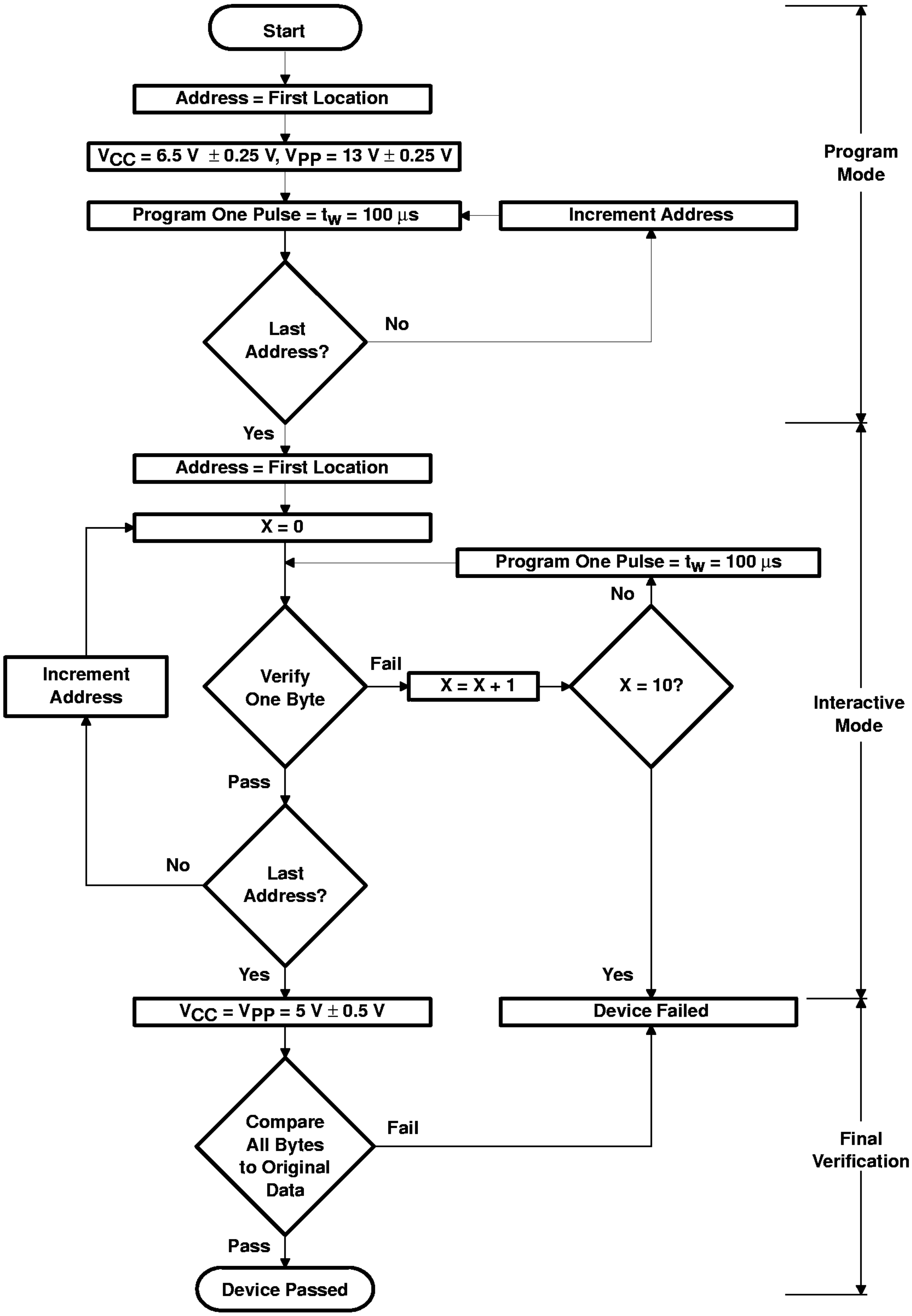


Figure 1. SNAP! Pulse Programming Flow Chart

signature mode

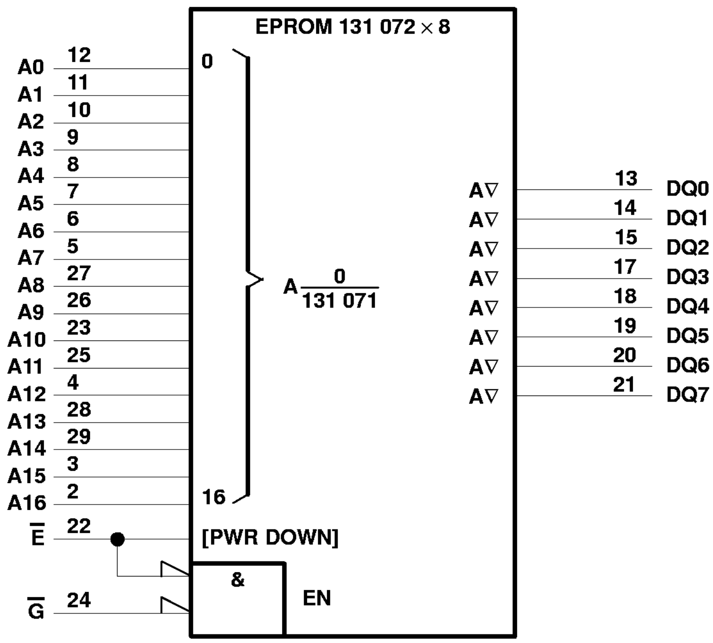
The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 26) is forced to 12 V. Two identifier bytes are accessed by toggling A0. All addresses must be held low. The signature code for these devices is 97D6. A0 low selects the manufacturer's code 97 (Hex), and A0 high selects the device code D6 (Hex), as shown in Table 2.

Table 2. Signature Mode

IDENTIFIER†	PINS									
	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	HEX
MANUFACTURER CODE	V_{IL}	1	0	0	1	0	1	1	1	97
DEVICE CODE	V_{IH}	1	1	0	1	0	1	1	0	D6

† $\overline{E} = \overline{G} = V_{IL}$, A1–A8 = V_{IL}, A9 = V_H, A10–A16 = V_{IL}, $V_{PP} = V_{CC}$

logic symbol‡



‡ This symbol is in accordance with ANSI / IEEE Std 91-1984 and IEC Publication 617-12. J package illustrated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.6 V to 7 V
Supply voltage range, V_{PP} . . . . . −0.6 V to 14 V
Input voltage range, All inputs except A9 . . . . . −0.6 V to V_{CC} + 1 V
A9 . . . . . −0.6 V to 13.5 V
Output voltage range, with respect to V_{SS} (see Note 1) . . . . . −0.6 V to V_{CC} + 1 V
Operating free-air temperature range, T_A . . . . . −55°C to 125°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

				'27C010A-12 '27C010A-15 '27C010A-20			UNIT
				MIN	NOM	MAX	
V_{CC}	Supply voltage	Read mode (see Note 2)		4.5	5	5.5	V
		SNAP! Pulse programming algorithm		6.25	6.5	6.75	V
V_{PP}	Supply voltage	Read mode (see Note 3)		V_{CC}−0.6	V_{CC}	V_{CC}+0.6	V
		SNAP! Pulse programming algorithm		12.75	13	13.25	V
V_{IH}	High-level dc input voltage		TTL	2		V_{CC}+0.5	V
			CMOS	V_{CC}−0.2		V_{CC}+0.5	
V_{IL}	Low-level dc input voltage		TTL	– 0.5		0.8	V
			CMOS	– 0.5		GND+0.2	
T_A	Operating free-air temperature			– 55		125	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.
3. During programming, V_{PP} must be maintained at 13 V ± 0.25 V.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level dc output voltage		I_{OH} = – 20 µA	V_{CC} – 0.2		V
			I_{OH} = –2.5 mA	3.5		
V_{OL}	Low-level dc output voltage		I_{OL} = 2.1 mA		0.4	V
			I_{OL} = 20 µA		0.1	
I_I	Input current (leakage)		V_I = 0 V to 5.5 V		±1	µA
I_O	Output current (leakage)		V_O = 0 V to V_{CC}		±1	µA
I_{PP1}	V_{PP} supply current		V_{PP} = V_{CC} = 5.5 V		10	µA
I_{PP2}	V_{PP} supply current (during program pulse)		V_{PP} = 13 V		50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}		500	µA
		CMOS-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC} ± 0.2 V		100	
I_{CC2}	V_{CC} supply current (active) (output open)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL} t_{cycle} = minimum cycle time,† outputs open		30	mA

† Minimum cycle time = maximum access time

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz‡

PARAMETER		TEST CONDITIONS	MIN	TYP§	MAX	UNIT
C_I	Input capacitance	V_I = 0 V, f = 1 MHz		4	8	pF
C_O	Output capacitance	V_O = 0 V, f = 1 MHz		6	10	pF

‡ Capacitance measurements are made on sample basis only.
§ All typical values are at T_A = 25°C and nominal voltages.

switching characteristics over recommended ranges of operating conditions (see Notes 4 and 5)

PARAMETER		TEST CONDITIONS	’27C010A-12		’27C010A-15		’27C010A-20		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL load, Input $t_r \le$ 20 ns, Input $t_f \le$ 20 ns		120		150		200	ns
$t_{a(E)}$	Access time from chip enable			120		150		200	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			55		75		75	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first¶		0	50	0	60	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first¶		0		0		0		ns

¶ Value calculated from 0.5-V delta to measured output level.

NOTES: 4. For all switching characteristics, the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low (reference AC testing waveform).
5. Common test conditions apply for t_{dis} except during programming.

switching characteristics for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C (see Note 4)

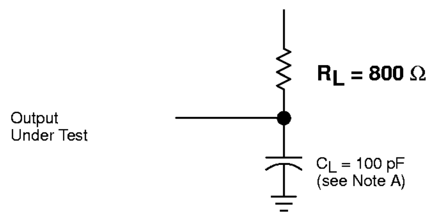
PARAMETER		MIN	MAX	UNIT
$t_{dis(G)}$	Disable time, output disable time from $\overline{G}$	0	130	ns
$t_{en(G)}$	Enable time, output enable time from $\overline{G}$		150	ns

NOTE 4: For all switching characteristics, the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low (reference AC testing waveform).

timing requirements for programming

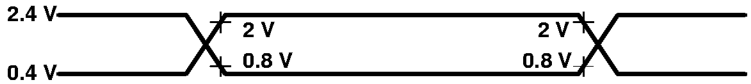
			MIN	TYP	MAX	UNIT
$t_{w(PGM)}$	Pulse duration, program	SNAP! Pulse programming algorithm	95	100	105	µs
$t_{su(A)}$	Setup time, address		2			µs
$t_{su(E)}$	Setup time, $\overline{E}$		2			µs
$t_{su(G)}$	Setup time, $\overline{G}$		2			µs
$t_{su(D)}$	Setup time, data		2			µs
$t_{su(VPP)}$	Setup time, V_{PP}		2			µs
$t_{su(VCC)}$	Setup time, V_{CC}		2			µs
$t_{h(A)}$	Hold time, address		0			µs
$t_{h(D)}$	Hold time, data		2			µs

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and fixture capacitance.

ac testing input/output waveforms



AC testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

Figure 2. AC Test Output Load Circuit

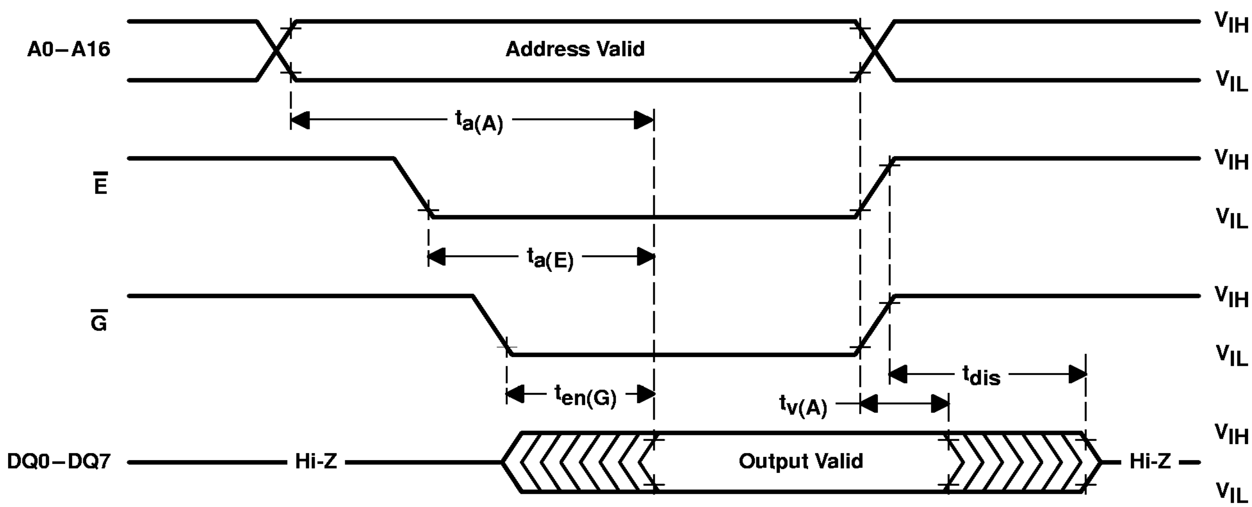
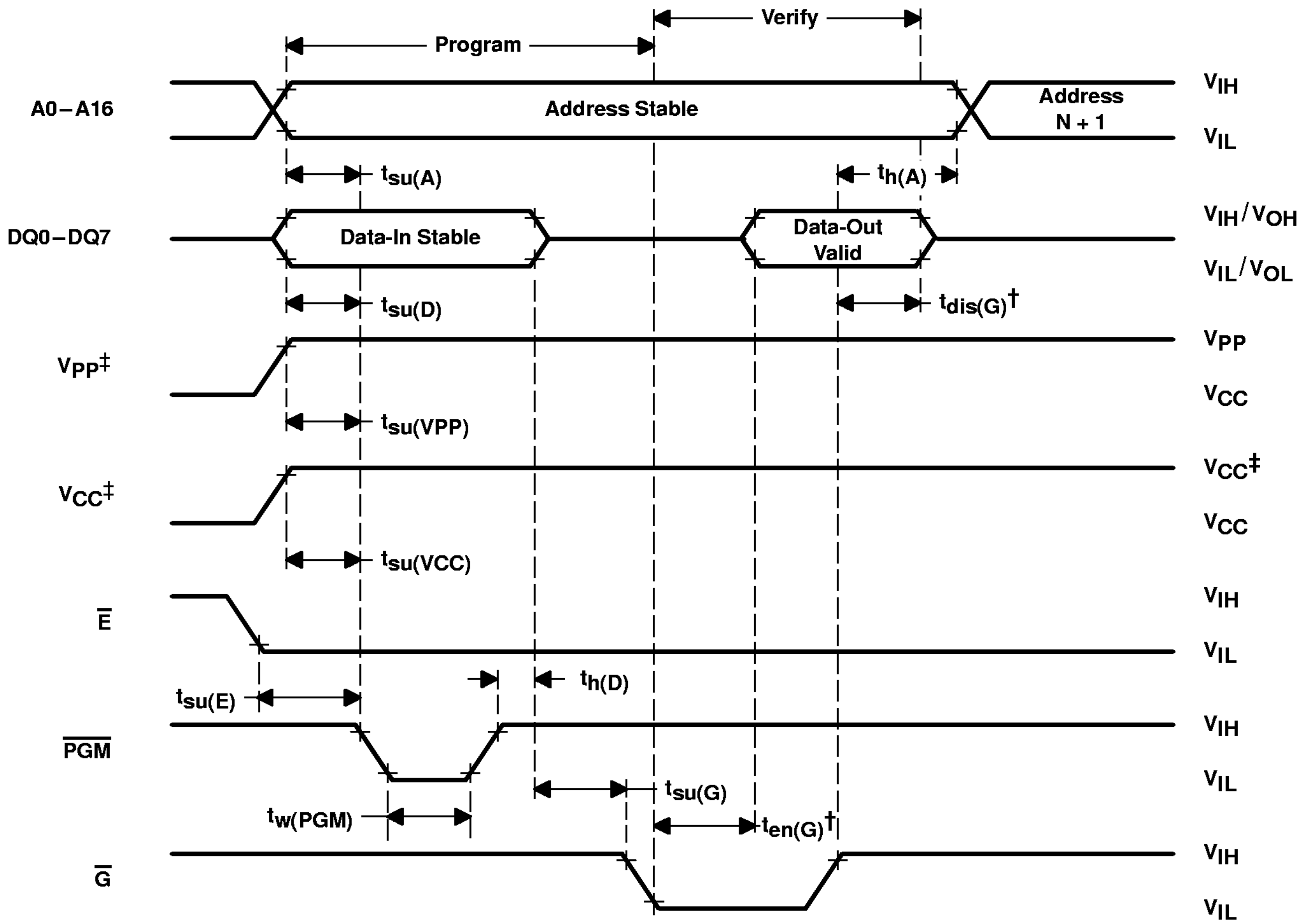


Figure 3. Read-Cycle Timing

PROGRAMMING INFORMATION



† $t_{dis(G)}$ and $t_{en(G)}$ are characteristics of the device but must be accommodated by the programmer.
‡ 13-V V_{PP} and 6.5-V V_{CC} for SNAP! Pulse programming.

Figure 4. Program-Cycle Timing (SNAP! Pulse Programming)

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