LH21256

NMOS 256K (256K × 1) Dynamic RAM

FEATURES

- 262,144 × 1 bit organization
- Access times: 100/120/150 ns (MAX.)
- Cycle times: 200/230/260 ns (MIN.)
- Page mode operation
- Power supply: +5 V ± 10%
- Power consumption:
  Operating: 467.5/440/385 mW (MAX.)
  Standby: 27.5 mW (MAX.)
- TTL compatible I/O
- Built-in gated $\overline{CAS}$ function
- Separate I/O allows Early-Write action
- Available for read modify write, $\overline{RAS}$ only refresh, hidden refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh
- 256 refresh cycle (refreshing time 4 ms)
- Built-in high output bias generator circuit
- Packages:
  16-pin, 300-mil DIP
  16-pin, 325-mil ZIP

DESCRIPTION

The LH21256 is a 262,144 word × 1 bit dynamic RAM fabricated using N-channel 2-layer polysilicon gate process technology. With mulitiplexed address inputs and standard 16-pin DIP/ZIP packages, it is easy to comprise memory systems with high speed, low power consumption and large memory capacity. The LH21256 operates on a single +5 V power supply. The built-in high output substrate bias generator circuit eliminates sensitivity to undershoot on the input signals.

PIN CONNECTIONS

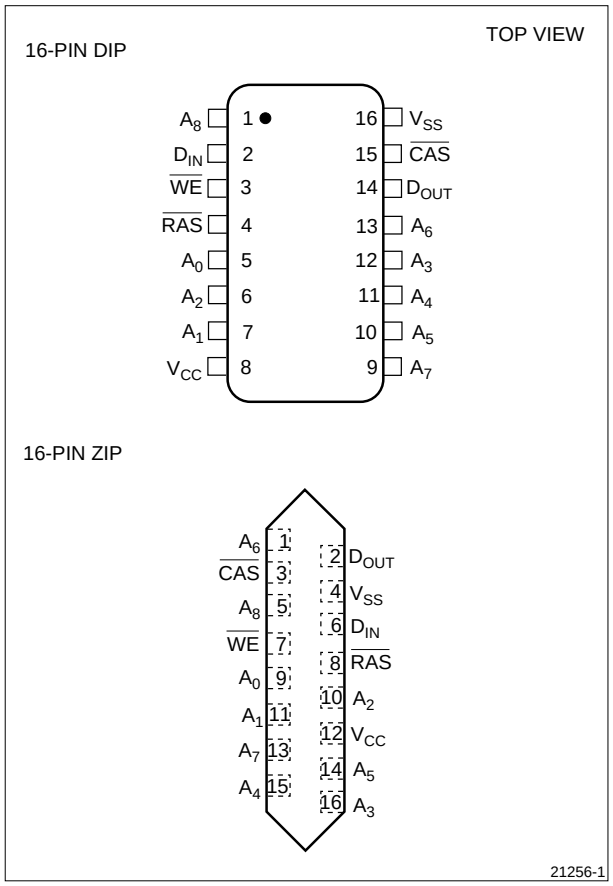


Figure 1. Pin Connections for DIP and ZIP Packages

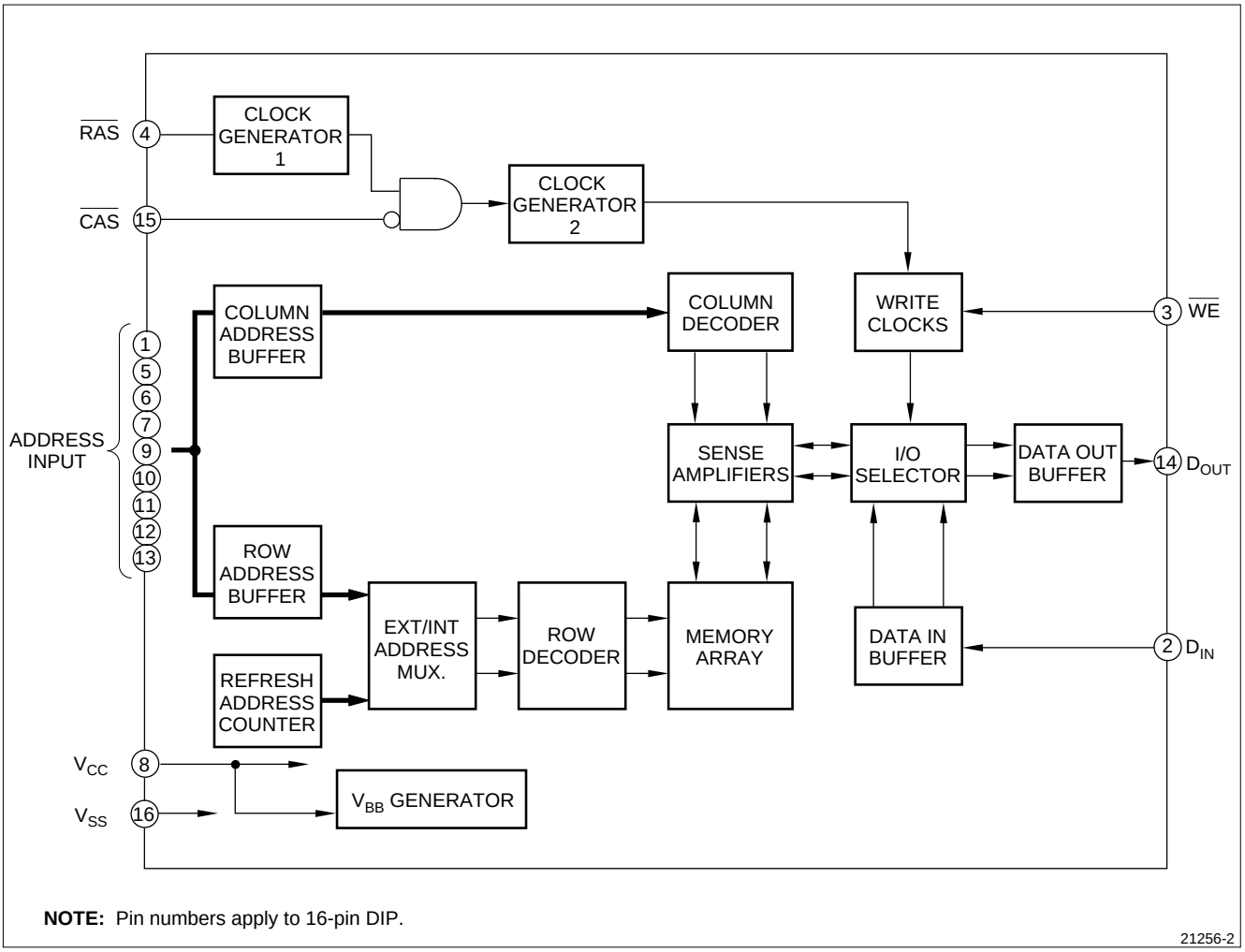


Figure 2. LH21256 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_8	Address input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable

SIGNAL	PIN NAME
D_{IN}	Data input
D_{OUT}	Data output
V_{CC}	Power supply (+5 V)
V_{SS}	Power supply (0 V)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_T	-1.0 to 7.0	V	1
Output short-circuit current	I_O	50	mA	
Power consumption	P_D	1.0	W	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. Referenced to V_{SS}

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Input voltage	V_{IH}	2.4		6.5	V	1
	V_{IL}	-1.0		0.8		

NOTE:
1. Referenced to V_{SS}

CAPACITANCE (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C, f = 1MHz)

PARAMETER		SYMBOL	MIN.	TYPICAL	MAX.	UNIT
Input capacitance	A_0 - A_8, D_{IN}, $\overline{WE}$	C_{IN1}			7	pF
	$\overline{RAS}$, $\overline{CAS}$	C_{IN2}			10	pF
Output capacitance	D_{OUT}	C_{OUT}			8	pF

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER		SYMBOL	MIN.	MAX.	UNIT	NOTE
Average supply current in normal operation	LH21256-10	I_{CC1}	—	85	mA	1, 2
	LH21256-12		—	80		
	LH21256-15		—	70		
Average supply current in standby mode		I_{CC2}	—	5.0	mA	1
Average supply current in $\overline{RAS}$ only refresh time	LH21256-10	I_{CC3}	—	65	mA	1, 2
	LH21256-12		—	60		
	LH21256-15		—	55		
Average supply current in page mode	LH21256-10	I_{CC4}	—	50	mA	1, 2
	LH21256-12		—	45		
	LH21256-15		—	40		
$\overline{CAS}$ before $\overline{RAS}$ average supply current in refresh cycle	LH21256-10	I_{CC5}	—	65	mA	1, 2
	LH21256-12		—	60		
	LH21256-15		—	55		
Input leakage current	0 V ≤ V_{IN} ≤ 6.5 V 0 V on all other pins	$I_{I(L)}$	-10	10	µA	
Output leakage current	0 V ≤ V_{OUT} ≤ 6.5 V Output in high-impedance state	$I_{O(L)}$	-10	10	µA	
Output 'High' voltage	I_{OUT} = -5 mA	V_{OH}	2.4	—	V	
Output 'Low' voltage	I_{OUT} = 4.2 mA	V_{OL}	—	0.4	V	

NOTES:
1. The output pins are in high-impedance state.
2. I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on the cycle time.

AC CHARACTERISTICS[1, 2, 3] (V_{CC} = 5 V ± 10%, T_A = 0 to 70°C)

PARAMETER	SYMBOL	LH21256-10		LH21256-12		LH21256-15		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Random read/write cycle time	t_{RC}	200	—	230	—	260	—	ns	
Read write cycle time	t_{RWC}	240	—	275	—	310	—	ns	
Access time from $\overline{RAS}$	t_{RAC}	—	100	—	120	—	150	ns	4, 6
Access time from $\overline{CAS}$	t_{CAC}	—	50	—	60	—	75	ns	5, 6
Output turn-off delay time	t_{OFF}	0	30	0	35	0	40	ns	
Rise and fall time	t_T	3	35	3	35	3	35	ns	3
$\overline{RAS}$ precharge time	t_{RP}	90	—	100	—	100	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	50	—	60	—	75	—	ns	
$\overline{CAS}$ precharge time	t_{CPN}	25	—	30	—	35	—	ns	
$\overline{CAS}$ pulse width	t_{CAS}	50	10,000	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	100	—	120	—	150	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{FCH}	100	—	120	—	150	—	ns	
$\overline{CAS}$ set up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{FCS}	20	—	25	—	30	—	ns	
$\overline{RAS}$/$\overline{CAS}$ delay time	t_{RCD}	20	50	25	60	30	75	ns	7, 8
$\overline{CAS}$/$\overline{RAS}$ precharge time	t_{CRP}	20	—	25	—	30	—	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	15	—	20	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	25	—	25	—	45	—	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	75	—	95	—	120	—	ns	
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	0	—	ns	11
Read command hold time from $\overline{RAS}$	t_{RRH}	20	—	20	—	20	—	ns	11
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	10
Write command hold time	t_{WCH}	35	—	40	—	45	—	ns	
Write command hold time from $\overline{RAS}$	t_{WCR}	85	—	100	—	120	—	ns	
Write command pulse width	t_{WP}	35	—	40	—	45	—	ns	
Write command $\overline{RAS}$ lead time	t_{RWL}	35	—	40	—	45	—	ns	
Write command $\overline{CAS}$ lead time	t_{CWL}	35	—	40	—	45	—	ns	
$\overline{RAS}$ write command delay time	t_{RWD}	95	—	120	—	150	—	ns	
$\overline{CAS}$ write command delay time	t_{CWD}	45	—	60	—	75	—	ns	
Data input setup time	t_{DS}	0	—	0	—	0	—	ns	9
Data input hold time	t_{DH}	30	—	30	—	35	—	ns	9
Data input hold time from $\overline{RAS}$	t_{DHR}	80	—	90	—	110	—	ns	
Refresh time	t_{REF}	—	4	—	4	—	4	ms	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0	—	0	—	0	—	ns	

NOTES:

1. For proper operation, at least 500 µs of pause time after power-on followed by several initialization cycles (usually 8 ordinary refresh cycles) should be given.
2. AC characteristics assume t_T = 5 ns.
3. Timing measurements are referenced to V_{IH} (MIN.) and V_{IL} (MAX.). (t_T refers to the transition time between V_{IH} and V_{IL}.)
4. Only when $t_{RCD} \leq t_{RCD}$ (MAX.). If $t_{RCD} > t_{RCD}$ (MAX.), t_{RAC} will increase by (t_{RCD} - t_{RCD} (MAX.))
5. When $t_{RCD} \geq t_{RCD}$ (MAX.).
6. Load condition for 2TTL + 100 pF.
7. t_{RCD} (MAX.) is the maximum point for t_{RCD} where t_{RAC} (MAX.) is ensured, and does not represent a limit of operation. If t_{RCD} (MAX.) ≤ t_{RCD}, the access time is controlled by t_{CAC}.
8. t_{RCD} (MIN.) = t_{RAH} (MIN.) + 2t_T + t_{ASC} (MIN.).
9. t_{DS} and t_{DH} are given with respect to the fall of $\overline{CAS}$ in the Early-Write cycle and the fall of $\overline{WE}$ in the read/write cycle and the Read-Modify-Write cycle.
10. t_{WCS}, t_{CWD} and t_{RWD} are the specified points of the operating mode, and do not represent a limit of operation. When $t_{WCS} \geq t_{WCS}$ (MIN.), it comes into early write cycle with D_{OUT} pin coming into high-impedance state. When $t_{CWD} \geq t_{CWD}$ (MIN.) and $t_{RWD} \geq t_{RWD}$ (MIN.), it comes into the read/write cycle with the output data becoming the information for the selection cell. Timing other than the above-mentions will give undefined value of output.
11. The operation is ensured when either t_{RCH} or t_{RRH} is satisfied.

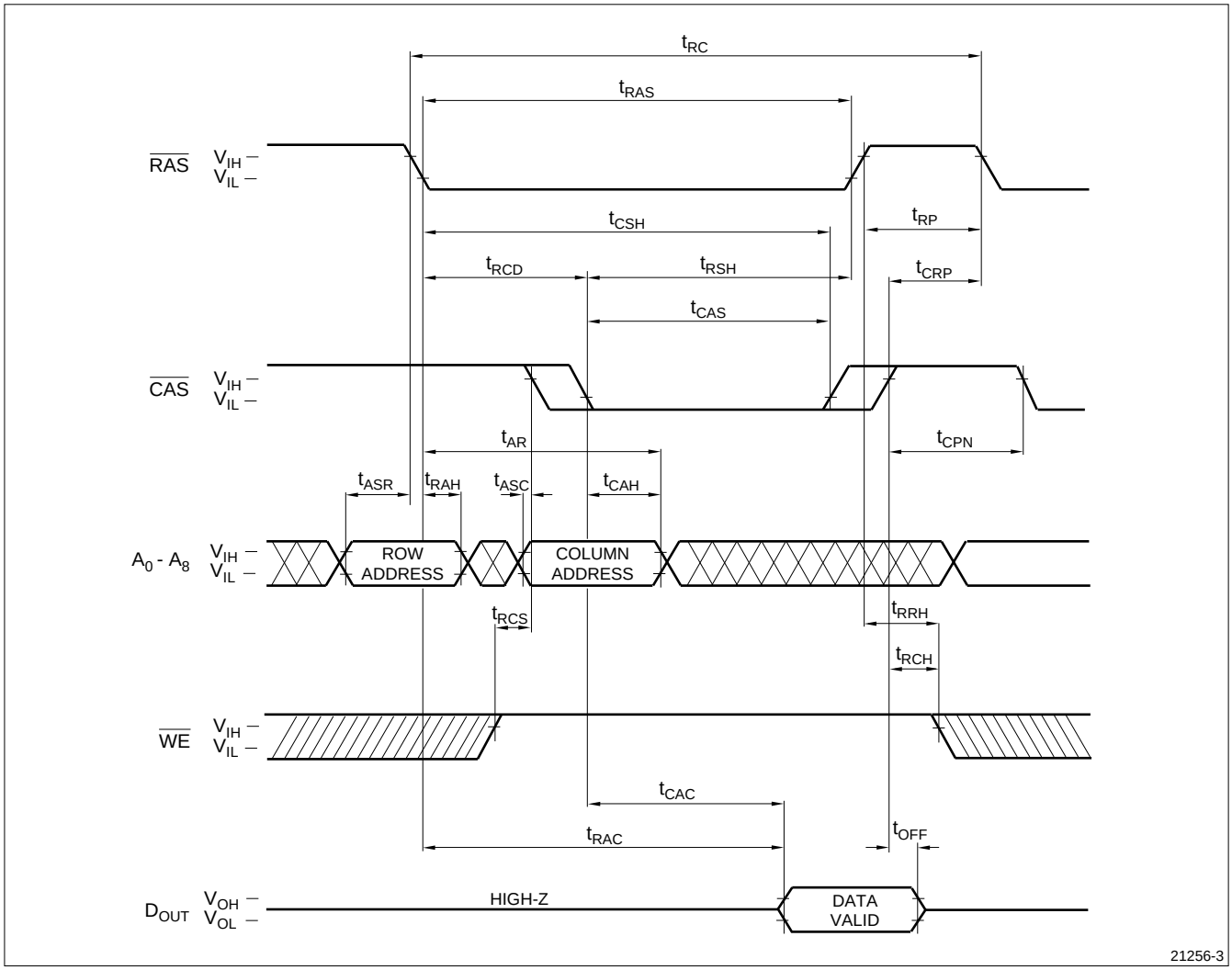


Figure 3. Read Cycle

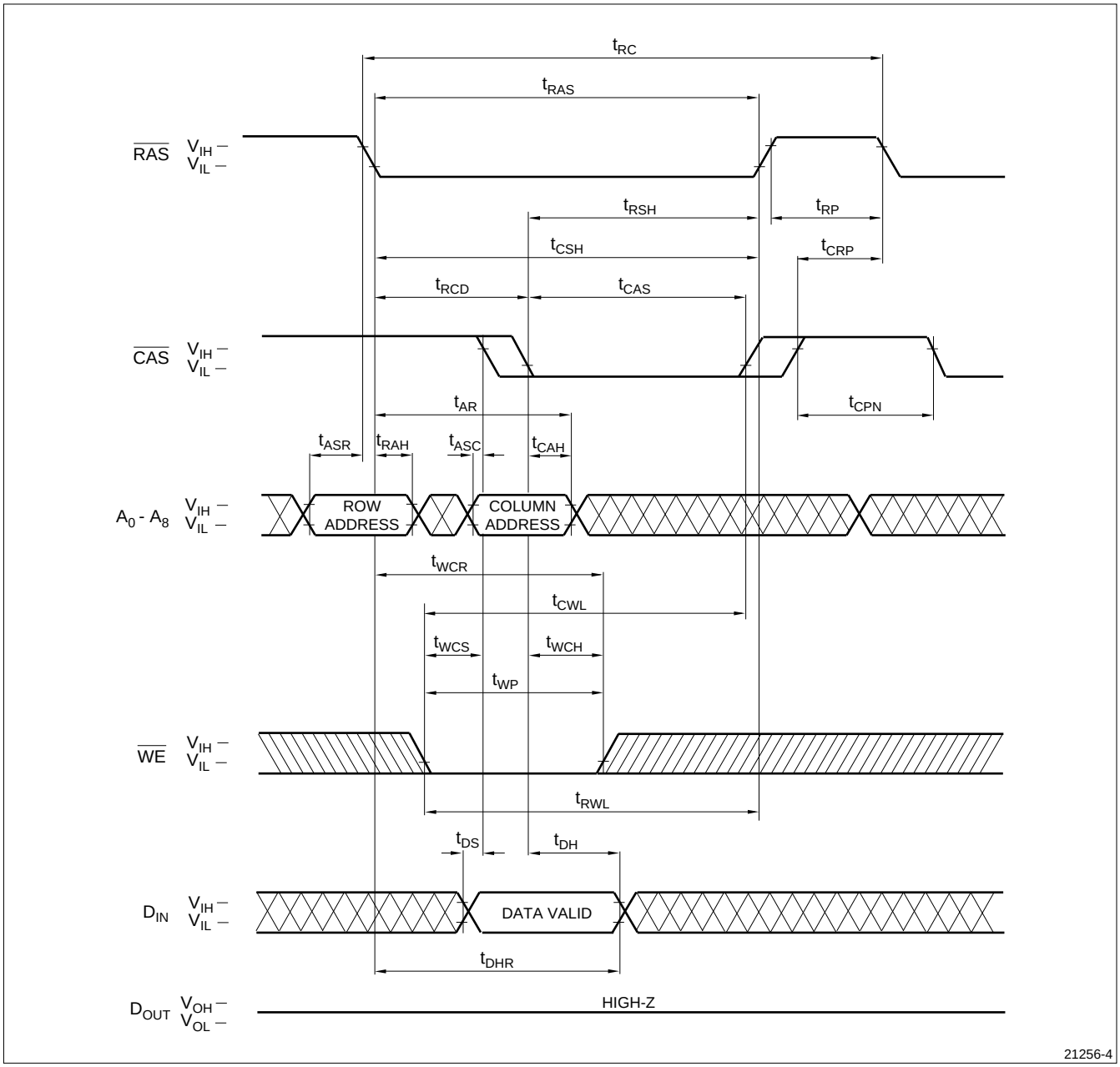


Figure 4. Write Cycle (Early Write)

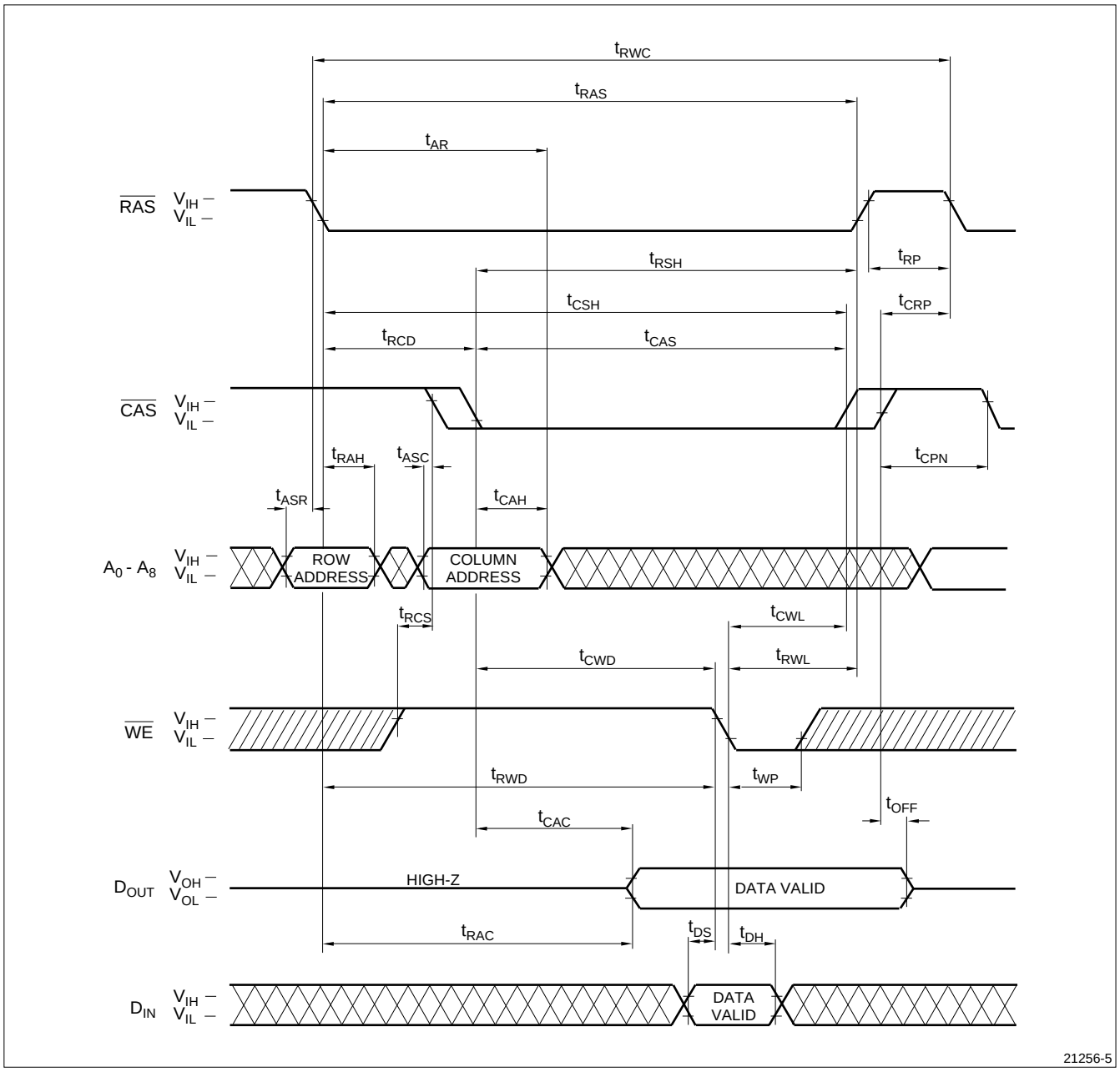


Figure 5. Read-Write/Read-Modify-Write Cycle

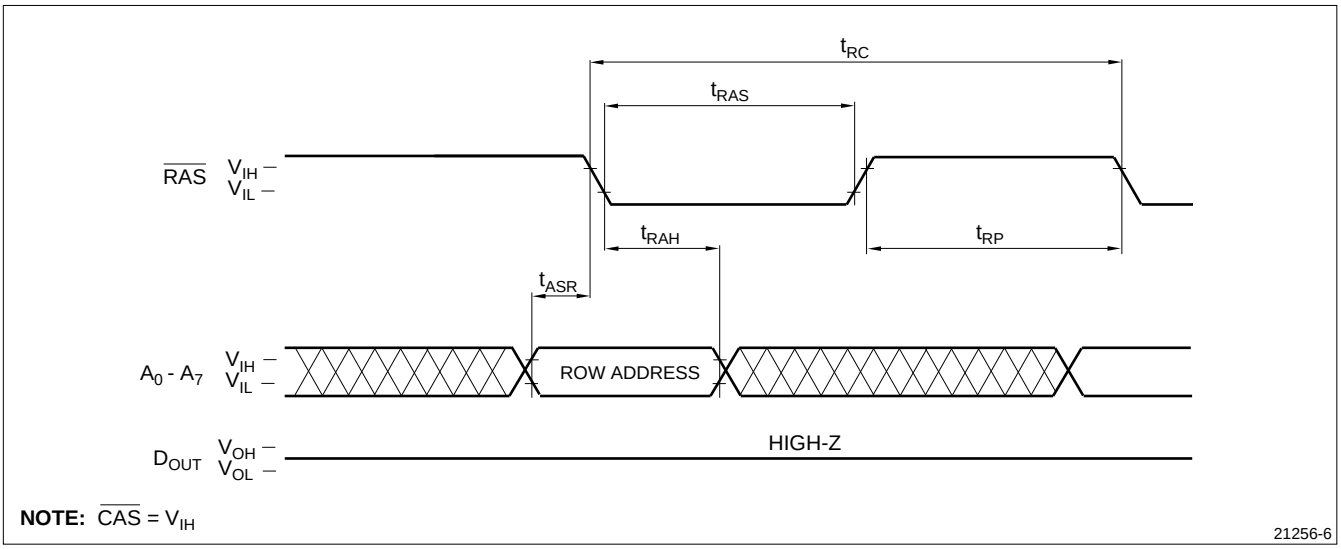


Figure 6. $\overline{RAS}$ Only Refresh Cycle

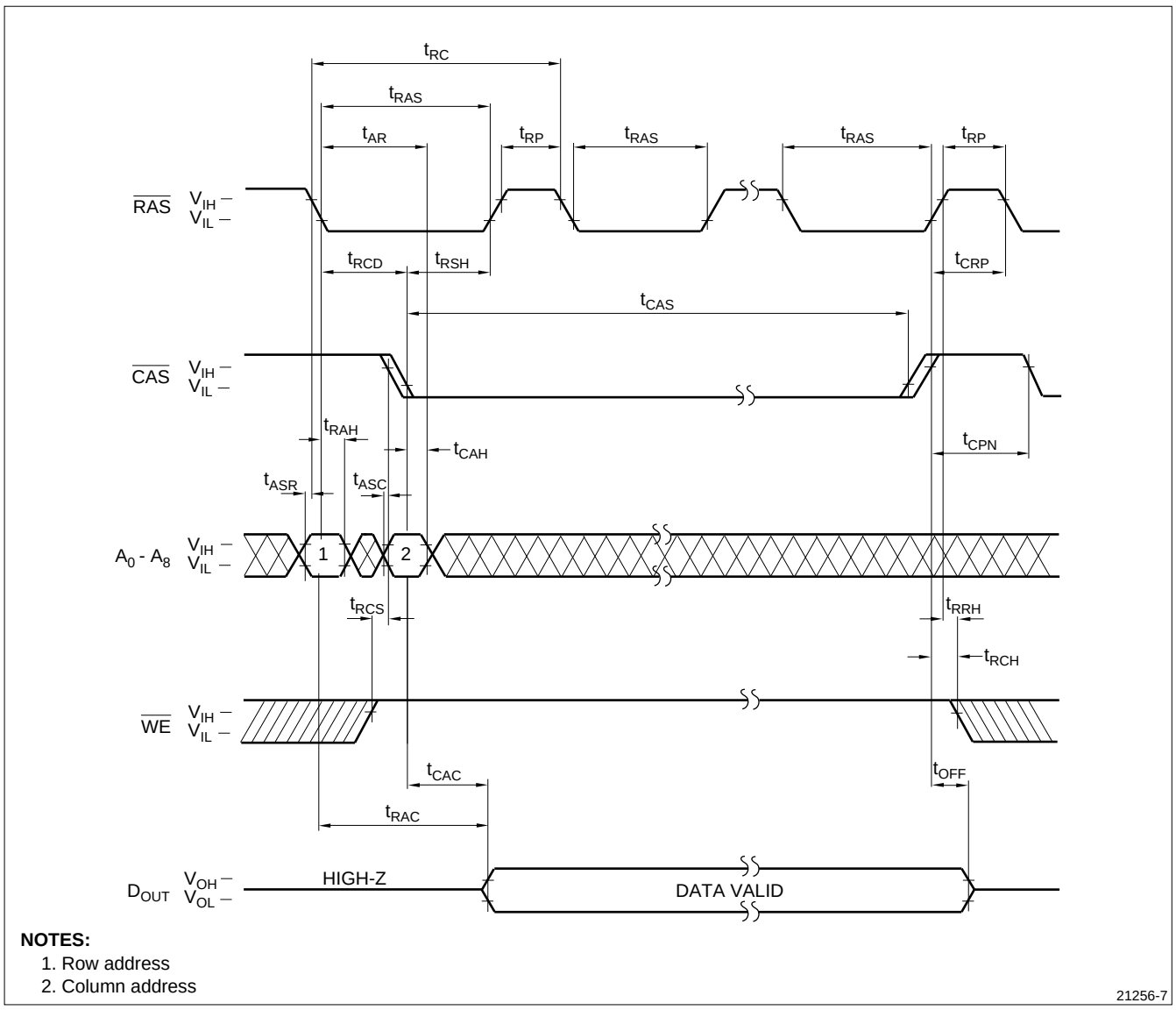


Figure 7. Hidden Refresh Cycle

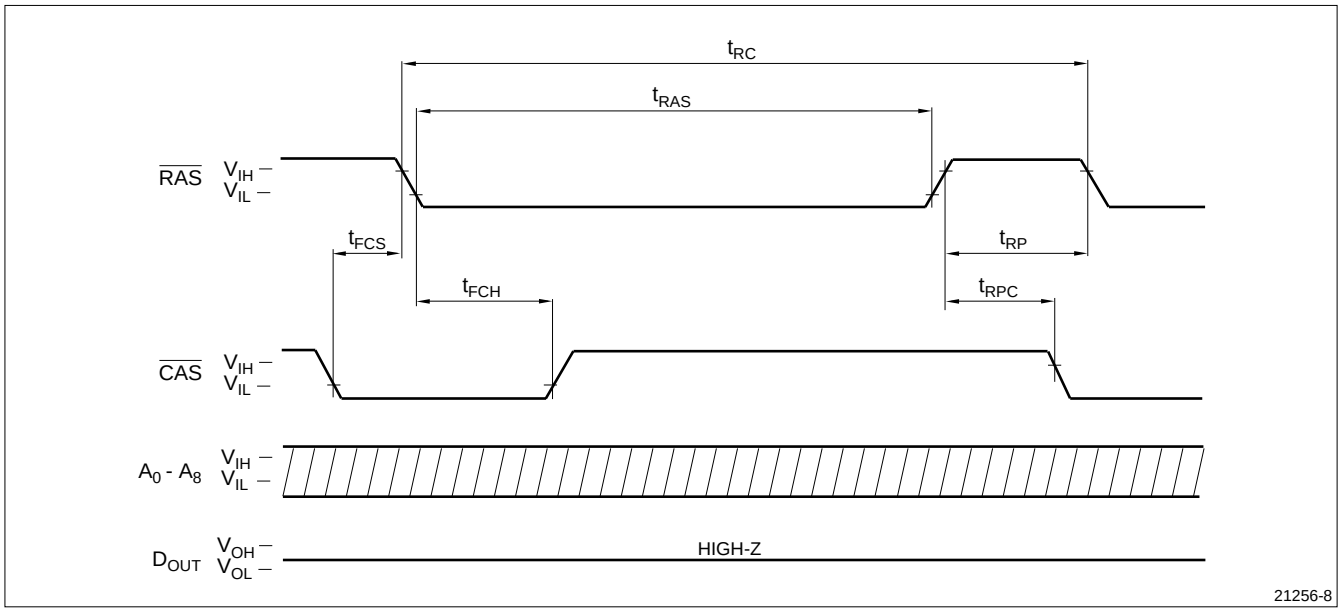
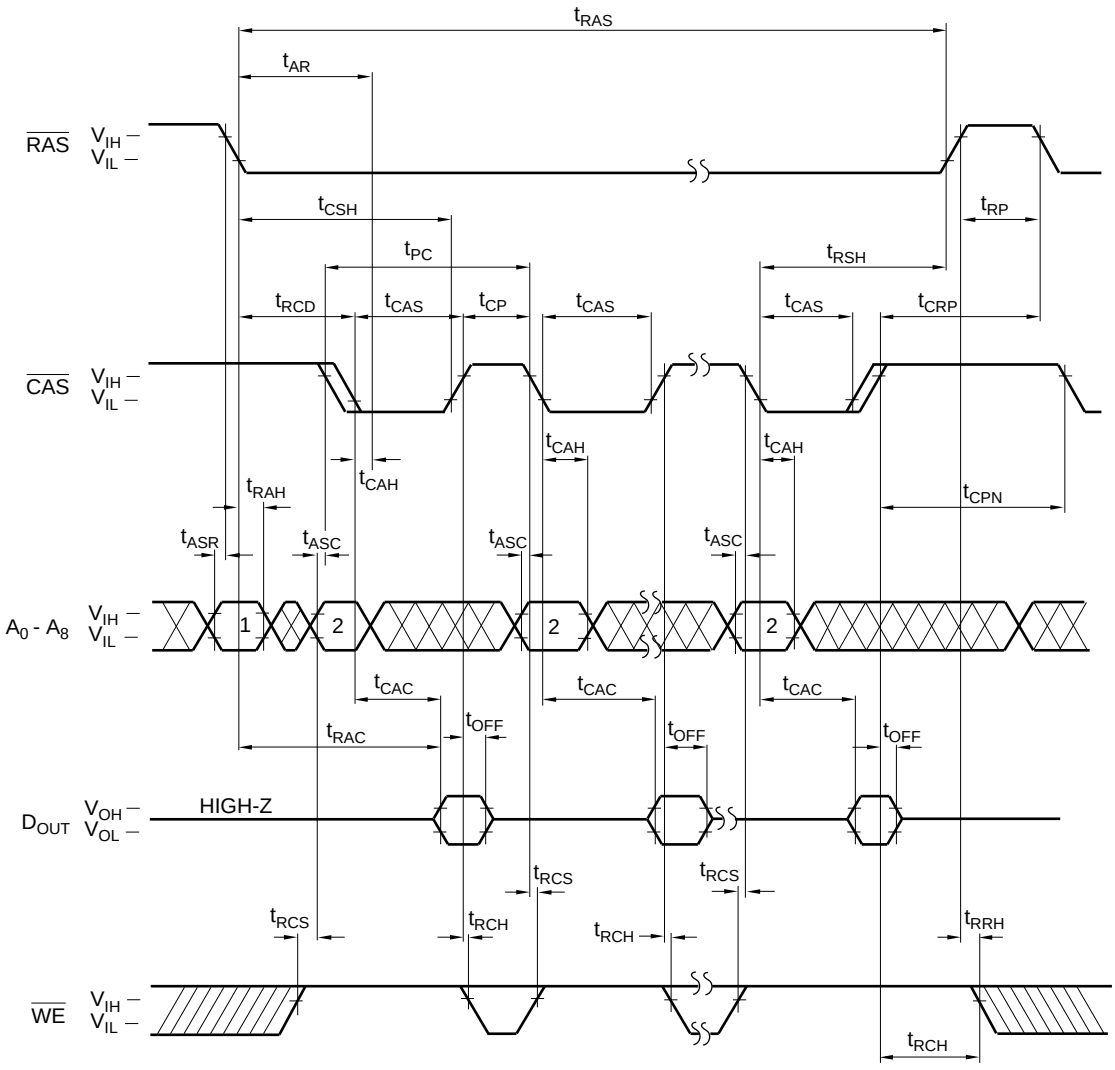


Figure 8. $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

PAGE MODE CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

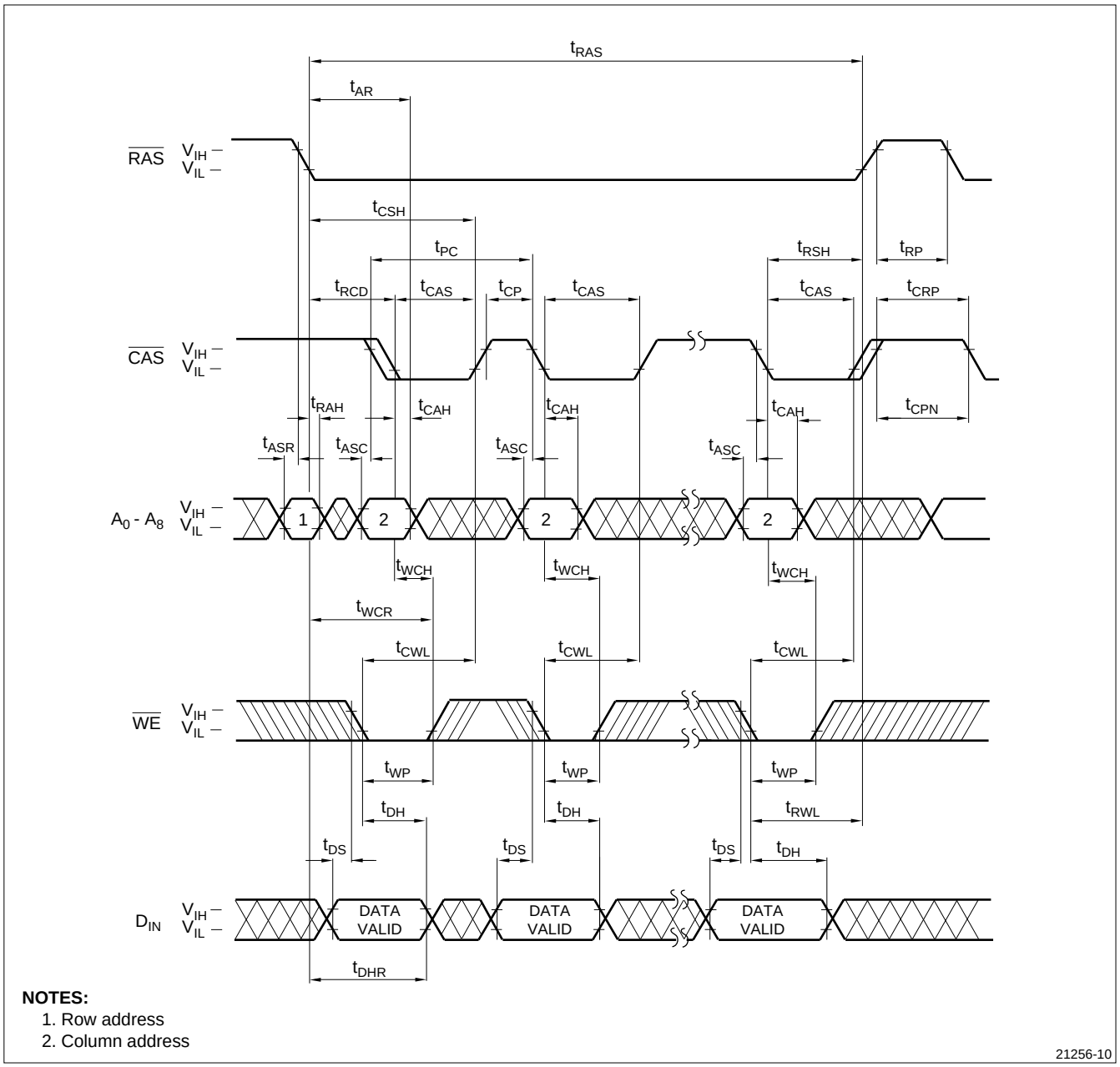
PARAMETER	SYMBOL	LH21256-10		LH21256-12		LH21256-15		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Page mode cycle time	t_{PC}	100	—	120	—	145	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	40	—	50	—	60	—	ns	



NOTES:
1. Row address
2. Column address

21256-9

Figure 9. Page Mode Read Cycle

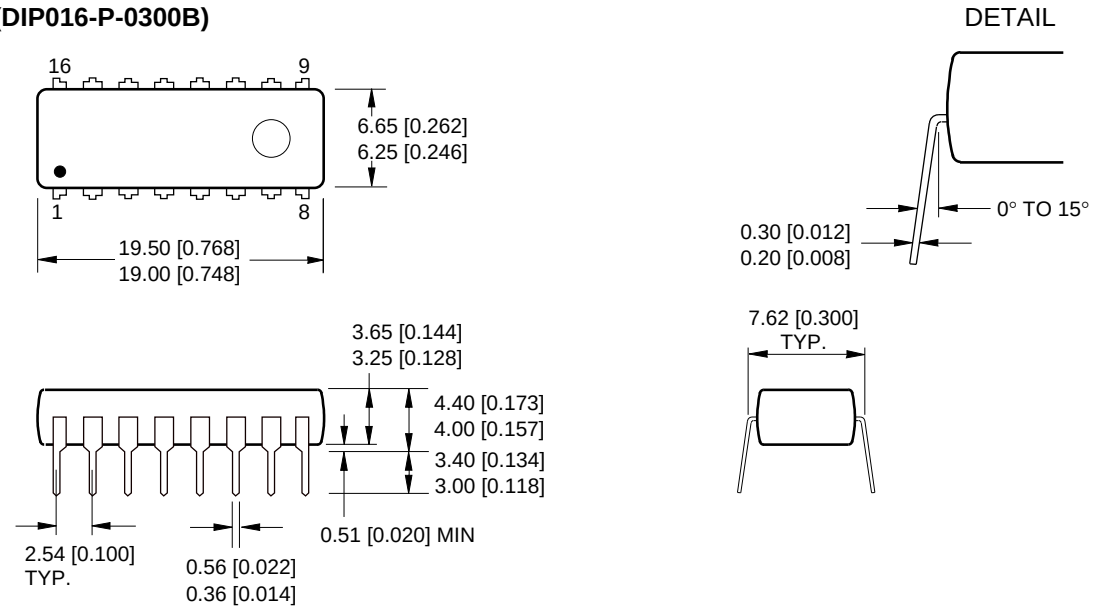


NOTES:
1. Row address
2. Column address

Figure 10. Page Mode Write Cycle

PACKAGE DIAGRAMS

16DIP (DIP016-P-0300B)

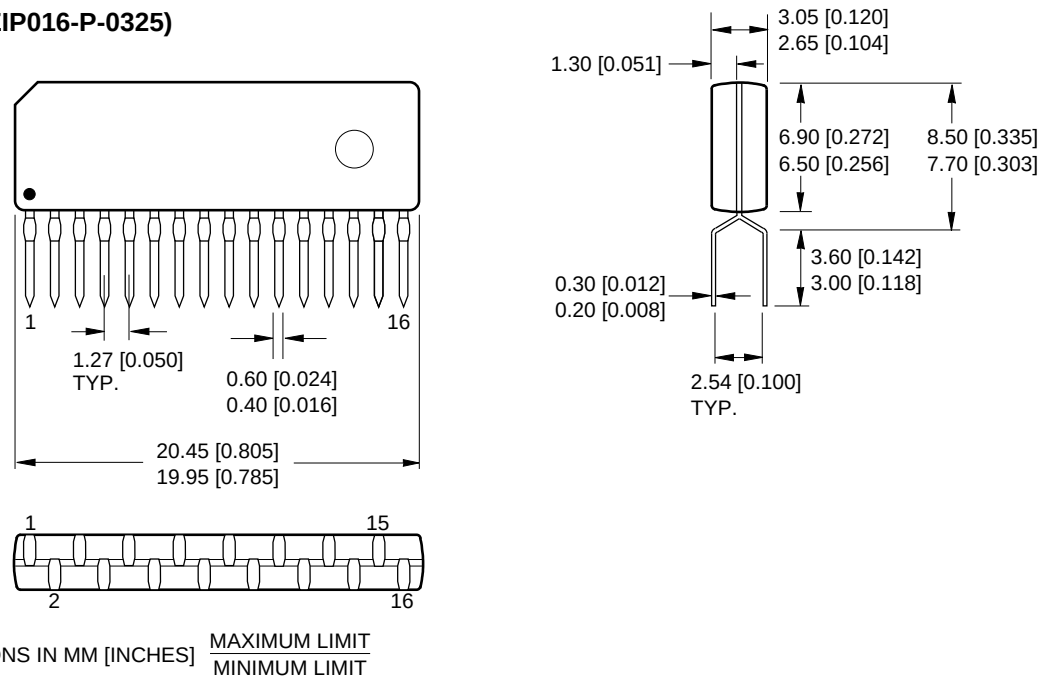


DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

16DIP

16-pin, 300-mil DIP

16ZIP (ZIP016-P-0325)

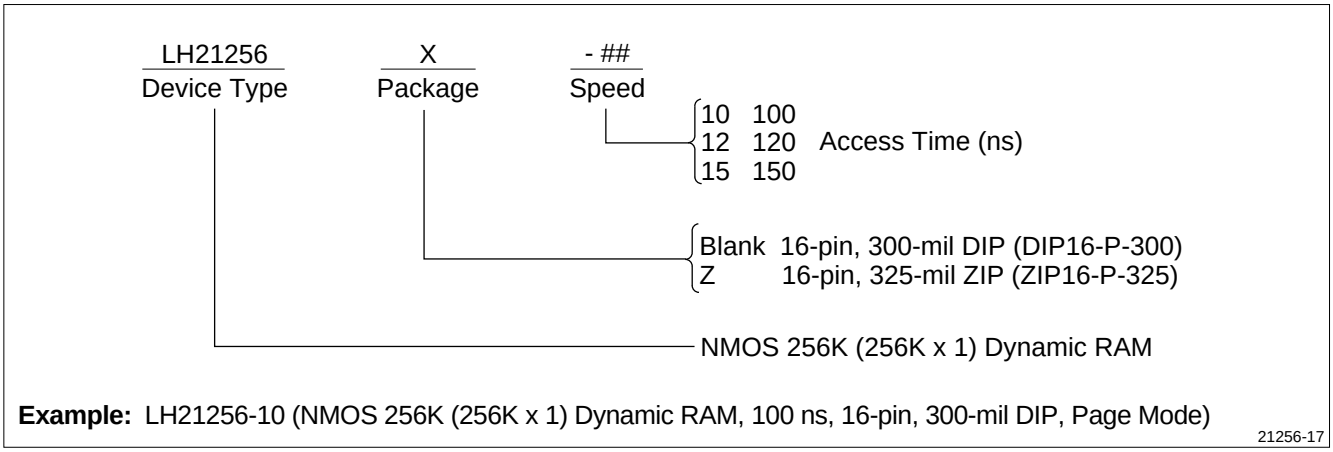


DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

16ZIP

16-pin, 325-mil ZIP

ORDERING INFORMATION



Example: LH21256-10 (NMOS 256K (256K x 1) Dynamic RAM, 100 ns, 16-pin, 300-mil DIP, Page Mode)

21256-17