A68C257
256K (32K x 8) CHMOS LATCHED EPROM

- **Extended Automotive Temperature Range: −40°C to +125°C**
- **6801, 6803, 68HC11 Microcomputer Compatible**
  - **— Integrated Address Latch**
  - **— Active-High Chip Enable**
  - **— Active-High Output Enable**
- **200 ns Maximum Access Time**
- **CMOS and TTL Compatible**
- **Low Power**
  - **— 30 mA Max. Active**
  - **— 100 μA Max. Standby**
- **Fast Programming**
  - **— Quick-Pulse Programming™ Algorithm**
  - **— Programming Time as Fast as 4 Seconds**
- **Noise Immunity Features**
  - **— ± 10% V_{CC} Tolerance**
  - **— Latch-up Immunity Through EPI Processing**
- **28-Pin Cerdip and 32-Lead PLCC Packages**

(See Packaging Spec., Order #231369)

Intel's 68C257 is a 256K-bit 5V-only CHMOS EPROM organized as 32,768 8-bit words. CHMOS*III-E circuitry provides high speed performance, low power, and noise immunity.

High-memory boot-up locations and active-high read strobes are characteristics of 68-family microcomputers. Address latches and inverters are required when traditional EPROMs are connected to these microcomputers. The 68C257 contains all of this circuitry in a single package for "no-glue" interfacing. Its integrated features reduce system cost, board space, power, inventory, incoming inspection, and design time and ensure performance that is superior to discrete-component alternatives.

Address inputs incorporate latches so designers can tie the 68C257's pins directly to a processor's multiplexed address/data pins. The independent ALE (Address Latch Enable) latches addresses without impacting access time. CE (Chip Enable) and OE (Output Enable) are active-high for "no-glue" interfaces to 68-family microcomputers.

The Quick-Pulse Programming™ algorithm quickly and reliably programs the 68C257 in four seconds or less.

Intel's EPI processing achieves the highest degree of latch-up protection. Address and data pins withstand stresses up to 100 mA from −1V to V_{CC} + 1V.

*HMOS and CHMOS are patented processes of Intel Corporation.

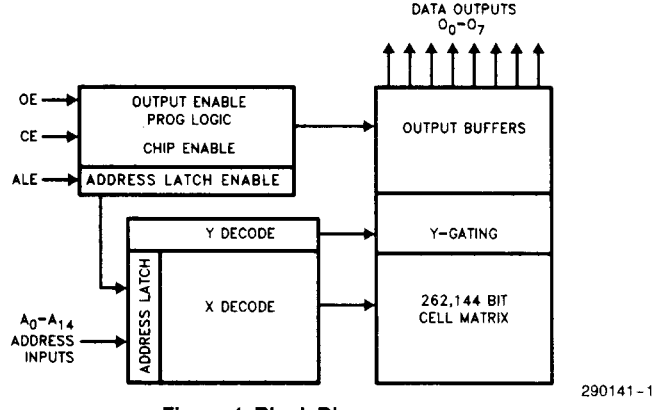


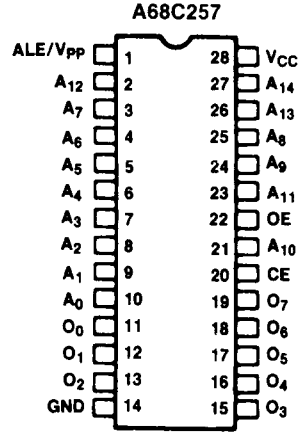
Figure 1. Block Diagram

February 1991
Order Number: 290141-003

Pin Names

A_0–A_{14}	ADDRESSES
O_0–O_7	OUTPUTS
OE, $\overline{OE}$	OUTPUT ENABLE
CE, $\overline{CE}$	CHIP ENABLE
ALE/V_{PP}	ADDRESS LATCH ENABLE/V_{PP}
N.C.	NO CONNECT
D.U.	DON'T USE

87C64	87C257
V_{PP}	ALE/V_{PP}
A_{12}	A_{12}
A_7	A_7
A_6	A_6
A_5	A_5
A_4	A_4
A_3	A_3
A_2	A_2
A_1	A_1
A_0	A_0
O_0	O_0
O_1	O_1
O_2	O_2
Gnd	Gnd



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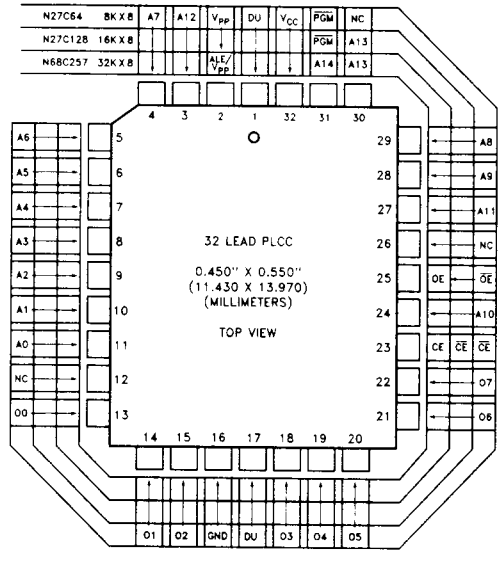
87C257	87C64
V_{CC}	V_{CC}
A_{14}	$\overline{PGM}$
A_{13}	N.C.
A_8	A_8
A_9	A_9
A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}$
A_{10}	A_{10}
$\overline{CE}$	ALE/$\overline{CE}$
O_7	O_7
O_6	O_6
O_5	O_5
O_4	O_4
O_3	O_3

Figure 2. DIP Pin Configuration

NOTE:
Intel "Universal Site"-Compatible EPROM Pin Configurations are Shown in the Blocks Adjacent.



290141-3

Figure 3. PLCC Lead Configuration

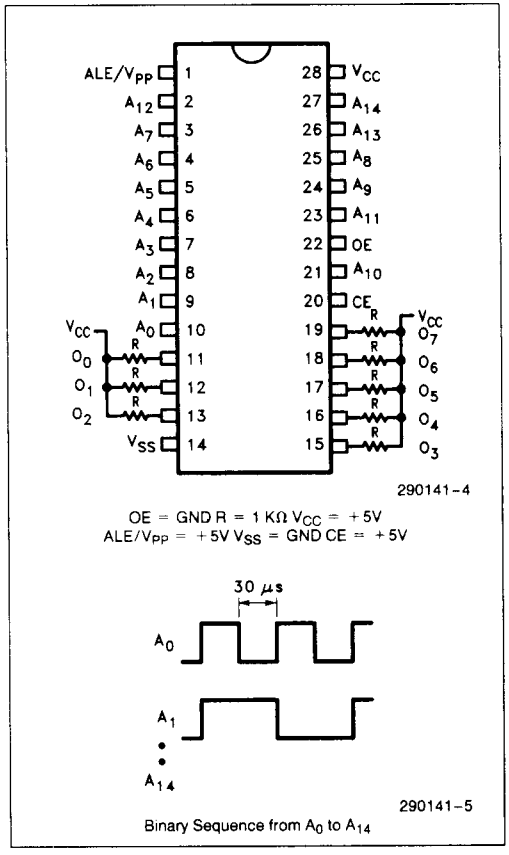
AUTOMOTIVE TEMPERATURE EPROMs

Intel Automotive EPROMs have received additional processing to enhance product characteristics. The automotive temperature range is −40°C to +125°C during operating modes.

AUTOMOTIVE OPTIONS

Versions

Speed Versions	Packaging Options	
	Cerdip	PLCC
200V10	AD	AN



Burn-In Bias and Timing Diagrams

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ABSOLUTE MAXIMUM RATINGS*

Operating Temperature During Read ..... −40°C to +125°C
Temperature Under Bias ..... −40°C to +125°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with Respect to Ground ..... −2V to +7V(1)
Voltage on A_9 with Respect to Ground ..... −2V to +13.5V(1)
V_{PP} Supply Voltage with Respect to Ground During Programming ..... −2V to +14.0V(1)
V_{CC} Supply Voltage with Respect to Ground ..... −2V to +7.0V(1)

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

READ OPERATION

DC CHARACTERISTICS TTL and NMOS Inputs, $-40°C \le T_A \le +125°C$

Symbol	Parameter		Notes	Min	Typ(2)	Max	Units	Test Condition
I_{LI}	Input Load Current				0.01	1.0	μA	V_{IN} = 0V to 5.5V
I_{LO}	Output Leakage Current					±10	μA	V_{OUT} = 0V to 5.5V
I_{SB}	V_{CC} Current Standby with Inputs—	Switching				10	mA	CE = V_{IL}, ALE = V_{IH}
		Stable				1.0	mA	CE = ALE = V_{IL}
I_{CC_1}	V_{CC} Current Active		5			30	mA	CE = ALE = V_{IH} f = 5 MHz, I_{OUT} = 0 mA
V_{IL}	Input Low Voltage (±10% Supply)		1	−0.5		0.8	V	
V_{IH}	Input High Voltage (±10% Supply)			2.0		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage					0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage			2.4			V	I_{OH} = −400 μA
I_{OS}	Output Short Circuit Current		6			100	mA	

DC CHARACTERISTICS CMOS Inputs, $-40°C \le T_A \le +125°C$

Symbol	Parameter		Notes	Min	Typ(2)	Max	Units	Test Condition
I_{LI}	Input Load Current				0.01	1.0	μA	V_{IN} = 0V to 5.5V
I_{LO}	Output Leakage Current					±10	μA	V_{OUT} = 0V to 5.5V
I_{SB}	V_{CC} Current Standby with Inputs—	Switching	4			6	mA	CE = GND, ALE = V_{CC}
		Stable				100	μA	CE = ALE = GND
I_{CC_1}	V_{CC} Current Active		5			15	mA	CE = ALE = V_{IH} f = 5 MHz, I_{OUT} = 0 mA
V_{IL}	Input Low Voltage (±10% Supply)			−0.2		0.8	V	
V_{IH}	Input High Voltage (±10% Supply)			0.7 V_{CC}		V_{CC} + 0.2	V	
V_{OL}	Output Low Voltage					0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage			V_{CC} − 0.8			V	I_{OH} = −2.5 mA
I_{OS}	Output Short Circuit Current		6			100	mA	

NOTES:
1. Minimum DC input voltage is −0.5V. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5V which may overshoot to V_{CC} + 2V for periods less than 20 ns.
2. Typical limits are at V_{CC} = 5V, T_A = +25°C.
3. CE and ALE are ±0.2V. All other inputs can have any value within spec.
4. Maximum current value is with outputs O_0 to O_7 unloaded.
5. Output shorted for no more than one second. No more than one output shorted at a time. I_{OS} is sampled but not 100% tested.

READ OPERATION

AC CHARACTERISTICS(1) $-40°C \leq T_A \leq +125°C$

Versions(3)		$V_{CC} \pm 10\%$	68C257-200V10 N68C257-200V10		Unit
Symbol	Characteristic		Min	Max	
t_{ACC}	Address to Output Delay			200	ns
t_{CE}	CE to Output Delay			200	ns
t_{OE}	OE to Output Delay			75	ns
t_{DF}(2)	OE Low to Output High Z			40	ns
t_{OH}(2)	Output Hold from Addresses, CE or OE Change-Whichever is First		0		ns
t_{LL}	Latch Deselect Width		50		ns
t_{AL}(2)	Address to Latch Set-Up		15		ns
t_{LA}	Address Hold from LATCH		30		ns
t_{LOE}	ALE to Output Enable		30		ns

NOTES:
1. See AC Testing Input/Output Waveforms for timing measurements.
2. Guaranteed and sampled.
3. Model Number Prefixes: No Prefix = CERDIP
   N = PLCC

AC CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) ..... 10 ns
Input Pulse Levels ..... V_{OL} to V_{OH}
Input Timing Reference Level 1.5V
Output Timing Reference Level ..... V_{IL} and V_{IH}

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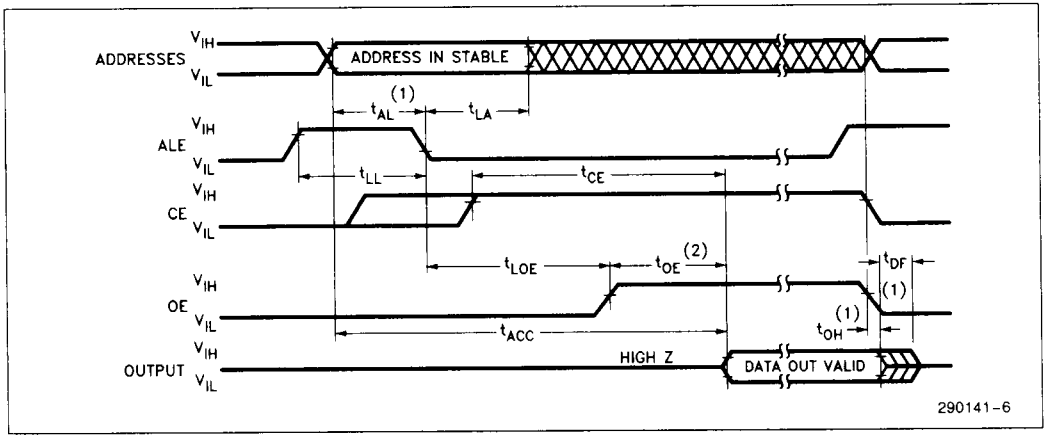
AC WAVEFORMS



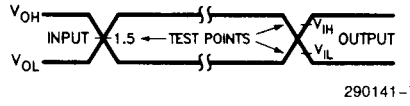
NOTES:
1. This parameter is only sampled and is not 100% tested.
2. OE may be delayed up to $t_{CE} - t_{OE}$ after the rising edge of CE without impact on t_{CE}.

CAPACITANCE(1) T_A = 25°C, f = 1.0 MHz

Symbol	Parameter	Max	Units	Conditions
C_{IN}	Address/Control Capacitance	6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	12	pF	V_{OUT} = 0V

NOTE:
1. Sampled. Not 100% tested.

AC TESTING INPUT/OUTPUT WAVEFORM



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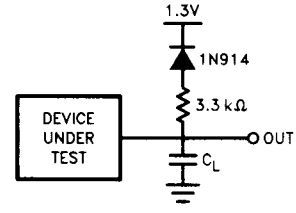
AC testing inputs are driven at V_{OH} for a Logic "1" and V_{OL} for a Logic "0". Timing measurements are made at V_{IH} for a Logic "1" and V_{IL} for a Logic "0".

AC TESTING LOAD CIRCUIT



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C_L = 100 pF
C_L Includes Jig Capacitance

DEVICE OPERATION

Table 1 lists A68C257 operating modes. Read mode requires a single 5V power supply. All input levels are TTL or CMOS except A_9 in int$_e$ligent Identifier mode and V_{PP}.

Table 1. Mode Selection

Mode \ Pins	CE	OE	A_9	A_0	ALE/V_{PP}	V_{CC}	Outputs
Read	V_{IH}	V_{IH}	X(1)	X	X	5.0V	D_{OUT}
Output Disable	V_{IH}	V_{IL}	X	X	X	5.0V	High Z
Standby	V_{IL}	X	X	X	X	5.0V	High Z
Programming(5)	V_{IL}	V_{IH}	X	X	(Note 4)	(Note 4)	D_{IN}
Program Verify(5)	V_{IH}	V_{IL}	X	X	(Note 4)	(Note 4)	D_{OUT}
Optional Program Verify	V_{IH}	V_{IH}	X	X	V_{CC} (Note 4)	(Note 4)	D_{OUT}
Program Inhibit(5)	V_{IH}	V_{IH}	X	X	(Note 4)	(Note 4)	High Z
int$_e$ligent Identifier(3, 5) -Manufacturer	V_{IL}	V_{IL}	V_H(2)	V_{IL}	X	V_{CC}	89 H
int$_e$ligent Identifier(3, 5) -A68C257	V_{IL}	V_{IL}	V_H(2)	V_{IH}	X	V_{CC}	27 H

NOTES:
1. X can be V_{IL} or V_{IH}.
2. V_H = 12.0V ±0.5V.
3. A_1–A_8, A_{10-12} = V_{IL}, A_{13-14} = X.
4. See Table 2 for V_{CC} and V_{PP} programming voltages.
5. During Int$_e$ligent Identifier Mode (A_9 = V_H) and Programming Modes (ALE/V_{PP} = 12.75V), CE and OE default to active-low enables.

Read Mode

The 68C257 has two control functions; both must be logically active to obtain data at the outputs. Chip Enable (CE) is the power control and the device-select. Output enable (OE) gates data to the output pins by controlling the output buffer. When the address is stable (ALE = V_{IH}) or latched (ALE = V_{IL}), the address access time (t_{ACC}) equals the delay from CE to output (t_{CE}). Outputs display valid data t_{OE} after the rising edge of OE, assuming t_{ACC} and t_{CE} times are met.

The 68C257 reduces the hardware interface in multiplexed address-data bus systems. Figure 4 shows a low power, small board space, minimal chip 68C257/microcontroller design. The processor's multiplexed bus (AD_{0-7}) is tied to the 68C257's address and data pins. No separate address latch is needed because the 68C257 latches all address inputs when ALE is low.

The ALE input controls the 68C257's internal address latch. As ALE transitions from V_{IH} to V_{IL}, the last address present at the address pins is retained. The OE control can then enable EPROM data onto the bus.

The 68C257 is ideal for systems with program memory at high-address locations. Address decoders and "glue" chips can be eliminated by simply tying address line A_{15} to the active-high CE. The 68C257's active-high OE input connects directly to a 68-family microcomputer's active-high READ strobe ("E" clock output).

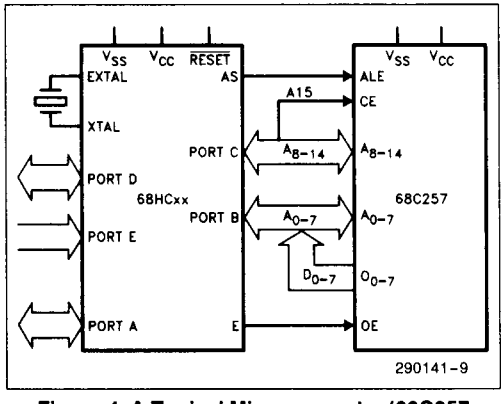

Figure 4. A Typical Microcomputer/68C257 System Configuration

Standby Mode

The standby mode substantially reduces V_{CC} current. When CE = V_{IL}, the standby mode places the outputs in a high impedance state, independent of the OE input.

Two Line Output Control

EPROMs are often used in larger memory arrays. Intel provides two contol inputs to accommodate multiple memory connections. Two-line control provides for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To efficiently use these two control inputs, an address decoder should enable CE while OE should be connected to all memory-array devices and the system's active-high READ control line. This assures that only selected memory devices have active outputs while deselected memory devices are in low-power standby mode.

SYSTEM CONSIDERATIONS

EPROM power switching characteristics require careful device decoupling. System designers are interested in three supply current (ICC) issues—standby current levels, active current levels, and transient current peaks produced by falling and rising edges of Chip Enable. Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-Line Control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 μF ceramic capacitor connected between its V_{CC} and GND. This high frequency, low inherent-inductance capacitor should be placed as close as possible to the device. Additionally, for every eight devices, a 4.7 μF electrolytic capacitor should be placed between V_{CC} and GND at the array's power supply connection. The bulk capacitor will overcome voltage slumps caused by PC board trace inductances.

PROGRAMMING MODES

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

Initially, and after each erasure, all EPROM bits are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" are programmed, the data word

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can contain both "1s" and "0s". Ultraviolet light erasure is the only way to change "0s" to "1s".

The programming mode is entered when V_{PP} is raised to its programming voltage (see Table 2). Data is programmed by applying an 8-bit word to the output pins (O_{0-7}). Pulsing CE to TTL-low while OE = V_{IH} will program data. TTL levels are required for address and data inputs.

To simplify programming, CE and OE inputs default to active-low (as opposed to read modes active-high) enables when either $A_9 = V_H$ or ALE/V_{PP} is at its programming voltage (12.75V). This allows programming equipment to identify the 68C257 and program it with a standard programming algorithm. The 68C257 uses the same programming algorithm as the 87C257. Programming equipment that programs one device can also program its counterpart.

Program Inhibit

The Program Inhibit mode allows parallel programming of multiple EPROMs with different data. With V_{PP} at its programming voltage, a CE-low pulse programs the desired EPROM. CE-high inputs inhibit programming of non-targeted devices. Except for CE and OE, parallel EPROMs may have common inputs.

Program Verify

With V_{PP} and V_{CC} at their programming voltages, a verify (read) determines that bits are correctly programmed. The verify is performed with CE = V_{IH} and OE = V_{IL}. Valid data is available t_{OE} after OE falls low.

Optional Program Verify

The optional verify allows parallel programming and verification when several devices share a common bus. It is performed with CE = OE = V_{IH} and V_{PP} = V_{CC} = 6.25V. The normal read mode is then used for program verify. Outputs will tri-state depending on OE and CE.

inteligent Identifier™ Mode

The inteligent Identifier Mode will determine an EPROM's manufacturer and device type. Programming equipment can automatically match a device with its proper programming algorithm.

This mode is activated when programming equipment forces 12V ±0.5V on the EPROM's A_9 address line. With A_1–A_8, A_{10}–A_{12} = V_{IL} (A_{13-14} are don't-care), address line $A_0 = V_{IL}$ will present the manufacturer's code and $A_0 = V_{IH}$ the device code (see Table 1). When $A_9 = V_H$, CE and OE default to active-low and ALE need not be toggled to latch each identifier address. This mode functions in the 25°C ±5°C ambient temperature range required during programming.

ERASURE CHARACTERISTICS (FOR CERDIP EPROMS)

Exposure to light of wavelength shorter than 4000 Angstroms (Å) begins EPROM erasure. Sunlight and some fluorescent lamps have wavelengths in the 3000–4000Å range. Constant exposure to room-level fluorescent light can erase an EPROM in about 3 years (about 1 week for direct sunlight). Opaque labels over the window will prevent unintentional erasure under these lighting conditions.

The recommended erasure procedure is exposure to 2537Å ultraviolet light. The minimum integrated dose (intensity x exposure time) is 15 Wsec/cm^2. Erasure time using a 12000 μW/cm^2 ultraviolet lamp is approximately 15 to 20 minutes. The EPROM should be placed about 1 inch from the lamp. The maximum integrated dose is 7258 Wsec/cm^2 (1 week @ 12000 μW/cm^2). High intensity UV light exposure for longer periods can cause permanent damage.

CHMOS NOISE CHARACTERISTICS

System reliability is enhanced by Intel's CHMOS EPI-process techniques. Protection on each data and address pin prevents latch-up; even with 100 mA currents and voltages from −1V to V_{CC} + 1V. Additionally, the V_{PP} pin is designed to resist latch-up to the 14V maximum device limit.

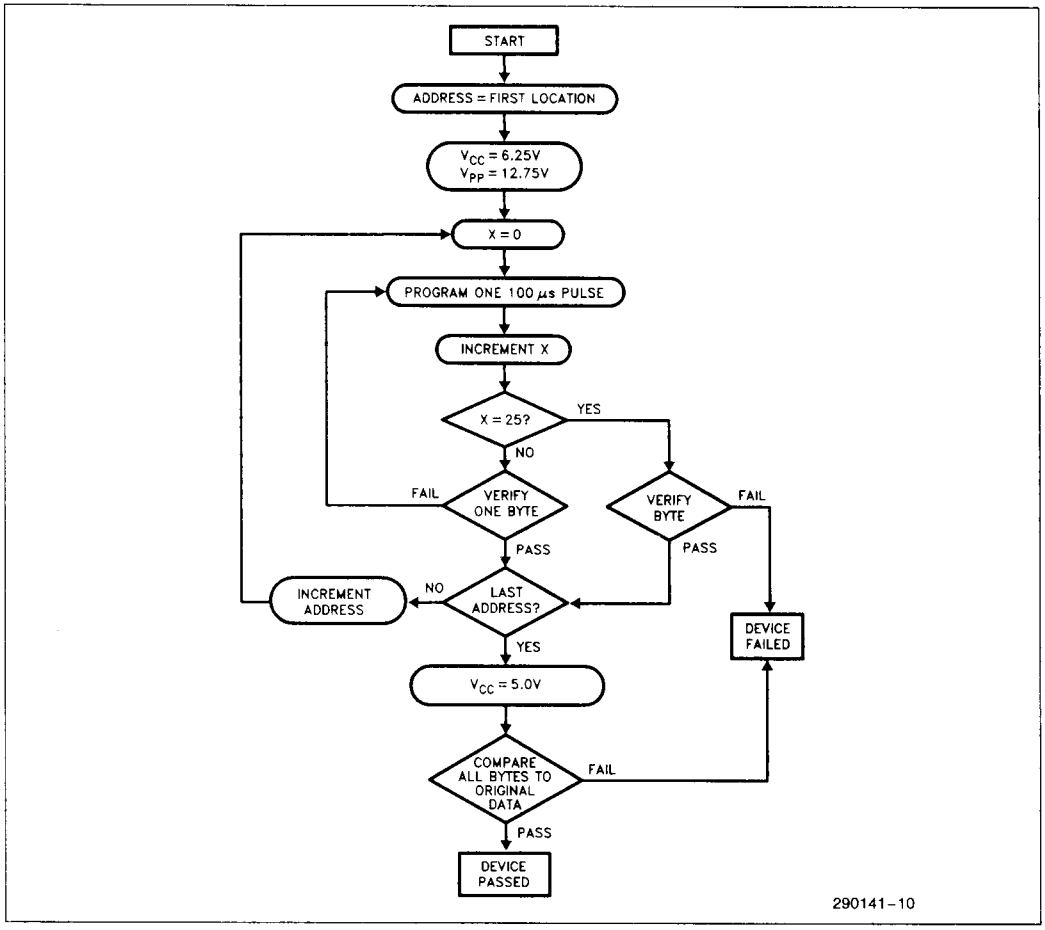

Figure 5. Quick-Pulse Programming™ Algorithm

Quick-Pulse Programming™ Algorithm

The Quick-Pulse Programming algorithm programs Intel's 68C257 EPROM. Developed to substantially reduce production programming throughput time, this algorithm can program a 68C257 in under four seconds. Actual programming time depends on the PROM programmer used.

The Quick-Pulse Programming algorithm uses a 100 microsecond initial-pulse followed by a byte verification to determine when the addressed byte is correctly programmed. The algorithm terminates if 25 100μs pulses fail to program a byte. Figure 5 shows the Quick-Pulse Programming algorithm flowchart.

The entire program-pulse/byte-verify sequence is performed with V_{CC} = 6.25V and V_{PP} = 12.75V. When programming is complete, all bytes should be compared to the original data with V_{CC} = 5.0V.

In addition to the Quick-Pulse Programming Algorithm, the 68C257 has also been characterized for the Quick-Board Programming Algorithm. The Quick-Board Programming Algorithm was developed for specific automotive applications using Intel's 1.0 micron EPROM products. Contact the factory or an automotive sale representative for any information regarding the Quick-Board Programming Algorithm.

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DC PROGRAMMING CHARACTERISTICS $T_A = 25°C \pm 5°C$

Table 2

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Unit	
I_{LI}	Input Current (All Inputs)		1.0	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.2	0.8	V	
V_{IH}	Input High Level	2.0	$V_{CC} + 0.5$	V	
V_{OL}	Output Low Voltage During Verify		0.4	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage During Verify	$V_{CC} - 0.8$		V	$I_{OH} = -400$ μA
I_{CC2}(3)	V_{CC} Supply Current		30	mA	
I_{PP2}(3)	V_{PP} Supply Current (Program)		50	mA	$CE = V_{IL}$
V_{ID}	A9 intelligent Identifier Voltage	11.5	12.5	V	
V_{PP}(1)	Programming Voltage	12.5	13.0	V	
V_{CC}(1)	Supply Voltage During Programming	6.0	6.5	V	

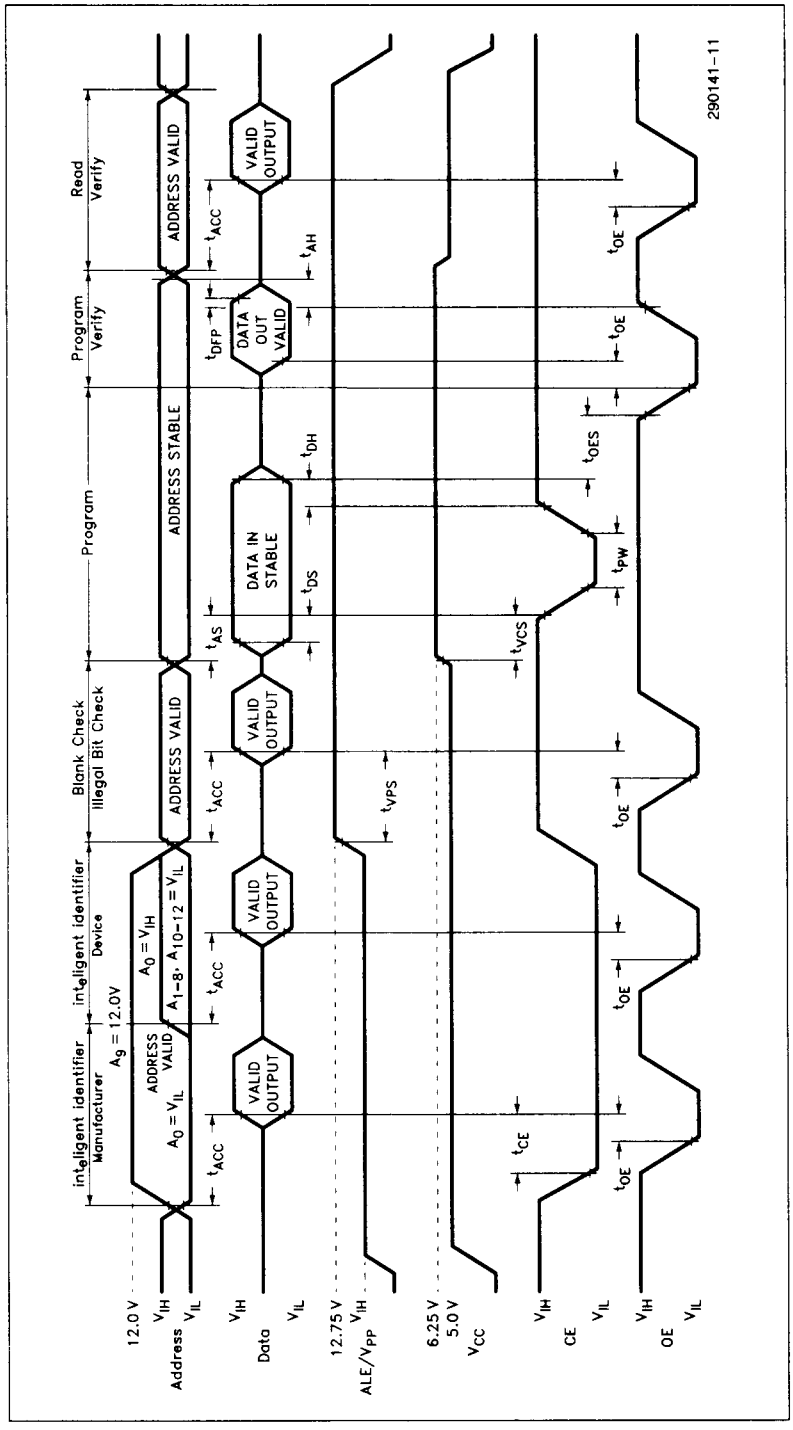
AC PROGRAMMING CHARACTERISTICS

$T_A = 25°C \pm 5°C$; see Table 2 for V_{CC} and V_{PP} voltages.

Symbol	Parameter	Limits				Conditions
		Min	Typ	Max	Unit	
t_{AS}	Address Setup Time	2			μs	
t_{OES}	OE Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DFP}(2)	OE High to Output Float Delay	0		130	ns	
t_{VPS}(1)	V_{PP} Setup Time	2			μs	
t_{VCS}(1)	V_{CC} Setup Time	2			μs	
t_{PW}	CE Program Pulse Width	95	100	105	μs	
t_{OE}	Data Valid from OE			150	ns	

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
3. The maximum current value is with outputs O_0 to O_7 unloaded.

PROGRAMMING WAVEFORMS



NOTES:
1. The input timing reference level is $V_{IL} = 0.8V$ and $V_{IH} = 2V$.
2. t_{OE} and t_{DFP} are device characteristics but must be accommodated by the programmer.
3. To prevent device damage during programming, a 0.1 µF capacitor is required between V_{PP} and ground to suppress spurious voltage transients.
4. During programming, the address latch function is bypassed whenever $V_{PP} = 12.75V$ or $A_9 = V_H$. When V_{PP} and A_9 are at TTL levels, the address latch function is enabled, and the device functions in read mode.
5. V_{PP} can be 12.75V during Blank Check and Final Verify; if so, CE must be V_{IH}.

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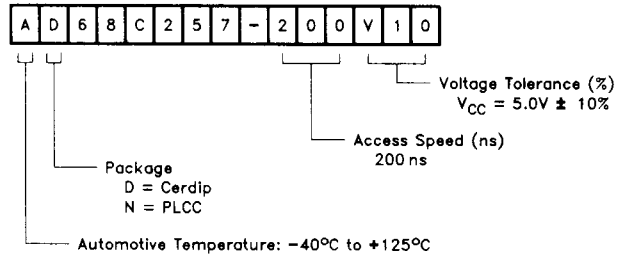
ORDERING INFORMATION



Valid Combinations:

AD68C257-200V10 AN68C257-200V10

REVISION HISTORY

Number	Description
003	Deleted reference to Intel's int$_e$ligent Programming Algorithm Added new Quick-Board Programming Algorithm.