MBM27C256-25, MBM27C256-30, MBM27C256-45

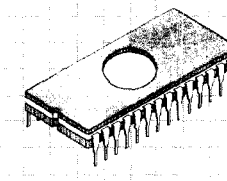
CMOS 32,768 X 8-Bit UV Erasable and Electrically Programmable Read Only Memory

Description

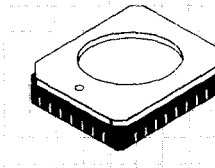
The Fujitsu MBM27C256 is a high speed 262,144-bits complementary MOS erasable and electrically reprogrammable read only memory (EPROM). It is especially well suited for application where rapid turn-around and/or bit pattern experimentation, and low-power consumption are important.

A 28-pin dual-in line package with a transparent lid and 32-pad leadless chip carrier (LCC) are used to package the MBM27C256. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MBM27C256 is fabricated using CMOS double polysilicon gate technology with single transistor stacked gate cells. It is organized as 32,768 words by 8-bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.



Ceramic Package DIP-28C-C01

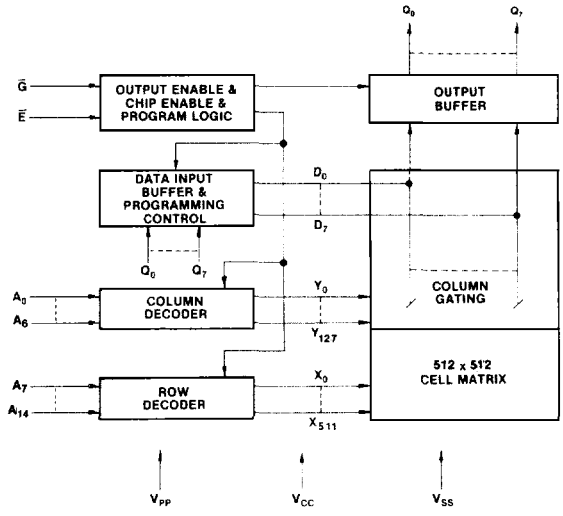


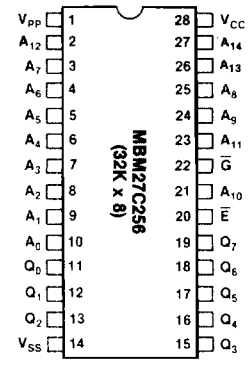
Ceramic Package LCC-32C-A01

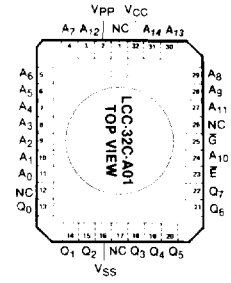
Features

- CMOS Power Consumption: 550 μW max. (Standby) 40 mW/MHz (Active)
- 32,768 words by 8-bits organization, fuly decoded
- Simple programming requirements
- Single location programming
- High speed programming algorythm (typically two 1 ms pulses)
- No clock required (fully static operation)
- TTL compatible inputs and outputs
- Three state output with OR-tie capability
- Output Enable $\overline{G}$ pin for simplified memory expansion
- Fast Access Time: MBM27C256-25 250 ns max. MBM27C256-30 300 ns max. MBM27C256-45 450 ns max.
- Single +5V operation
- Jedec Standard 28-pin DIP package/32-pad LCC

MBM27C256 Block Diagram and Pin Assignments







Absolute Maximum Ratings
(See Note)

Parameter	Symbol	Value	Unit
Temperature Under Bias	T_A	−25 to +85	°C
Storage Temperature	T_{stg}	−65 to +125	°C
Inputs/Outputs with Respect to GND	V_{IN}, V_{OUT}	−0.6 to +7	V
V_{PP} with Respect to GND	V_{PP}	−0.6 to +22	V
V_{CC} with Respect to GND	V_{CC}	−0.6 to +7	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may effect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. It is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Functions and Pin Connections

Function (DIP Pin No.) / Mode	Address Input (2~10, 21, 23~27)	Data (11~13, 15~19)	$\overline{E}$ (20)	$\overline{G}$ (22)	V_{CC} (28)	V_{PP} (1)	V_{SS} (14)
Read	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{CC}	V_{CC}	GND
Output Disable	A_{IN}	High Z	V_{IL}	V_{IH}	V_{CC}	V_{CC}	GND
Stand By	Don't Care	High Z	V_{IH}	Don't Care	V_{CC}	V_{CC}	GND
Program	A_{IN}	D_{IN}	V_{IL}	V_{IH}	V_{CC}	V_{PP}	GND
Program Verify	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{CC}	V_{PP}	GND
Program Inhibit	Don't Care	High Z	V_{IH}	Don't Care	V_{CC}	V_{PP}	GND

Capacitance
(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)	C_{IN}	—	4	6	pF
Output Capacitance (V_{OUT} = 0V)	C_{OUT}	—	8	12	pF

Recommended Operating Conditions
(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
V_{CC} Supply Voltage[1]	V_{CC}	4.50	5.0	5.50	V	0°C to +70°C
V_{PP} Supply Voltage	V_{PP}	V_{CC} −0.6	—	V_{CC} +0.6	V	
Input High Voltage	V_{IH}	2.0	—	V_{CC} +0.3	V	
Input Low Voltage	V_{IL}	−0.1	—	0.8	V	

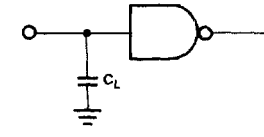
Note 1. V_{CC} must be applied either before or coincident with V_{PP} and removed either after or coincident with V_{PP}.

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Input Load Current (V_{IN} = 5.25V)	I_{LI}	—	—	10	μA
Output Leakage Current (V_{OUT} = 5.25V)	I_{LO}	—	—	10	μA
V_{PP} Supply Current	I_{PP}	—	1	100	μA
V_{CC} Standby Current ($\overline{E}$ = V_{IH})	I_{SB1}	—	—	1	mA
V_{CC} Standby Current ($\overline{E}$ = V_{CC} −0.3V to V_{CC} + 0.3V, I_{OUT} = 0mA)	I_{SB2}	—	1	100	μA
V_{CC} Active Current ($\overline{E}$ = V_{IL})	I_{CC1}	—	—	30	mA
V_{CC} Operation Current (f = 4MHz, I_{OUT} = 0mA)	I_{CC2}	—	—	30	mA
Output Low Voltage (I_{OL} = 2.1mA)	V_{OL}	—	—	0.45	V
Output High Voltage (I_{OH} = −400μA)	V_{OH1}	2.4	—	—	V
Output High Voltage (I_{OH} = −100μA)	V_{OH2}	V_{CC} −0.7	—	—	V

AC Test Conditions

Input Pulse Levels:	0.8 V to 2.0 V
Input Rise and Fall Time:	≤20 ns
Timing Measurement Reference Levels:	1.0 V and 2.0 V for inputs 0.8 V and 2.0 V for outputs
Output Load:	1 TTL gate and C_L = 100pF



AC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MBM27C256-25 Min	MBM27C256-25 Max	MBM27C256-30 Min	MBM27C256-30 Max	MBM27C256-45 Min	MBM27C256-45 Max	Unit
Address to Output Delay ($\overline{E}$ = $\overline{G}$ = V_{IL})	TAVQV	—	250	—	300	—	450	ns
$\overline{E}$ to Output Delay ($\overline{G}$ = V_{IL})	TELQV	—	250	—	300	—	450	ns
$\overline{G}$ to Output Delay ($\overline{E}$ = V_{IL})	TGLQV	—	100	—	120	—	150	ns
Output Enable High to Output Float (See Note)	TGHQZ	0	60	0	105	—	130	ns
Address to Output Hold	TAXQX	0	—	0	—	0	—	ns

Note: TGHQZ is specified from $\overline{E}$, or $\overline{G}$, whichever occurs first.

Programming/Erasing Information, continued

The programming mode is entered when +6V is applied to the VCC pin followed by applying +21V to VPP pin. A TTL low input must be applied to the E input and a TTL high input must be applied to the G input. After the programming voltages and TTL levels have stabilized, a sequence of 1 millisecond pulses must be applied to the P pin for programming. After each pulse, a pulse counter must be incremented and the location should be checked for accuracy. Upon verification, an additional sequence of 1 millisecond pulses equal to the present value of the pulse counter must be applied to the location to ensure proper levels of stored charge. An alternate approach to the additional pulses would be to apply a single TTL low pulse with a width equivalent to the value of the pulse counter multiplied by 1 millisecond. When the pulse counter reaches a maximum of 20, the verification procedure is skipped and a flag is set to indicate a program failure. Upon completion of programming of the entire device, a final array verification (all locations) is required. All Fujitsu devices will typically require only two 1 millisecond pulses (one initial and one additional) to reach sufficient stored charge levels.

Erasure

In order to clear all locations of their programmed contents, it is necessary to expose the MBM27C256 to an ultraviolet light source. A dosage of 15W-seconds/cm^2 is required to completely erase an MBM27C256. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å) with intensity of 12,000μW/cm^2) for 15 to 20 minutes. The MBM27C256 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

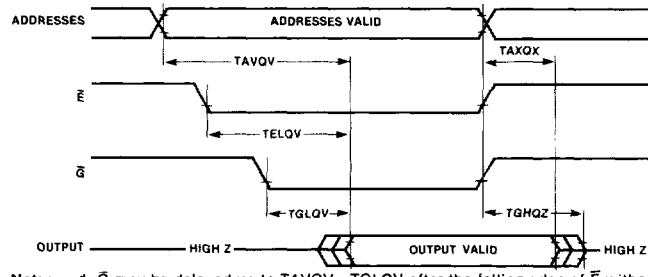
It is important to note that the MBM27C256 and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, nevertheless, the exposure to fluorescent light and sunlight will eventually erase the MBM27C256 and such exposure should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

DC Characteristics
(T_A = 25 ±5°C, V_{CC} = 6V ±0.25V, V_{PP} = 21V ±0.5V)

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IN} = 5.25V/0.45V)	I_{LI}	—	—	10	μA
V_{PP} Supply Current During Programming Pulse ($\overline{E} = V_{IL}$)	I_{PP}	—	—	30	mA
V_{CC} Supply Current	I_{CC}	—	—	30	mA
Input Low Voltage	V_{IL}	−0.1	—	0.8	V
Input High Voltage	V_{IH}	2.0	—	V_{CC} +0.3	V
Output Low Voltage During Verify (I_{OL} = 2.1 mA)	V_{OL}	—	—	0.45	V
Output High Voltage During Verify (I_{OH} = −400μA)	V_{OH}	2.4	—	—	V

Notes:
(1) V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.
(2) V_{PP} must not be greater than 21.5 V including overshoot. Permanent device damage may occur if the device is taken out or put into socket remaining V_{PP} = 21 volts. Also, during $\overline{E} = V_{IL}$, V_{PP} must not be switched from 5 volts to 21 volts or vise-versa.

Operation Timing Diagram



Notes: 1. $\overline{G}$ may be delayed up to TAVQV—TGLQV after the falling edge of $\overline{E}$ without impact on TAVQV.
2. TGHQZ is specified from $\overline{E}$ or $\overline{G}$, whichever occurs first.

Programming/Erasing Information

Memory Cell Description

The MBM27C256 is fabricated using a single-transistor stacked gate cell construction, implemented via double-layer polysilicon technology. The individual cells consist of a bottom floating gate and a top select gate (see Fig. 3). The top gate is connected to the row decoder, while the floating gate is used for charge storage. The cell is programmed by the injection of high energy electrons through the oxide and onto the floating gate. The presence of the charge on the floating gate causes a shift in the cell threshold (refer to Fig. 4). In the initial state, the cell has a low threshold (V_{TH1}) which will enable the transistor to be turned on when the cell is selected (via the top select gate). Programming shifts the threshold to a higher level (V_{TH0}), thus preventing the cell transistor from turning on when selected. The status of the cell (i.e., whether programmed or not) can be determined by examining its state at the sense threshold (V_{THS}), as indicated by the dotted line in Fig. 4.

Conventional Programming

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM27C256 has all 262,144 bits in the "1", or high, state. "0's" are loaded into the MBM27C256 through the procedure of programming.

The programming mode is entered when +21V is applied to the V_{PP} pin and $\overline{E}$ is at V_{IL}. During programming, $\overline{E}$ is kept at V_{IL}. A 0.1μF capacitor between V_{PP} and V_{SS} is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. A pattern of eight bits are placed on the respective output pins. The voltage levels should be standard TTL levels.

The procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. All that is required is that one 50 msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55.0 msec.

"Quick Pro" Programming

In addition to the standard 50 millisecond pulse width programming procedure, the MBM27C256 can be programmed with a fast programming algorithm designed by Fujitsu called Quick Pro™. The algorithm (shown in figure 3) utilizes a sequence of 1 millisecond pulse to program each location. This algorithm will typically yield a savings of 86% in programming time per device when utilized in commercially available programmers. However, in custom programmer designs that require less overhead the savings can be even greater.

Fig. 1 — Memory Cell

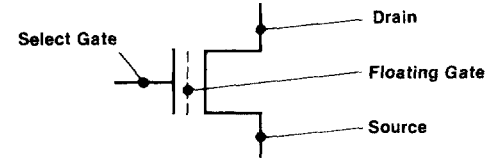
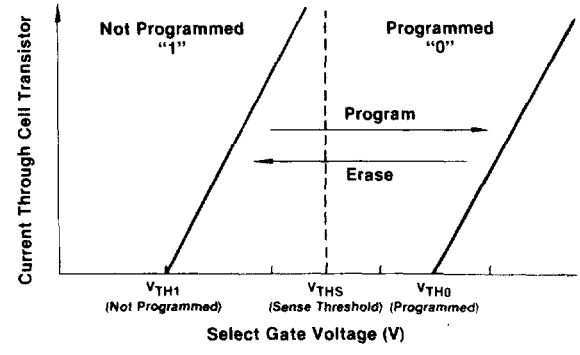


Fig. 2 — Memory Cell Threshold Shift



AC Characteristics
(T_A = 25 ±5°C,
V_{CC} = 5V ±5%
V_{PP} = 21V ±0.5V)

Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time	TAVEL	2	—	—	μs
$\overline{E}$ Setup Time	TEHGH	2	—	—	μs
$\overline{G}$ Setup Time	TGHEL	2	—	—	μs
Data Setup Time	TDVEL	2	—	—	μs
V_{PP} Setup Time	TVPPHEL	2	—	—	μs
Address Hold Time	TEHAX	2	—	—	μs
$\overline{G}$ Hold Time [1]	TEHGL	2	—	—	μs
Data Hold Time	TEHDZ	2	—	—	μs
$\overline{G}$ Recovery Time [1]	TGLEL	2	—	—	μs
$\overline{E}$ to Output Valid	TELQV	—	—	1	μs
Output Disable to Output Float Delay	TEHQZ	—	—	130	ns
Programming Pulse Width-Quick-Pro™	TELEH	0.95	1.00	1.05	ms
Programming Pulse Width-Conventional	TELEH	45	50	55	

[1] TEHGL + TGLEL ≥ 50 μs

Programming Waveform