October 1999

H8S and H8/300H

16-Bit

Microcontrollers

HITACHI


H8S/2238
HD
64F2238TE
JAPAN

H8S and H8/300H

16-Bit

Microcontrollers

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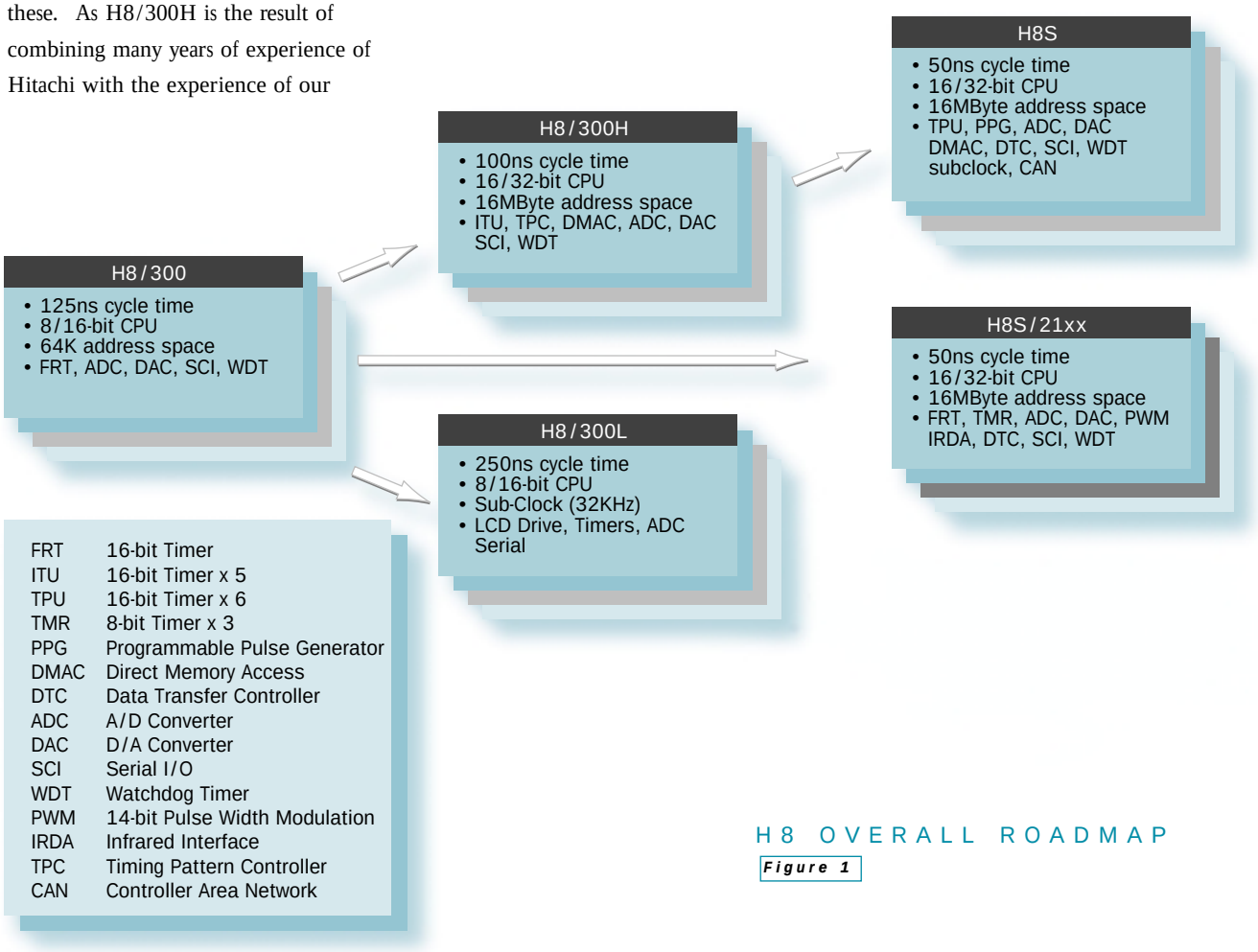
INDEX

Welcome **To**

Hitachi's 16-bit microcontroller families H8S and H8/300H.

Hitachi is the second biggest supplier of 16-bit microcontrollers to the European market (according to Dataquest), as well as the third for 4-bit, sixth for 8-bit and number 2 for 32-bit RISC microcontrollers (the latter on a world-wide basis).

At Hitachi Europe we think that this success is driven by our strong commitment to be a leading force in the microcontroller marketplace and our belief that we must listen to our customer's requirements and then meet these. As H8/300H is the result of combining many years of experience of Hitachi with the experience of our customers, H8/300H is an excellent example where this policy has worked for our customers and Hitachi.
In continuation of this policy H8S is Hitachi's answer to our customers request for more performance and lower power consumption at better cost/performance ratios. Hitachi also added larger memories and improved the peripherals to allow single-chip systems, where previously several components have been necessary. Switching such a multi-chip system to a single-chip system can drastically reduce radiation, in today's electronic industry a very important concern.



H8 OVERALL ROADMAP

Figure 1

The European electronics industry demands full service and support. Hitachi, responded by setting up a European engineering and tool design subsidiary 12 years ago: Hitachi Microsystems Europe (HMSE) based in Maidenhead (UK).
HMSE provides our customers with locally designed and supported tools ranging from low cost evaluation boards to fully featured real time emulators based on IBM-compatible PC's at a very competitive price. Software ranges from Assembler, an ANSI C-Compiler via a C-level debugger to MakeApp, a tool that sets up peripherals and creates driver routines on the click of a mouse.

H8S and H8/300H are part of Hitachi's software compatible H8 product range, which covers a performance range from 400ns to 40ns cycle time, whilst increasing word length from 8 to 16 bit and memory space from 64KB to 16MB. This product range offers an industry leading mix of memory options (including many flash derivatives), peripherals and performance/power consumption, all of this being software compatible for protection of our customer's software investment. Hitachi produces and ships over 20 million H8 microcontrollers every month, in a vast range of advanced packaging and temperature options.

H8S offers up to 25 native MIPS peak performance (resulting in almost 10 Dhrystone MIPS), the peripherals and the memory options (for example H8S/2238F with 256KB Flash and 16K RAM) to make it an industry standard in telecommunications and very successful in industrial (e. g. motor control, vending machines, security systems) and emerging consumer applications like new electronic video cameras, still cameras and advanced car radios. Just recently H8S and H8/300H have also enjoyed much success in automotive applications, as CAN is now available on-chip and in the rapidly growing field of smart-card appliances, because many derivatives include one or more ISO7816-compliant serial interfaces.

From a statistics point of view, every day 2 customers decide to use a 16-bit microcontroller made by Hitachi.

Usually our customer's product development will continue to proliferate over the years. For those customers who may need more performance than 16-bit microcontrollers can offer, it is good to know that Hitachi is an industry leader in 32-bit RISC microcontrollers as well. Hitachi's SH1 and SH2 RISC microcontroller families offer 10 MIPS or more (Dhrystone), as well as similar or in some cases even the same peripherals and memory options up to 256K Flash and 10K RAM. Please order Hitachi's SH RISC microcontroller shortform to get a detailed introduction!

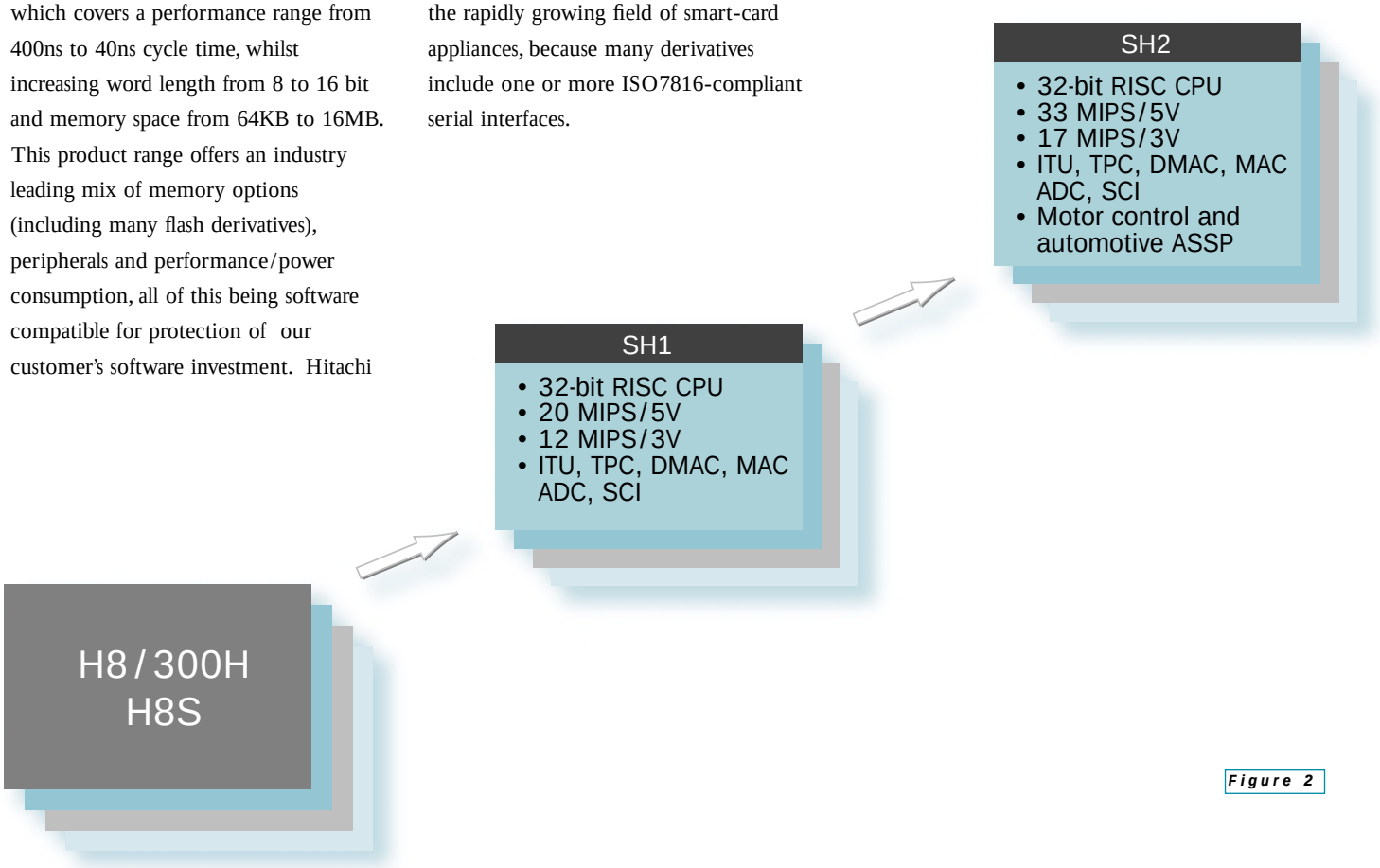
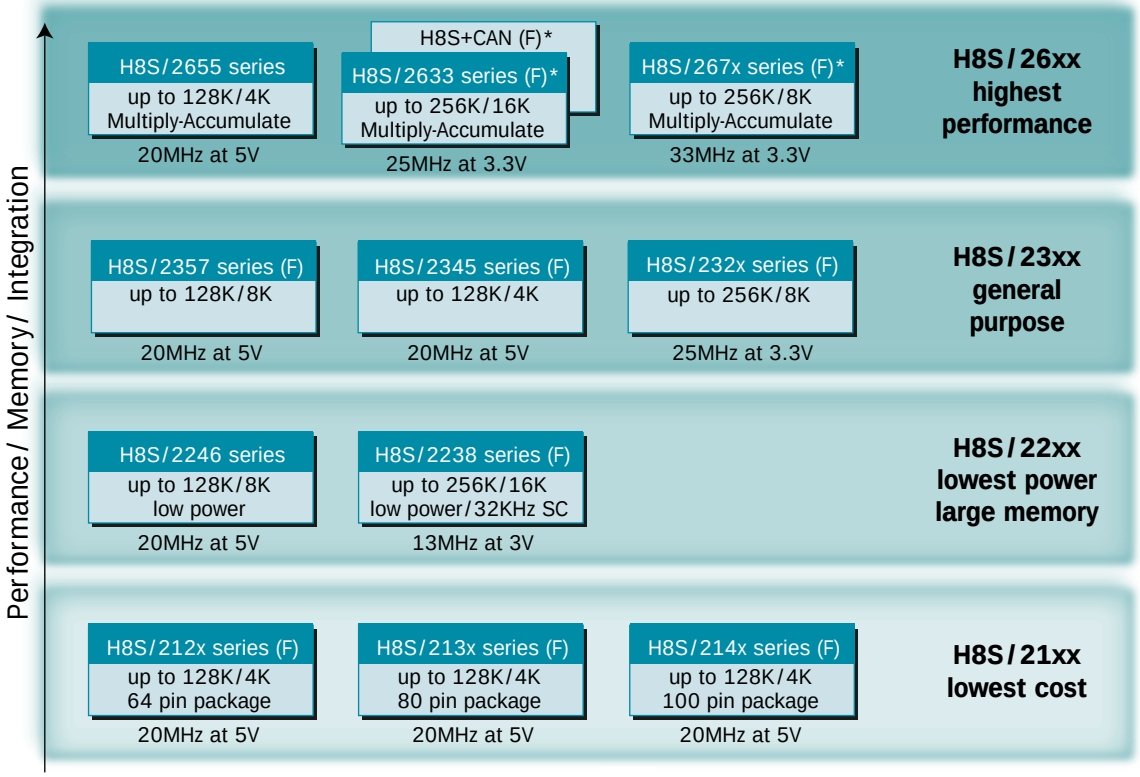


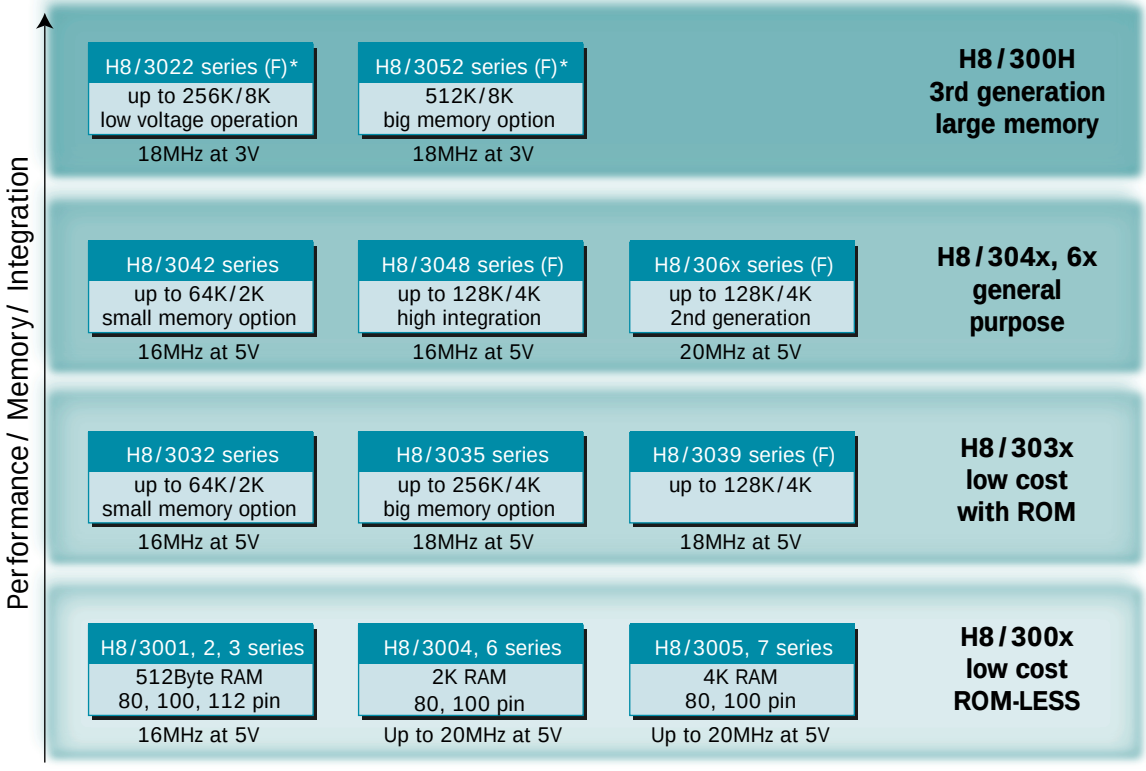
Figure 2

H8S Roadmap



* Under development (F) FLASH version available Note: most 5V derivatives are also available in 3V/10MHz or 3V/13MHz

H8/300H Roadmap



* Under development (F) FLASH version available Note: most 5V derivatives are also available in 3V/8MHz or 3V/10MHz

Figure 3

C P U

All H8 share a common CPU architecture, a general purpose register architecture that allows efficient execution of software written in C and produces dense code. A good code density is important to reduce the amount of memory needed, which in turn results in a lower system cost and helps to avoid external memory. As shown below in figure 5 the 8-bit H8 families have 16-bit wide registers and the 16-bit families have 32-bit wide registers, all of which can also be used partially (for example in bytes). H8S adds an extended Condition Code Register (EXR) to allow improved interrupt control and H8S/2655 adds a Multiply-Accumulate Unit (MAC) to boost performance in DSP-type applications.

Furthermore H8S executes basic instructions in only one clock cycle, half as many as H8/300H.

Being general purpose there is no restriction placed on how each register is used, thus they can be used for pointer or data operations. The architecture also allows any of the data addressing modes to be used in conjunction with any register.

This rich set of general purpose registers provides the compiler writer with ample opportunities to optimise the code generated by the compiler. Local variables can be optimised into registers wherever possible, thus reducing the number of bytes of code needed to manipulate them. Also, because each register can be used as an accumulator, index register or address pointer, the address arithmetic which must be performed by the compiler can be done very effectively. Register ER7 is used as a stack pointer, so all accesses to stack based data can be performed very fast.

In addition to the general purpose registers there are two control registers, a Condition Code Register (CCR) and a Program Counter (PC). The CCR is an 8-bit wide register which contains all the CPU flags such as overflow, zero and carry as well as the interrupt flags. The carry flag also doubles as a bit accumulator when the bit manipulation operations are used.

The H8/300H CPU offers a H8/300 compatible mode which allows straightforward reuse of existing H8/300 software. This mode is available in H8/3032, H8/3042 and µCBIC products.

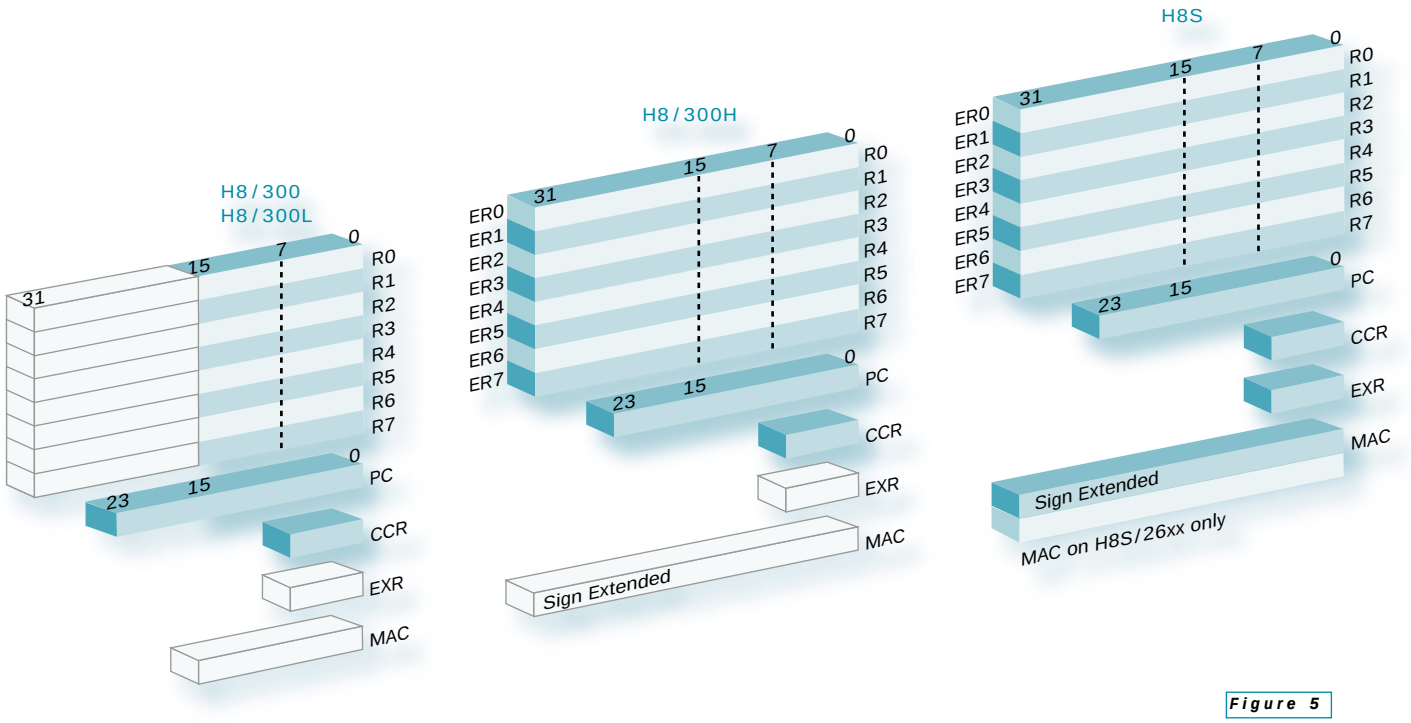


Figure 5

Instruction **Set**

H8/300H has an instruction set which suits the combined needs of HLL programming and embedded applications. It comprises of 62 instructions, with an emphasis on arithmetic instructions, address manipulation and bit processing. More than half of all instructions have an instruction length of only 2 Bytes making very compact code. H8S extends the instruction set to 69 instructions. BOLD instructions are new on H8S.

Function	Instruction
Data transfer	MOV, PUSH, POP, MOVTPE, MOVFPE, **LDM, STM**
Arithmetic operations	ADD, SUB, ADDX, SUBX, INC, DEC, ADDS, SUBS, DAA, DAS, MULXU, DIVXU, MULXS, DIVXS, CMP, NEG, EXTS, EXTU, **TAS, MAC, LDMAC, STMAC, CLRMAC**
Logic operations	AND, OR, XOR, NOT
Shift operations	SHAL, SHAR, SHLL, SHLR, ROTL, ROTR, ROTXL, ROTXR
Bit manipulation	BSET, BCLR, BNOT, BTST, BAND, BIAND, BOR, BIOR BXOR, BIXOR, BLD, BILD, BST, BIST
Branch	Bcc, JMP, BSR, JSR, RTS
System control	TRAPA, RTE, SLEEP, LDC, STC, ANDC, ORC, XORC, NOP

In comparison with the H8/300 CPU most of the data transfer, logical, shift and arithmetic instructions are improved to handle 16 and 32-bit data. New instructions added to the H8/300H include signed multiplication, sign extension, 16-bit branch instructions and a software trap instruction.

H8S further improves the instruction set by adding STM (store multiple) and LDM (load multiple). These instructions allow to evacuate multiple registers on to the stack, thus drastically shortening the time if compared with multiple PUSH and POP. For example, pushing 4 registers onto the stack takes 40 states on H8/300H and only 11 on H8S. Also improved are some bit manipulations (to include 16/32-bit absolute addressing) and shift operations to support 2-bit shifts. H8S/2655 also adds instructions to support the Multiply-Accumulate-Unit.

Arithmetic Instructions

In order to perform complex algorithms such as digital filtering, H8S and H8/300H are equipped with powerful arithmetic instructions, including addition and subtraction on 32-bit data and multiplication of 16 x 16-bit data and division of 32 / 16-bit data. Multiplication and division are both available as signed and unsigned operations, which eliminate the need for time consuming library calls. The table below gives a guide to the execution speed of various arithmetic instructions with a clock of 16MHz (H8/300H) and 20MHz (H8S).

Operation	H8S	H8/300H
Add 32bit operands	50ns	125ns
AND 32 bit operands	50ns	125ns
multiply/divide 16bit operands (32bit result, signed)	200ns/ 650ns	875ns

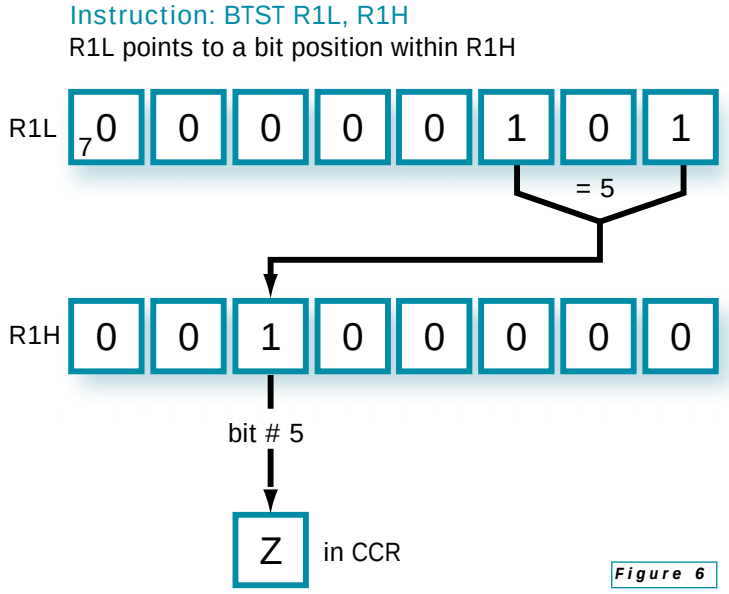


Figure 6

Bit Processing

In microcontroller applications it is often necessary to manipulate data on a bit by bit basis. A good example would be where an I/O pin needs to be set to switch on a lamp or a solenoid. To meet this demand H8S and H8/300H have 14 separate bit processing instructions which allow the programmer to manipulate bit data very easily.

It is also possible to perform boolean algebra on bit data using the carry flag of the CCR register as a bit accumulator. In a microcontroller application it is often necessary to perform a branch depending on the values of two bit flags located in RAM or I/O ports. Using the boolean operations provided by H8S and H8/300H the first bit can be loaded into the carry flag. Then a bitwise logical operation can be executed using the second bit. This sequence would then be followed by a branch depending on the value of the carry flag.

Another feature of the H8S and H8/300H bit processing capability is its ability to access bits indirectly, using the value from a general purpose register as a bit pointer. This mechanism is shown in figure 6 and is useful for scanning a byte for set or cleared bits.

Software Interrupt

The TRAPA instruction has been implemented in the H8S and H8/300H CPU. This instruction implements a software interrupt, jumping to a service routine via one of four exception vectors (TRAPA 0 - 3). This operation can be used to implement fast, space efficient calls to often used sub-routines such as schedulers and other O/S routines. The TRAPA instruction can also be used as a call to an error handling routine.

Addressing

To support large memory systems, the linear address space of the H8/300H and the H8S CPU core allows direct access to every address in the whole 16MByte address space via 24-bit address pointers. The linear address space means there is no need to set up page registers and there are also no limitations on the size of code modules or data arrays and structures.

Addressing Modes

Another way a CPU architecture can support the efficiency of the compiler is by providing a full set of powerful and flexible addressing modes. To ensure that the compiler is as efficient as possible the H8S and H8/300H CPU's provide eight addressing modes as shown in the table. Each instruction can use a subset of the available addressing modes. Supporting both, array and stack data types, the CPU has indirect addressing with either postincrement or predecrement. These modes support byte, word and long word data (±1,2 and 4) as shown in figure 7.

Three absolute addressing modes are provided using 8, 16 or 24-bit absolute addresses. Using the 24-bit address the entire 16MBytes address space is accessible. The 8 and 16-bit absolute address modes assume that the upper byte or word of the address is H'FFFF or H'FF respectively. This allows for the efficient address specification for the on-chip I/O area and RAM areas which are both placed at the top of the address map. These shortened addresses save significant amounts of code when these areas are accessed.

Register direct	R n
Register indirect	@ E R n
Register indirect with displacement	@ (d: 16, E R n) @ (d: 24, E R n)
Register indirect with post-increment/ Register indirect with pre-decrement	@ E R n +, @ - E R n
Absolute address	@ a a : 8, @ a a : 16, @ a a : 24
Immediate	# x x : 8, # x x : 16, # x x : 32
PC-relative	@ (d : 8, PC), @ (d : 16, PC)
Memory indirect	@@ a a : 8

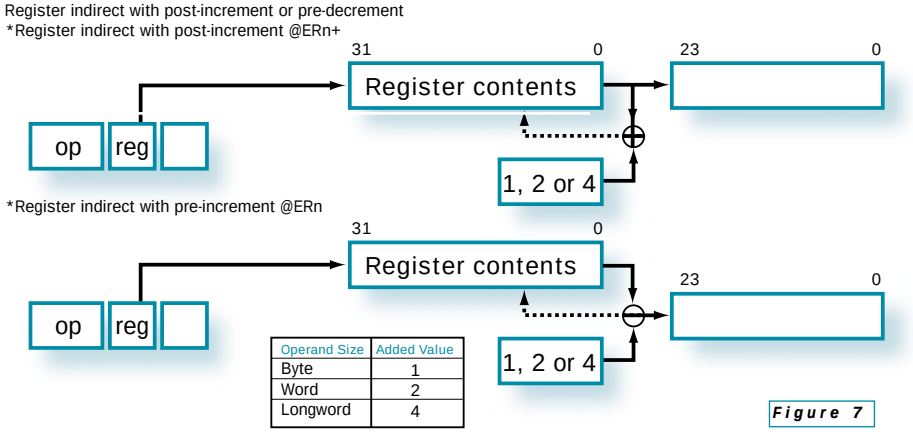


Figure 7

Low **Power**

In today's electronics industry, low power consumption is an ever increasing concern for many engineers. Beyond obvious reasons like longer battery life for example in mobile phones, notebooks and electronic cameras, there are many more reasons why low power is paramount:

- Some applications have legal restrictions on power consumption like gas meters (to avoid a spark causing an explosion), electricity metering to avoid unnecessary loading of the mains network or fixed telecommunication equipment that is powered off the line
- other applications can draw much current under normal conditions but have to run of a battery when mains fails, e. g. security systems and cash registers
- Some car electronics must keep up a minimum level of activity while a car is parked, nevertheless the car battery must not be flat when the car is to be used again
- and last but not least, low power goes hand in hand with low radiation!

Numerous measures have been taken to allow H8/300H and H8S to meet all these demands:

- All derivatives are available in low voltage versions as well (except H8/3039). Low voltage operation not only significantly reduces power consumption, but also allows battery operation with a smaller number of cells and reduces radiation drastically, especially where external busses have to be used.
- All derivatives can be run off a slower clock, down to 2MHz. Power consumption will drop almost in proportion. A H8S/2246 for example will only draw appr. 4mA (typical) at 3V and at 2MHz with all the modules operating.

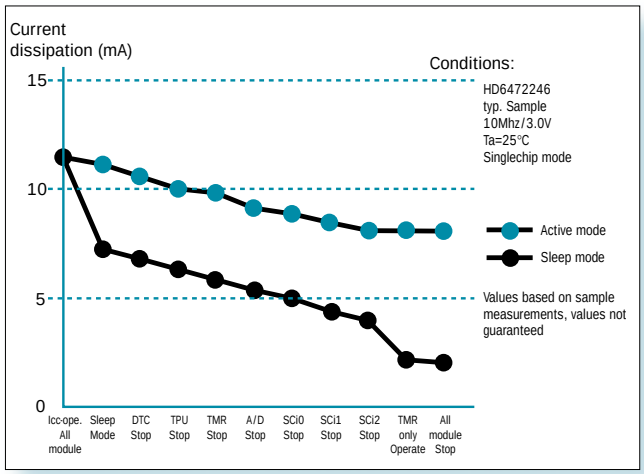


Figure 8

- The CPU can be stopped (sleep mode), with all the registers and memory contents being retained. Peripherals continue to operate and any interrupt will wake up the CPU instantly. Sleep mode reduces power consumption by about one third.
- Just like the CPU can be stopped at times of low activity, some H8/300H and all H8S derivatives allow to stop peripheral modules. For example, while the ADC is not needed the software simply clears the corresponding bit in the module stop register. Figure 8 shows how much current is saved per module for a H8S/2355 and also shows a curve for H8S/2246 with one module after the other being turned off. The lower curve shows the same, if the CPU is brought into sleep as well.
- Beyond the possibility to run H8/H8S off a slower clock statically, some H8/300H and all H8S offer the ability to dynamically reduce the clock internally ('clock gearing'). In case of H8/300H clock gearing effects the entire chip, so reduction will be almost proportional, in case of H8S clock gearing effects only bus masters (CPU, DMA, DTC) to avoid reprogramming of e. g. timers. The effect is shown in Figure 9.
- Some H8S derivatives also feature a 32KHz subclock, which allows to run the CPU, the 8-bit timers and the watchdogs at 32KHz ('subactive'), or just the 8-bit timers and watchdogs ('subsleep') or finally the watchdogs only ('watch mode'). In watch mode a periodical interrupt, which is generated from the subclock at a rate of once per second for example, wakes up the CPU. The CPU then checks system status (e. g. key pressed?) and then activates other modules or returns to sleep, as

DTC stop	0. 3mA
TPU stop	9mA
TMR stop	2mA
DAC stop	2. 2mA
ADC stop	2mA
each SCI stop	2mA

Sample data (not guaranteed), typical, at 5V /20MHz for a H8S/2355

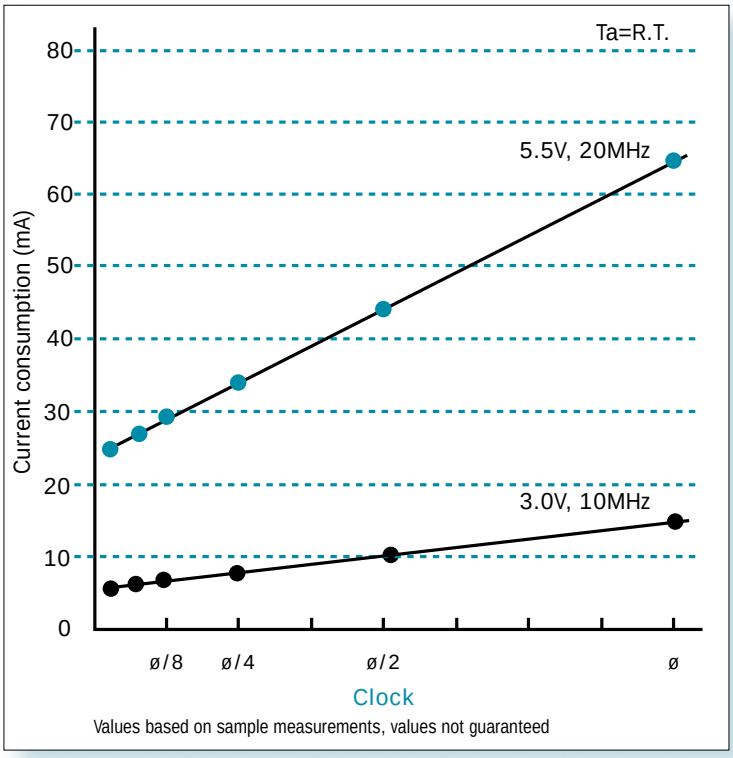
required. Hence, very low average power consumption can be achieved, even with a real time clock being implemented in software.

- If no activity is required, but RAM contents must be retained, H8/H8S microcontrollers can be brought into standby. In this mode the oscillator is stopped and power consumption drops to leakage current levels (0.01µA, typical at room temperature). Two modes are provided, software standby which allows to retain IO ports and hardware standby, which only retains RAM. RAM retention voltage is only 2V.

Some of these methods can be combined to achieve outstanding average power consumption values, while allowing high performance operation at times of high activity.

As an example for such a combination, let's assume the DTC would be used to move results of ADC conversions from the ADC to a RAM buffer (e.g. 64 Byte). The CPU does not need to process the data before acquisition of all data has finished. This scenario would allow to turn off all the modules, except the ADC and the DTC, and put the CPU into sleep during acquisition. The resulting current would be only appr. 3mA at 10MHz and 3V Vcc. After acquisition of all 64 Byte has ended, an interrupt wakes up the CPU to process the data. While doing so the software may choose to activate other peripheral modules as required. Please note that power consumption in this scenario could be further reduced if 10MHz clock gives more performance then needed. Typical Icc between 2mA and 3mA are possible.

Figure 9



Values based on sample measurements, values not guaranteed

Exceptions and **Interrupt** Controller

H8/300H and H8S feature a sophisticated interrupt system, that allows to respond quickly to asynchronous events. The worst case interrupt response time is 2. 6µs for H8/300H (at 16MHz) and 1. 5µs for H8S (at 20MHz). Because almost every interrupt source has its own vector, the interrupt service routine can immediately start to do some useful work, instead of polling status flags to find the cause of the interrupt. If two or more exceptions occur simultaneously, they are accepted and processed in order of priority. Software interrupts ('Trap') are accepted at all times, in the program execution state.

Interrupts are handled as follows:

- The PC and the CCR are pushed onto the stack
- The interrupt mask bits are updated
- A vector address corresponding to the exception source is generated, and program execution starts from that address

External interrupts (NMI and IRQ)

H8/300H and H8S have several external interrupts, including one non-maskable-interrupt (NMI). NMI can be programmed to be activated on either the rising or the falling edge. Interrupt request pins (IRQ) can be programmed to recognise either a low level or a low going edge on H8/300H, and on H8S can be programmed to recognise a low level, a rising or a falling edge or both edges.

Trap instruction exceptions (TRAPA)

These exceptions start when a TRAPA instruction is executed in program execution state. The TRAPA instruction has four vectors as specified by its argument. This exception can be used as an efficient mechanism for calling operating system functions, as it takes only 2 Byte to execute a TRAPA instruction, compared to 4 Byte for a BSR and 8 Byte for a JSR.

Interrupt Controller on H8/300H

The H8/300H interrupt controller can be operated in two modes, either maintaining compatibility with the standard H8/300 interrupt controller, or in a more advanced mode.

- **H8/300 compatible mode**
  In this mode the acceptance of maskable interrupts is controlled by the I-bit in the CCR. If I is set, then all interrupts are disabled (except NMI) and if I is cleared then all interrupts are enabled. When an interrupt is accepted, the controller automatically sets the I-bit, thus disabling any other maskable interrupts for the duration of the interrupt service routine (ISR), unless it is cleared by the users code.

- **H8/300H advanced mode**
  To increase the power of the interrupt controller, an extra interrupt status bit is included in the condition code register, known as the UI or User Interrupt bit. This extended operation allows the user to specify raised priority interrupt sources, which are capable of interrupting a low priority ISR which is already running. The priority of individual interrupt sources is programmed in a number of interrupt priority registers (IPR).

Interrupt controller on H8S

The interrupt controllers within the H8S family differ, depending on the particular H8S series. H8S/2655 has an interrupt controller that provides four modes (0...3) and the other series provide a subset.

- **Mode 0**
  This mode provides the mechanism known from H8/300. Acceptance is solely controlled by the I-bit.

- **Mode 1**
  In this mode acceptance is controlled by I and UI, thus providing functional compatibility with H8/300H.

- **Mode 2**
  This mode provides an 8-level priority mechanism controlled by bits I0. . I2 in the EXR register. Priorities for each interrupt source can be programmed in a set of IPR registers.

- **Mode 3**
  This mode combines mode 1 and 2, effectively providing up to 9 levels of priority.

H8S/265x derivatives can use modes 0. . 4, H8S/263x, H8S/23xx, H8S/223x and 222x can use modes 0 and 2, and H8S/224x and 21xx can use modes 0 and 1.

Memory **FLASH**

A traditional strength of Hitachi's microcontrollers are the large integrated memories and the advanced memory technology.

Already for many years, it has been an important strategy to provide microcontrollers with high-speed, on-chip Flash memory to the European market, always at the leading edge of this industry trend. This technology is now offered in its third generation, providing larger memory sizes and single-voltage programming. Hitachi is currently shipping over 4M Flash microcontrollers per month.

A table in the middle of this brochure shows Hitachi's 16-bit microcontrollers by ROM and RAM size, including 16 on-chip Flash derivatives. Please use the table to select the devices which meet your memory requirements.

Hundreds of customers worldwide have taken advantage of our flash based microcontrollers in their designs, about one third in industrial and automotive applications, approximately one fourth each in consumer and office automation and the remainder in telecommunications.

Integrating large and flexible memories has numerous benefits for our customers, some of which are becoming crucial in today's demanding electronics industry. For example: Switching an older microcontroller design, which uses external memory and peripherals, to a single-chip design, will drastically reduce radiation, because the address and data busses are a major source of radiation in a system. Together with the low power consumption of Hitachi's microcontrollers, such a redesign will often immediately eliminate radiation problems. At the same time costly shielding measures may become unnecessary, thus lowering system cost and board space requirements will become less.

Other benefits of large integrated memory and especially of on-chip Flash memory are:

- end of line programming allows flexibility in the software until shipment
- allows easy and fast update in the field without the need to open the equipment
- allows software updates even remotely, e. g. via modem/phone line
- fast response to changing customer requirements
- non volatile storage of data and parameters
- full availability of all ports, if external busses can be avoided
- full speed operation, often impossible or expensive if external memory is used

Flash programming

- **BOOT Mode**
  Boot mode is entered if the mode pins of a H8/H8S are in a certain state after reset. In boot mode program execution starts from a hidden ROM. The software in this ROM initialises one of the serial interfaces, downloads another piece of software (available from Hitachi, if desired), which then allows to (re)programme the Flash memory. Boot mode can be used to supply a blank (i. e. new) Flash device with a software, even when the device is already soldered onto the PCB.

- **USER Mode**
  User mode is not entered via reset. It is fundamentally just like normal operation, but with Flash programming enabled via the mode (usually FWE) pins.
  In user mode, an external trigger event causes the user software to copy a piece of code into RAM. Program execution then jumps to this code. The Flash can then be reprogrammed under the control of the user's application, using all the resources of the chip (i. e. downloading the new code does not necessarily have to use a serial interface, but could use any other resource). This mode is intended for Flash memory updates.

- **PROM Mode**
  All H8/H8S Flash derivatives can also be programmed using general purpose programming equipment, i. e. in the same way OTP's are programmed.

Bus State **Controller** (BSC)

As one of the key reasons for using the H8S and H8/300H is the 16MBytes linear address space, it will often be used in a system with a large amount of external memory. Consequently, H8S and H8/300H are supported by a powerful bus state controller (BSC) that allows external memory and/or peripherals to be connected with no (in some rare cases with little) glue logic. Also, the BSC helps to get the maximum performance out of any external devices, for example by avoiding address decode delays, where on-chip chip-select generation is used.

The BSC divides the memory space into 8 areas. For each of these areas a number of attributes is selectable, for example:

- the wait mode (automatic insertion or hardware protocol)
- the number of wait states
- the bus width (8/16-bit)
- DRAM access protocol for one area on 300H (=2Mbytes) and for 4 areas on H8S (=8Mbytes)(not on all devices)

Bus State Controller (BSC) on H8S

One of the major advantages of H8S over H8/300H is its basic instruction execution within a single clock cycle, that is only 50ns at 20MHz clock if executed from internal memory. In order to minimise the negative impact on performance when going off chip, every effort has been made to create a BSC with a maximum of throughput and flexibility.

Major enhancements include support for fast-page mode DRAM (on H8S/26xx and on some H8S/23xx derivatives), burst mode ROM, a write buffer that executes slow external write accesses independently (on H8S/26xx and on some H8S/23xx derivatives) and the improvement of read access time by moving the clock edge that latches the read data to the end of the bus cycle.

DRAM interface

Areas two to five can be set to interface directly to DRAM on on H8S/26xx and on some H8S/23xx derivatives, allowing up to 8MB of DRAM to be connected without any glue logic. The BSC handles the address multiplexing (8,9 or 10 bits), the timing and allows to use fast page mode. DRAM with CAS-before-RAS (CBR) or self-refresh are supported. For CBR refresh mode the BSC provides an independent refresh counter, so that no other timers have to be used.

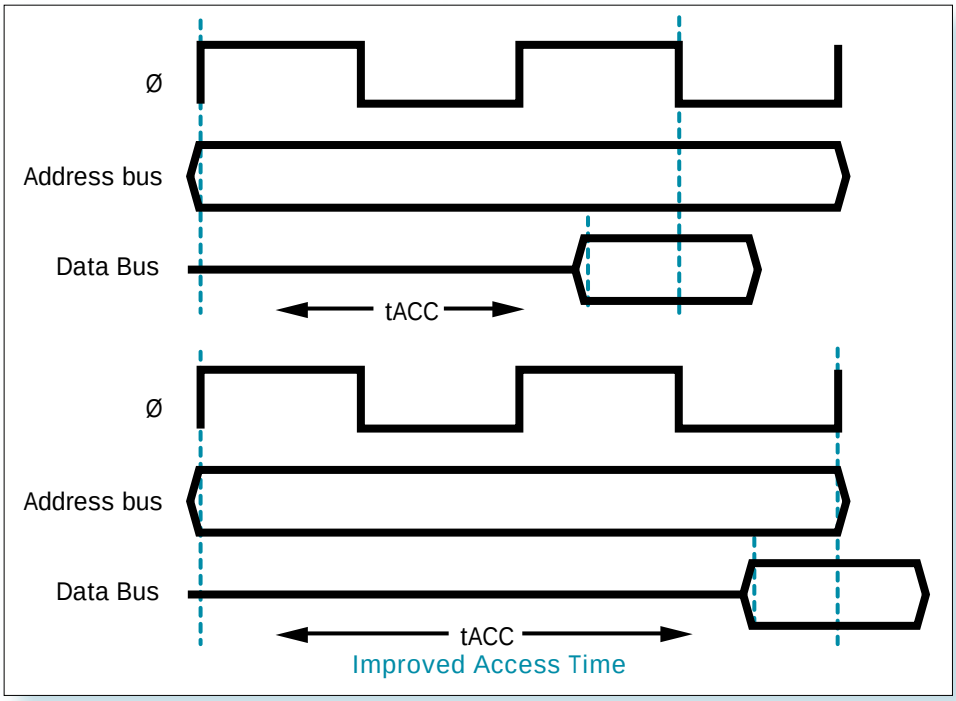


Figure 10

Improved read access timing

In order to give external devices a maximum of time to drive the required data onto the bus, the read access edge that latches the data, has been moved to the end of the cycle. Therefore read access time is improved by approximately one quarter, compared with H8/300H. Figures 10 & 11 illustrate this effect for several frequencies.

Write data buffer

On H8S/26xx and on some H8S/23xx derivatives, a write data buffer is provided. This feature allows the CPU to continue internal processing, while the BSC takes care of slow write accesses independently. Figure 12 shows an example of the timing when the write data buffer is used. When this function is activated, if an external write or DMA single address mode transfer continues for 2 states or longer, and there is an internal access next, only an external write is executed in the first state. But from the next state onward an internal access is executed in parallel with the external access, rather than waiting until it ends.

Bus release

On all H8S devices a mechanism is provided to allow external bus masters to obtain external bus ownership.
To request ownership an external master must drive the BREQ pin low. After the BREQ pins has been sampled low by the H8S, the address bus, data bus and the bus control pins are placed in a high impedance state and the Bus Acknowledge (BACK) signal is asserted to signal to the external master that the bus is now available. During bus release state internal processing continues as long as there is no external access. The internal bus master, wishing to access the external bus during bus release state, may use the BREQO signal to indicate to the external master that the bus ownership should be given back. The external bus master should respond by dropping BREQ. BREQO can also be used to signal that a refresh cycle for a DRAM is pending.

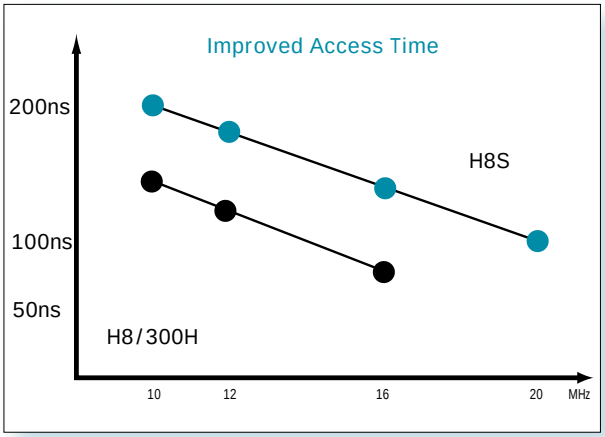


Figure 11

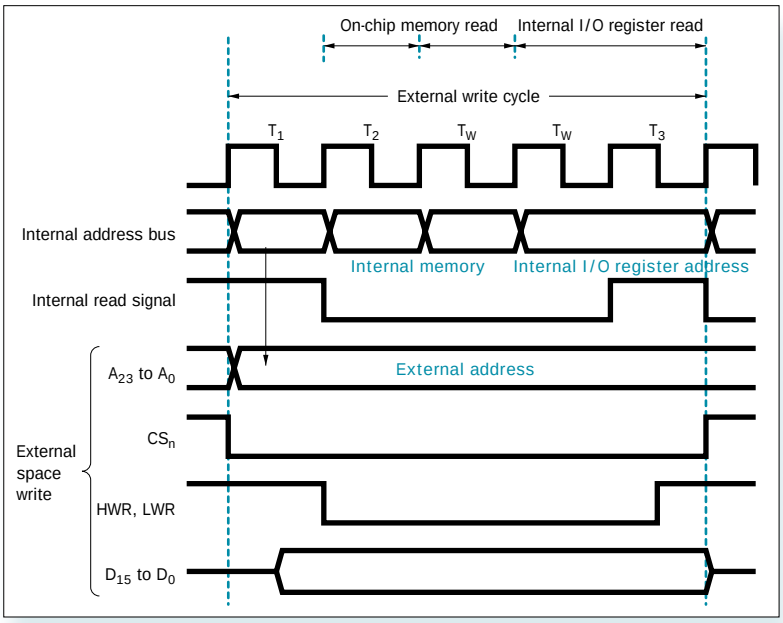


Figure 12

Direct Memory **Access** Controller (DMAC)

In a system with a high performance CPU and with large memory, a Direct Memory Access Controller will significantly increase system performance. Instead of wasting CPU performance to move data between peripherals and memory, virtually all of the CPU performance can be used for calculations, while the DMA handles the data transfers.

If combined with other peripherals, such as timers, SCI's or the real time outputs of the TPC/PPG, entire autonomous subsystems can be built, for example to drive stepper motors or to communicate with LCD modules or keyboards with hardly any CPU intervention.

As H8S almost triples the CPU performance of H8/300H, the DMAC on H8S has improvements over the H8/300H DMAC, in order to keep CPU and DMAC performance in a good balance. But let us first have a look at the common features:

- 4 channels in short address mode (used for transfers between internal IO and memory)*
- 2 channels in full address mode (used for transfers between memory and memory, or between external IO and memory)
- Byte or word transfer selectable
- address increment, decrement or fixed selectable, depending on mode
- DMA transfer request possible by timer, SCI0 and external request, depending on mode
- Interrupt request possible after each transfer or after specified number of transfers

* 8 channels on H8/3003

Some of the major improvements on H8S are:

- A special transfer mode has been added, single address mode, where both resources must be external and data is transferred in fly-by fashion for fastest transfer speed.
- More transfer request sources, e. g. A/D conversion end interrupt and at least 2 SCI can request a transfer

Short Address Mode

In this mode either the source or destination address is limited to only 8 bits (H8/300H) or 16 bits (H8S), with the upper bits being automatically set to logic '1'. This allows to access the internal IO registers. The other address is 24 bits wide, so that the entire memory space is accessible.
Within short address mode there is 'IO mode' (called sequential mode on H8S), where the full address can be automatically incremented or decremented, 'idle mode' with the full address being fixed and 'repeat mode', which allows cyclic data buffers to be automatically transferred. Cyclic data buffers are useful for many applications, e. g. to output a control pattern for a stepper motor.

Full Address Mode

To perform memory to memory transfers the full address mode can be used. Here, the source and destination addresses are 24-bits wide each, and therefore memory to memory transfer can be performed between any area of the full 16MBytes address space. This mode allows either a single transfer to occur per request ('normal mode'), or for a block of data to be moved ('block transfer mode'). In 'normal mode' and with 'auto-request' enabled, the DMAC can be set up in a burst mode, taking over the bus from the processor until all the transfers are complete, or in a cycle steal mode where the processor and the DMAC share the bus.

Single address mode (H8S)

Figure 13 illustrates the new single address mode. In single address mode a transfer of data is carried out directly between the data busses of two external devices, e. g. an external peripheral and DRAM. The advantage is the speed of the transfer, because the data is moved in a single cycle without a temporary storage. Either the source or the destination must be a device which can be accessed with a strobe alone, using the DACK pin. The address bus is used to access the other resource.

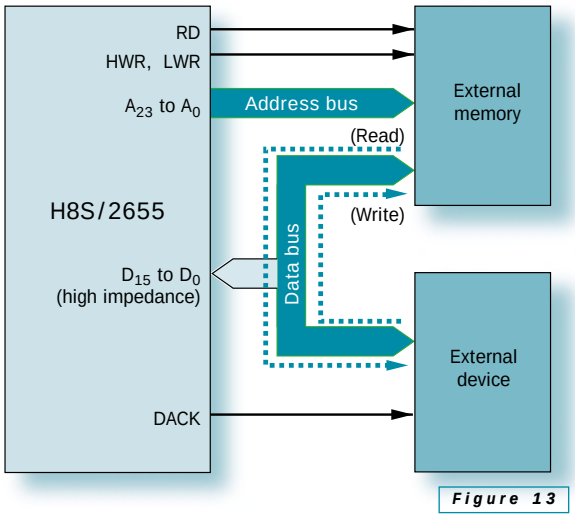


Figure 13

Data Transfer **Controller** (DTC)

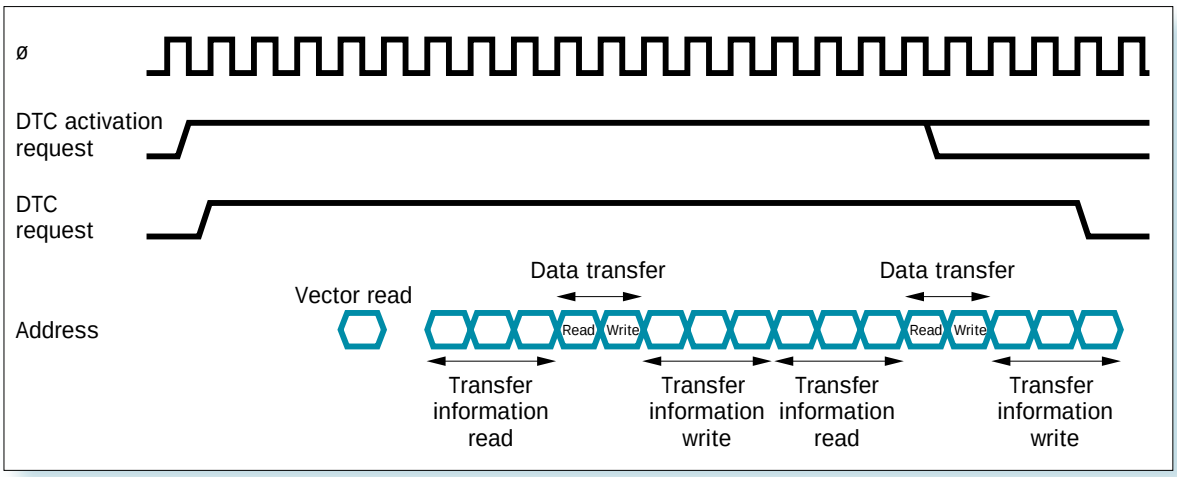
Analysis of many applications that use a DMAC has shown that a substantial part of these applications do not require the maximum speed of data transfers. These applications use a DMAC mainly to reduce CPU overhead, allowing the CPU to use its performance for calculations.

Therefore Hitachi conceived another peripheral to autonomously handle data transfers, the Data Transfer Controller (DTC). The DTC puts emphasise on offloading the CPU from data transfer tasks, while providing a maximum of flexibility. Unlike a DMAC the DTC can handle a very large number of transfer channels and transfers can be requested by almost any peripheral that can request an interrupt as well as by software. On the other hand a DTC transfer is approximately 5 times slower than a DMA transfer (1000ns as opposed to 200ns at 20MHz, assuming e. g. source is a peripheral and destination memory). In block transfer mode the DTC overhead is divided by the number of transfers within the block, thus practically eliminating the overhead penalty.

Also, a single trigger can request multiple transfers (chain mode).
This feature could, for example, be used to move the result of an analogue-to-digital conversion to a circular buffer in RAM, followed by automatic reprogramming of the ADC to perform other conversions. If the tasks given to the ADC are stored in a table in ROM, which is then used by the DTC in a round-robbing scheme, while the conversion results are stored in a corresponding number of circular buffers in RAM, the DTC and the ADC could perform a large set of completely different tasks without any CPU intervention whatsoever.
Figure 14 shows the timing of such a chain transfer. Please note that one cycle of phi is only 50ns at 20MHz. As can be seen, the DTC vector is read after a transfer request in only one cycle, each move of the transfer information between DTC RAM and DTC registers takes 3 cycles and the actual data transfers take 2 cycles (minimum).

The DTC could be seen as a DMAC with only a single channel implemented in hardware. The registers for the destination and source address, for the transfer mode and the transfer count actually exist only once. However, these registers are loaded with the information to be used for a particular transfer from RAM. That means that the structure of the DTC registers is mirrored in a special DTC RAM as many times as the designer has chosen to implement transfer channels. Each transfer can be specified to be byte- or word-wide, source and destination addresses can both be 24-bits wide (i. e. cover the full address range). Source and destination addresses can be either incremented or decremented (by 1 or 2), or can be fixed. A CPU interrupt can be requested for the interrupt that triggered the DTC transfer, either after each transfer or after the specified number of transfers have been performed.

Figure 14



Timer

One of the most important peripherals on any microcontroller is the timer unit. Timers have many uses in electronic systems. They trigger the task switch of real time operating systems, update software real time clocks, control AC, DC or stepper motors, check validity of external signals ('timeout'), count pulses for example from phase quadrature encoders and much more. Timers can even act as accurate digital-to-analog converters (DAC), if used as pulse-width-modulator (PWM).
In order to accommodate all these applications, Hitachi has developed 2 powerful and flexible timer units for their 16-bit microcontrollers, as well as several special-function timers, for example separate PWM timers, watch dog timers (WDT), low-power support timers, etc. These two timer units are the ITU on H8/300H, a 5-channel 16-bit timer unit with up to 10 input capture/output compare (IC/OC) and the TPU on H8S, a 6-channel 16-bit timer unit with up to 16 IC/OC.
An exception are the H8S/21xx devices. H8S/21xx is aimed on very cost sensitive application, where the advanced timer functionality of the ITU/TPU is either not needed or can be handled by the high performance H8S CPU instead. H8S/21xx has a 16-bit Free-Running-Timer (FRT) with 4 IC and 2 OC and 3 timers with 8-bit. A separate 14-bit PWM and 2 WDT (one with 32KHz subclock) are also provided.

Together with the large integrated memories and the other peripherals, these powerful timers are aimed at making single-chip systems possible, where previously microncontrollers with additional external devices had to be used. Hence, more money then is being spent on more powerful microcontrollers, could be saved on external devices, assembly cost, board space, power supply and on reduced counter measures against radiation. In particular, electronic systems which currently use 8-bit microcontrollers should be reconsidered under these aspects!

Integrated Timer Unit (ITU)

The ITU consists of five separate 16-bit timer channels, each of which can be clocked from an internal derivative of the system clock (ø, ø/2, ø/4 and ø/8) or from an external pin. If the ø clock option is selected, then the minimum resolution of the timer is 62. 5ns (ø = 16MHz). The standard timer functions provided by the ITU include ten general registers (GR), which can be used as output compares or input captures. A further four 16-bit buffer registers (BR) reduce the overhead placed on the CPU when servicing the timer block.

- **Output Compare Functions**
  To create output waveforms or timed interrupts, the ITU provides up to 10 output compare registers. The output compares work by producing an output of a pre-programmed level and/or an interrupt when the value in the counter matches the value stored in one of the output compare registers. The events that can be initiated by these compare matches are transitions on an output pin (to high, to low or toggle), a CPU interrupt (used for software timing functions), clearing the counter and the triggering of a DMA channel. Channels 3 and 4 allow to produce a pulse with duration down to one clock cycle (62. 5ns at 16MHz).

- **Input Capture Functions**
  The ITU provides up to 10 channels of input capture. In this mode the timer can be set up so that a transition on an input pin causes the value currently in the count register to be transferred into a capture register, thus time stamping that particular event. The ITU can be set to capture rising edges, falling edges and either of these. If required the timer unit can also clear the timer when the programmed external event occurs. The two buffer registers (BRA and BRB) provided in timer channels 3 and 4 can be used to buffer input time stamps. This allows events which occur very close to each other to be time stamped using one capture pin. This feature can also be used to measure the width of an incoming pulse, by programming the capture input to be triggered on both the rising and falling edges.
  By using input captures to measure the timing of external signals, very accurate measurements of variables such as frequency can be taken. The user can be sure that the accuracy of the measurement is not compromised by interrupt response time, as it is entirely a hardware driven facility.
  It is also possible to initiate DMA transfers when an input capture event occurs. This allows time stamps to be automatically placed in memory via the DMA controller, without needing to interrupt the CPU.

- **Timer Synchronisation**

  To allow timer channels in the ITU to be used in synchronisation, it is possible to set up two or more timers so that they are simultaneously written to via software and cleared by compare matches or input captures. When timer channels are put into this mode then their input and output events are also synchronised.

- **Standard PWM Mode**

  Each timer channel can be programmed to produce a single phase PWM output. Thus the ITU can output up to five separate channels of PWM. In this mode GRA controls the time when the pin goes high, and GRB when the pin goes low. Either GRA or GRB can be set to clear the counter, thus setting the frequency of the WM output.

- **AC Motor Control Outputs**

  To provide the PWM signals required to drive AC machines, the ITU provides two further PWM modes: Complementary 6-phase PWM and Reset Synchronised 6-phase PWM (shown in Figure 15). The main differences between these two modes are the transition points for the outputs and the provision of dead time between the phase outputs.

- **Phase Counting Mode**

  This mode finds use in servo control systems, where the position and speed feedback comes from a 2- phase quadrature encoder. In this type of encoder the waveforms output change their phase relationship depending on the direction of motion, as shown in Figure 16

The table below shows the PWM frequencies which can be obtained versus device clock speed and output resolution.

PWM Res.	16 MHz	12 MHz	10 MHz	8 MHz	6 MHz
14-bit	976. 5 Hz	732. 7 Hz	610 Hz	488 Hz	365 Hz
12-bit	3. 9 KHz	2. 9 KHz	2. 4 KHz	2 KHz	1. 5 KHz
10-bit	15. 6 KHz	11. 7 KHz	9. 7 KHz	7. 8 KHz	5. 8 KHz
9-bit	31. 2 KHz	23. 4 KHz	19. 5 KHz	15. 6 KHz	11. 7 KHz
8-bit	62. 4 KHz	46. 9 KHz	39 KHz	31. 3 KHz	23. 4 KHz
7-bit	124. 8 KHz	93. 8 KHz	78 KHz	62. 5 KHz	46. 8 KHz

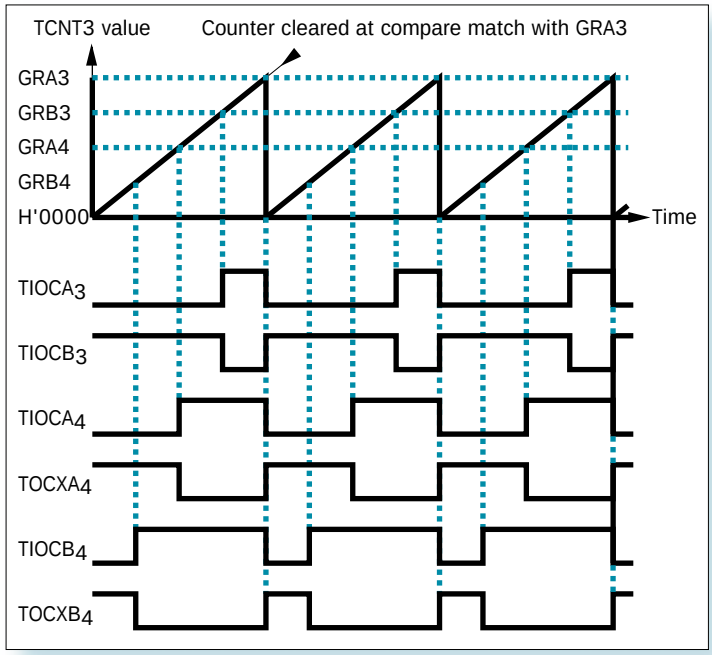


Figure 15

By utilising the phase counting mode on the ITU, TCNT2 will count up or down depending on the phase of the incoming signals. Therefore, the value of TCNT2 will reflect the positional changes experienced by the encoder.

This facility removes the requirement for extra hardware or interrupt handlers for position monitoring. In this mode the comparators of channel 2 can also be used to generate interrupts, for example when a certain position is reached.

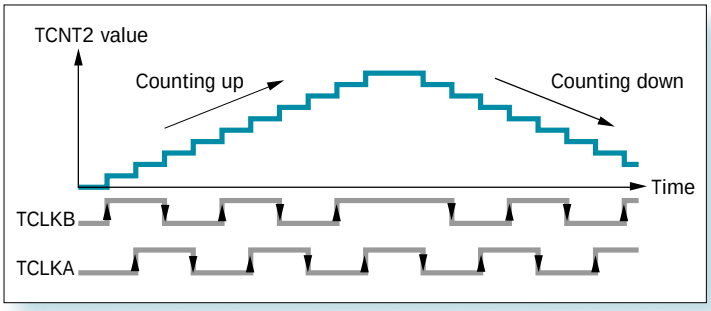


Figure 16

Modified ITU on H8/306x, H8/3006 and H8/3007

The ITU on H8/306x, H8/3006 and H8/3007 are modified to be more flexible. Channels 3 and 4 can be split into 4 timer channels (8-bit) instead of 2 timer channels (16-bit). However, this modified ITU does not have the special AC motor control modes (Complementary 6-phase PWM and Reset Synchronised 6-phase PWM). The buffering facility has also been removed.

Timer Pulse Unit (TPU)

The TPU is similar to the ITU, yet even more powerful and flexible. It is found on all H8S devices, with the H8S/224x and the H8S/222x devices having only half of a TPU implemented.
The TPU comprises six 16-bit timer channels with a total of 16 Timer General Registers (TGR), each of which can act either as an output compare or an input capture function. Some TGR's can also act as buffer registers to reduce the interrupt load that is put onto the CPU.
For each channel one out of eight input clocks can be selected in software. Possible sources are internal clocks, external clock pins or overflow of other timers, the latter effectively providing a method to cascade two 16-bit timers to form 32-bit timers.
While the ITU provides one channel for phase counting the TPU provides four. Also, the TPU allows to trigger an A/D conversion and can trigger data transfers by the Data transfer controller (DTC). The TPU allows to generate a 15-phase PWM signal, by using one TGR as the cycle register and the other 15 TGR's to set the duty.
However, as the ITU puts more emphasis on motor control and similar applications, the TPU does not support 'Reset synchronized 6-phase PWM mode' and 'Complementary 6-phase PWM mode'.

16-bit Free Running Timer (FRT)

The main timer unit of H8S/21xx is the 16-bit Free Running Timer (FRT), with 2 OC and 4 IC. The input capture facility can also be operated in buffered mode, with only 2 IC available in this case.
Input clock can be selected from 3 internal clocks and an external clock, which also allows event counting. The FRT unit features one independent interrupt for each IC, OC and one on overflow.

8-bit timers

The H8S/2655-series, H8S/2355 and 53, H8S/224x, H8S/234x and H8S/21xx all have an additional 8-bit timer module with two channels (TMR0 and TMR1). Each channel has two time constant registers (TCORA and TCORB) that are constantly compared with the counter value to detect compare matches. The 8-bit timer module can perform a variety of functions, including pulse output with an arbitrary duty cycle or counting events on an external pin.

The 8-bit timer module has the following features:

- Selection of internal clock phi/8, phi/64, phi/8192 or an external clock input.
- Selection of counter clear sources: compare match A or B, or external reset
- Cascading of both channels to form a 16-bit timer
- Channel 1 can also be used to count channel 0 compare matches

These 8-bit timers can also be used to keep up a minimum level of timer functionality in times of low activity of the overall system. The result is lowest power consumption on one hand, because the TPU can be switched off in that situation, but a minimum of timer activity on the other hand. The 8-bit timer could be used to update a software real time clock, for example, or scan a keyboard, so that the system can return to full activity when a key has been pressed.

Enhanced 8-bit timers on H8S/21xx

H8S/21xx derivatives feature a similar 8 bit timer module as described in the previous paragraph. However, it has a third 8-bit timer channel TMRY, which has similar functionality like TMR0 and TMR1, but no output pin that is under control of the compare match facility.

14 bit PWM timer

H8S/21xx is equipped with a two channel PWM timer, intended for use as a digital-to-analog converter. It is based on a 14-bit counter, thus enabling low-ripple, 14-bit resolution analog signals to be generated.

Watchdog Timer (WDT) on H8/300H

Often, a watchdog timer is a very important feature in any embedded application. It is used to ensure that any

"mishap' in the system (such as a noise induced software crash) is rectified as quickly as possible.
The principle behind a watchdog timer is very simple - a counter is constantly counting upwards, and correctly operating software ensures that this counter never overflows by continuously resetting the count. If the software crashes and the counter overflows, the watchdog "barks" and sends some stimulus to the microcontroller (normally a reset) to restart system operations in a controlled manner.
All H8/300H devices are equipped with a timer, which can be used either as a watchdog or as an interval timer. Its 'bark' is a reset if it is used as a watchdog. If used as interval timer, each overflow generates an interrupt.

Watchdog Timer (WDT) on H8S

The WDT on H8S has some improvements over the WDT on H8/300H.
It has an WDTOVF-pin that can signal the watchdog overflow to the outside world. It can select much slower clock sources up to phi/131072, which allows up to 1. 68s (at 20MHz) for the software to reset the watchdog before overflow.

Watchdog Timer (WDT) operating on 32KHz subclock

On some H8S derivatives a second WDT is implemented, which is operating off a 32KHz subclock. This subclock can be divided by 2 to 256 before it is used as counter input clock. Hence, the final overflow rate can be as low as 32KHz divided by 256x256 = once every two seconds. This WDT can request an interrupt, reset or NMI. If an interrupt is requested this WDT is useful to update a software real time clock. For this usage, every peripheral module on the device is turned off and the CPU is brought into sleep mode. Then the WDT wakes up the CPU every second, for example, the CPU updates the the software real time clock registers (usually kept in RAM) and goes to sleep again, if no other activity is pending.

Timing Pattern **Controller** (TPC) Programmable Pulse **Generator** (PPG)

These peripherals allow to generate digital output signals in synchronisation with a timer pulse, so that one could look at them as 'real time outputs'. Such a timer-driven digital output system allows to generate a continuous stream of data that appears on the pins precisely in the intervals that the timer is programmed to, without any 'jitter' that would be caused by e. g. interrupt latencies in a system where an interrupt service routine drives the pins. Also the TPC and PPG allow to do this without any CPU intervention, if used together with DMA.

The TPC and PPG provide registers called the 'Next Data Register'. The data in these registers will be transferred under timer control to the 'Port Data Registers' (i. e. to the pins). The CPU, the DMA or the DTC (where applicable) then have time until the next 'timer tick' to copy the next value from a data table in memory to the 'Next Data Register'. This mechanism works independently for four groups of four pins each, so that a total of 16 pins can be driven in that way.

The TPC and the PPG are first of all intended to drive stepper motors (up to four) with only very little CPU intervention required. However, they can be used in many different ways as well. It is quite easy, for example, to generate a serial data stream if an additional serial interface is required. It is even possible to drive an LCD module without using any LCD timing controller, thus eliminating a entire peripheral chip in a microcontroller system that is to be connected to an LCD module. Such an application is described in Hitachi's application note No. 55 (using Hitachi's SH microcontroller). Hitachi's application note No. 56 shows how to set up such a TPC/ITU/DMA system using MakeApp.

Stepper Motor Control with the TPC

Figure 17 shows how stepper motor control can be performed using the ITU, TPC and DMAC . In this example a two phase stepper motor is being driven, using complementary transistors. It is therefore necessary to provide a dead time between the switching of the phases to eliminate any short circuit conditions between the high side and low side drivers.

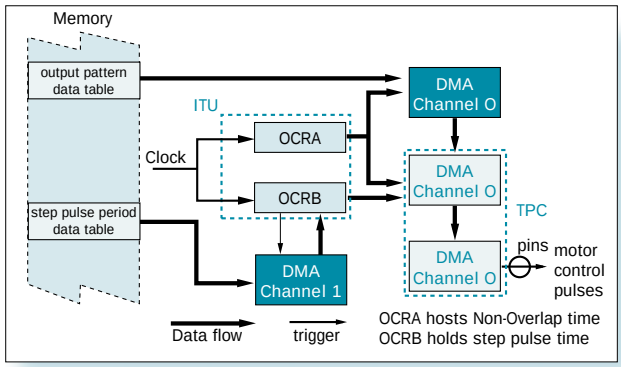


Figure 17

Using compare matches from the ITU to stimulate the DMAC, new pattern data is provided to the TPC. This pattern data represents the next phase drive pattern required, and is stored in a memory table. The DMAC uses its memory to I/O function to transfer this data on each compare match. The TPC also uses the stimulus from the ITU to transfer the contents of the NDR to the port. Using a TPC mode where transitions on the port from 0 to 1 (i. e. switching on a phase) are only made on compare match A, a dead time, equal to the value in GRA, is inserted.

When controlling a stepper motor, providing the phase patterns onto the port pins is only part of the story. It is also necessary to modify the time between new patterns being output to allow acceleration and deceleration of the motor as shown by the velocity profile.

When the TPC, ITU and DMAC are working together, the acceleration and deceleration phases, as well as the steady speed phase can be controlled with minimal CPU overhead. The CPU only needs to get involved when a transition from one phase to another is made. This is achieved by using a second memory to I/O DMA channel to reload the timer compare register after each new pattern has been output. Again the DMAC can take the next step period data from a table of values stored in the memory of the system. Therefore, by providing a table of increasing or decreasing values the motor can be decelerated or accelerated with no CPU intervention (Figure 18).

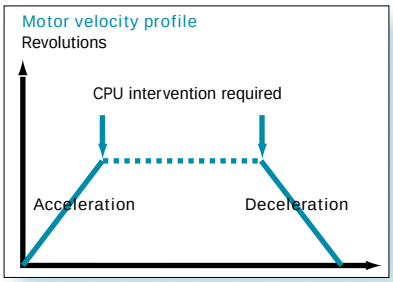


Figure 18

Differences between H8/300H TPC and H8S PPG

The difference between the H8/300H TPC and the H8S PPG is mainly the addition of the bit inversion to each output.

Also, the PPG is supported by the H8S DMA as well as the DTC.

Serial Communications **Interface** (SCI)

This form of communication has many uses in microcontroller applications, such as inter-device communications, diagnostics, host communication or as an interface to peripherals. All of Hitachi's 16-bit microcontrollers have at least one SCI, even though most have two or more. The SCI's on H8/300H and H8S can operate in asynchronous ('UART') or synchronous mode.

They have independent baud rate generators, so that none of the general purpose timers is used up to generate transmit/receive clocks, and external clocking is also possible. They are double buffered to allow 'back-to-back' transmission. Break detection is possible by reading the RxD pin level after a framing error has been detected.
To allow efficient SCI service by interrupt service routines each SCI is provided with 4 different interrupts, each with its own interrupt vector. These are transmit-data-empty, transmit-end, receive-data-full and receive error. Receive data errors are trapped using three error conditions -overflow, framing and parity. These three errors are indicated via one interrupt vector and three status flags in the serial status register.

Some other capabilities vary from family to family, as shown in the table.

The maximum bit rate in asynchronous operation is 625kbit/s at 20MHz for H8/300H and 781kbit/s at 25MHz for H8S, using the internal BRR. Using external clocks the values for asynchronous mode are half of that. For synchronous operation with external clock the bit rate is 3.33Mbit/s at 20MHz for H8/300H and over 4Mbit/s at 25MHz for H8S.

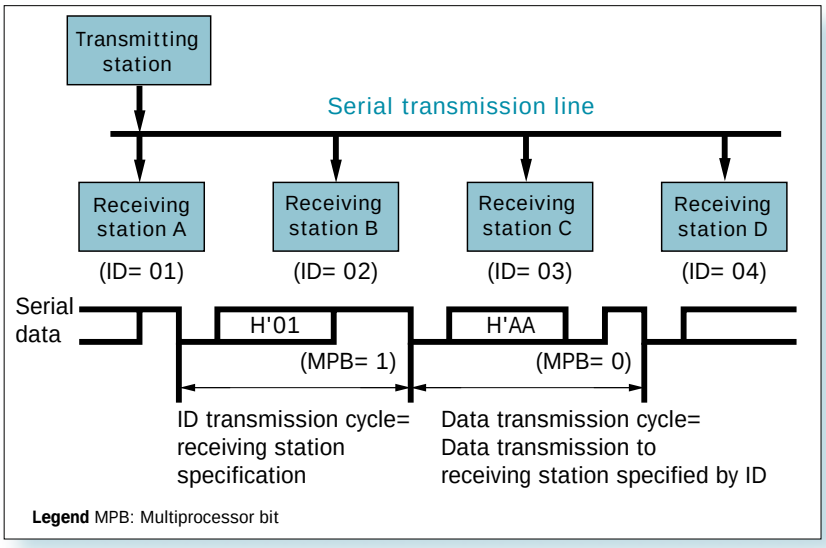
	H8/300H	H8S	H8S/21xx
Smart card interface (ISO 7816)	H8/3048 series	Yes	No
Multi-processor mode	Yes	Yes	Yes
IIC	No	H8S/2238 H8S/2633	H8S/21x7, 8
IrDA	No	H8S/2633	Yes
LSB/MSB-first selectable*	No	Yes	Yes
No. of SCI with DMA support	1	min. 2	No
DTC support	No	Yes	H8S/21x7, 8

* This feature allows to connect SPI compliant peripherals in most cases.

The H8S and the H8/300H serial ports also support multiprocessor communications using a master slave configuration in addition to the standard modes.

In this mode, communication between devices is performed using an additional multiprocessor bit (MPB) which is added to the data transmitted. This bit is used to differentiate between data frames and address frames. Thus, any frame sent from the master with the MPB set to one can be used to activate the required slave.
Slave devices on this network will only produce a receive interrupt when a frame is received with the MPB set, so the interrupt handler can check the address which has been transmitted.

Figure 19



Memory Type and Size

RAM \ ROM	0	16K	32K	48K	64K	96K	128K	192K	256K	512K
512 Byte	H8/3001 H8/3002 H8/3003	H8/3030 H8/3036								
1K			H8/3031 H8/3037							
2K	H8/3004 H8/3006 H8/3040* H8/3044* H8S/2350 H8S/2340 H8S/2310		H8/3040 H8/3044 H8S/2341 H8S/2130 H8S/2126 H8S/2120	H8/3041	H8/3032 H8/3038 H8/3042 H8/3045 H8/3060 H8/3065 H8S/2351 H8S/2343 H8S/2147 H8S/2142F H8S/2137 H8S/2132F H8S/2127 H8S/2122					
4K	H8/3005 H8/3007 H8S/2655* H8S/2240		H8S/2241		H8S/2653 H8S/2243 H8S/2233 H8S/2223	H8/3047 H8/3061 H8S/2143 H8S/2133 H8S/2123	H8/3033 H8/3039F H8/3020 H8/3048F H8/3062F H8/3067F H8S/2655 H8S/2345F H8S/2245 H8S/2235 H8S/2225 H8S/2148F H8S/2144F H8S/2138F H8S/2134F H8S/2128F H8S/2124	H8/3034	H8/3035	
8K	H8S/2352 H8S/2322 H8S/2312 H8S/2242*		H8S/2323 H8S/2242		H8S/2244		H8S/2357F H8S/2327 H8S/2246 H8S/2236	H8/3021	H8/3022F (UD) H8S/2676F (UD) H8S/2328F	H8/3052F (UD)
12K									H8S/2623F	
16K							H8S/2237 H8S/2227		H8S/2633F H8S/2238F	

H ROM-LESS or pseudo ROM-LESS(*)

H OTP and Mask

(UD) Under Development

H Mask-ROM

H Flash and Mask (H8S/2623,33 Flash only)

(UD) Under Development

	Device	H8/3001	H8/3002	H8/3003	H8/3004,5	H8/3006,7	H8/3020,1,2 (UD)
Memory	ROM (byte)	-	-	-	-	-	128,192,256k
	RAM (byte)	512	512	512	2,4k	2,4k	4,4,8k
	OTP (HD647...) or FLASH (HD64F...)	-	-	-	-	-	HD64F3022
Vcc/Clock	Vcc (V) / clock (MHz)	4.5-5.5/16	4.5-5.5/16	4.5-5.5/16	4.5-5.5/16	4.5-5.5/20	3.0-3.6/18
	(During Operation)	3.0-5.5/13	3.0-5.5/10	3.0-5.5/10	4.5-5.5/18	3.0-5.5/13	
		2.7-5.5/8	2.7-5.5/8	2.7-5.5/8	3.0-5.5/10	2.7-5.5/10	
					2.7-5.5/8		
	Flash Programming Voltage (V)						Vcc=3.0-3.6
	External data bus (bit)	8/16	8/16	8/16	8	8/16	8
Timer	ITU / TPU / FRT (16-bit timer)	5	5	5	5	3	5
	no of input capture/output compare	10 IC/OC	10 IC/OC	10 IC/OC	10 IC/OC	6 IC/OC	10 IC/OC
	8-bit timer	-	-	-	-	4 with 2 IC / 4 OC	-
	Watchdog timer	-	1	1	1	1	1
	14-bit PWM (channel)	-	-	-	-	-	-
Bus Master	DMAC (channels) Memory to/from I/O	-	4	8	-	4	-
	Memory to Memory	-	2	4	-	2	-
	DTC	-	-	-	-	-	-
Serial Communication	SCI (async/sync channels)	1	2	2	1	3	2
	Smart card i/f (channels)	-	-	-	-	3	2
	IIC (channels)	-	-	-	-	-	-
	IrDA (channels)	-	-	-	-	-	-
	CAN V2.0B (channels)	-	-	-	-	-	-
Analog	10-bit ADC (channels)	4	8	8	8	8	8
	8-bit DAC (channels)	-	-	-	-	2	-
Other Features	TPC (bit) / PPG (bit)	12	16	16	-	16	15
	Refresh controller /DRAM interface	-	Yes	Yes	-	Yes	-
	Chip select pins	-	4	8	-	8	-
	Interrupts Internal	20	30	34	21	36	25
	External	4	7	9	6	7	5
	I/O pins (incl. input only pins)	32	46	58	32	79	63
	Others						
	Data book	21-092	21-078	21-033A	21-106	21-117	TBA
	Package	FP-80A	FP-100B	FP-112	FP-80A	FP-100B	FP-80A
		TFP-80C	TFP-100B	TFP-120	TFP-80C	TFP-100B	TFP-80C

** For availability of mask ROM versions, please contact your Hitachi sales office or authorized distributor

G u i d e

H8/3030,1,2	H8/3033,4,5	H8/3036,7,8,9	H8/3040,1,2	H8/3044,5,7,8	H8/3052 (UD)	H8/3060,1,2	H8/3065,6,7	H8S/2120,2,3,4,6,7,8**
16,32,64k	128,192,256k	16,32,64,128k	32,48,64k	32,64,98,128k	512k	64,96,128K	64,96,128K	32,64,128,96,32,64,128k
512,1k,2k	4k	512,1,2,4k	2k	2,2,4,4k	8k	2,4,4k	2,4,4k	2,2,4,4,2,2,4k
HD6473032	HD6473035	HD64F3039	HD6473042	HD6473048 HD64F3048	HD64F3052	HD64F3062	HD64F3067	HD64F2128
4.5-5.5/16 3.0-5.5/10 2.7-5.5/8	4.5-5.5/18 3.0-5.5/10 2.7-5.5/8	4.5-5.5/18 3.0-5.5/10 2.7-5.5/8* (* mask only) Vcc=3.0-3.6 or 4.5-5.5	4.5-5.5/16 3.0-5.5/10 2.7-5.5/8	4.5-5.5/16 3.15-5.5/13* 2.7-5.5/8 (* mask/OTP only) Vpp=12V	3.0-5.5/18 Vcc=3.0-3.6	4.5-5.5/20 3.0-5.5/13 2.7-5.5/8* (* mask only) Vcc=3.0-3.6 or 4.5-5.5	4.5-5.5/20 3.0-5.5/13 2.7-5.5/8* (* mask only) Vcc=3.0-3.6 or 4.5-5.5	4.5-5.5/20 2.7-5.5/10* (* mask only) Vcc=4.5-5.5
8	8	8	8/16	8/16	8/16	8/16	8/16	8
5 10 IC/OC	5 10 IC/OC	5 10 IC/OC	5 10 IC/OC	5 10 IC/OC	5 10 IC/OC	3 6 IC/OC	3 6 IC/OC	1 4 IC / 2 OC
-	-	-	-	-	-	4 with 2 IC / 4 OC	4 with 2 IC / 4 OC	3 on 2120,2,3,4 4 on 2126,7,8
1	1	1	1	1	1	1	1	2
-	-	-	-	-	-	-	-	2 on 2126,7,8
-	-	-	4	4	4	-	4	-
-	-	-	2	2	2	-	2	-
-	-	-	-	-	-	-	-	1 on 2126,7,8
1	1	2	2	2	2	2	3	2
-	-	1	-	1	2	2	3	-
-	-	-	-	-	-	-	-	2 on 2126, 7, 8
-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-
8	8	8	8	8	8	8	8	8
-	-	-	2	2	2	2	2	-
16	16	15	16	16	16	16	16	-
-	-	-	Yes	Yes	Yes	-	Yes	-
-	-	-	4	8	8	8	8	-
21	21	25	30	30	30	27	36	29 (33 on 2126,7,8)
6	6	5	7	7	7	7	7	4
63	63	63	78	78	78	79	79	51
			3040x00 pseudo ROM-less avail.	3044x00 pseudo ROM-less avail.				ADC 16ch x6bit mode subclock mode
21-093	21-111	21-114	21-036	21-095A	TBA	21-116	21-115	18-016
FP-80A TFP-80C	FP-80A TFP-80C	FP-80A TFP-80C	FP-100B TFP-100B	FP-100B TFP-100B	FP-100B TFP-100B	FP-100B TFP-100B	FP-100B TFP-100B	DP-64S FP-64A, TFP-80C

H8S/2130,2,3,4,7,8**	H8S/2142,3,4,7,8**	H8S/2223,5,7	H8S/2233,5,7	H8S/2238	H8S/2240,1,2,3,4,5,6	H8S/2310,2	H8S/2322,3,7,8	H8S/2340,1,3,5	H8S
32,64,96,128,64,128k	64,96,128,64,128k	64,128,128k	64,128,128k	256k	0,32,32,64,64,128,128k	-	0,32,128,256k	0,32,64,128k	
2,2,4,4,2,4k	2,4,4,2,4k	4,4,16k	4,4,16k	16k	4,4,8,4,8,4,8k	2,8k	8k	2,2,2,4k	
HD64F2138 (128k) HD64F2134 (128k) HD64F2132 (64k)	HD64F2148 (128k) HD64F2144 (128k) HD64F2142 (64k)	HD6472237	HD6472237	HD64F2238	HD6472246	-	HD64F2328	HD6472345 HD64F2345	
4.5-5.5/20 2.7-5.5/10 Mask 3.0-5.5/10 Flash Vcc=3.0-3.6 or 4.5-5.5	4.5-5.5/20 2.7-5.5/10 Mask 3.0-5.5/10 Flash Vcc=3.0-3.6 or 4.5-5.5	2.7-3.6/13 2.2-3.6/6* (* mask only)	2.7-3.6/13* 2.2-3.6/6* 2.7-3.6/10 (* mask only)	2.7-5.5/13 2.2-3.6/6* (* mask only) Vcc=2.7-5.5 or 2.7-3.6	4.5-5.5/20 2.7-5.5/13* 2.7-5.5/10 (* mask only)	2.7-3.6/20 3.0-3.6/25	2.7-3.6/20 3.0-3.6/25 Vcc=2.7-3.6	4.5-5.5/20 2.7-5.5/10* (*mask/OTP only) Vcc=4.5-5.5	4.5 2.7
8	8/16	8/16	8/16	8/16	8/16	8/16	8/16	8/16	
1 4 IC / 2 OC	1 4 IC / 2 OC	3 8 IC/OC	6 16 IC/OC	6 16 IC/OC	3 8 IC/OC	6 16 IC/OC	6 16 IC/OC	6 16 IC/OC	16
3 on 2130,2,3,4 4 on 2137,8	3 on 2142,3,4 4 on 2147,8	2 with 2 OC	2 with 2 OC	4 with 4 OC	2 with 2 OC	2 with 2 OC	2 with 2 OC	2 with 2 OC	
2	2	2	2	2	1	1	1	1	
2	2	-	-	-	-	-	-	-	
-	-	-	-	-	-	-	4	-	
-	-	-	-	-	-	-	2	-	
1 on 2137,8	1 on 2147,8	Yes	Yes	Yes	Yes	Yes	Yes	Yes	
3	3	3	4	4	3	2	3	2	
-	-	3	4	4	3	2	3	2	
2 on 2137, 8	2 on 2147, 8	-	-	2	-	-	-	-	
1	1	-	-	-	-	-	-	-	
-	-	-	-	-	-	-	-	-	
8	8	8	8	8	4	8	8	8	
2	2	-	2	2	-	2	2	2	
-	-	-	-	-	-	-	16	-	
-	-	-	-	-	-	-	Yes	-	
-	-	8	8	8	8	8	8	4	
31 (43 on 2137,8)	34 (46 on 2147,8)	36	53	53	34	43	52	37	
9	9	9	9	9	9	9	9	9	
66	82	82	82	82	79	79	95	79	
ADC 16ch x6bit mode subclock mode	ADC 16ch x6bit mode subclock mode	32KHz subclock	32KHz subclock	internal step down 32KHz subclock	2242x00 pseudo ROM-less avail.				
18-018	18-017	18-012	18-012	18-020	18-004	TBA	18-021/22	18-010	1
FP-80A TFP-80C	FP-100B TFP-100B	FP-100A, FP-100B TFP-100B TFP-100G	FP-100A, FP-100B TFP-100B TFP-100G	FP-100A, FP-100B TFP-100B TFP-100G	FP-100B TFP-100B	FP-100A TFP-100B	FP-128 TFP-120	FP-100A, FP-100B TFP-100B, TFP-100G	F TF

/2350,1	H8S/2353,5	H8S/2352,7	H8S/2623, H8S/2626	H8S/2633**	H8S/2653,5	Device	
0,64k	64,128k	0,128k	256k	256k	64,128k	ROM (byte)	Memory
2k	2,4k	8k	12k	16k	4k	RAM (byte)	
-	HD6472355	HD6472357 HD64F2357	HD64F2623 HD64F2626	HD64F2633	HD6472655	OTP (HD647...) or FLASH (HD64F...)	
5-5.5/20 7-5.5/10	4.5-5.5/20 2.7-5.5/10	4.5-5.5/20 2.7-5.5/10* 3.0-5.5/13 Flash (*mask/OTP only) Vcc=3.0-3.6 or 4.5-5.5	3.0-3.6/20 (Vcc) 4.5-5.5/20(PVcc) Vcc=3.0-3.6	3.0-3.6/25 (Vcc) 4.5-5.5/25(PVcc) Vcc=3.0-3.6	4.5-5.5/20 2.7-5.5/10	Vcc (V) / clock (MHz) (During Operation) Flash Programming Voltage (V)	Vcc/Clock
8/16	8/16	8/16	8/16	8/16	8/16	External data bus (bit)	
6	6	6	6	6	6	ITU / TPU / FRT (16-bit timer)	Timer
6 IC/OC	16 IC/OC	16 IC/OC	16 IC/OC	16 IC/OC	16 IC/OC	no of input capture/output compare	
-	2 with 2 OC	2 with 2 OC	-	4 with 4 OC	2 with 2 OC	8-bit timer	
1	1	1	1	2	1	Watchdog timer	
-	-	-	-	4	-	14-bit PWM (channel)	
4	-	4	-	4	4	DMAC (channels) Memory to/from I/O	Bus Master
2	-	2	-	2	2	Memory to Memory	
Yes	Yes	Yes	Yes	Yes	Yes	DTC	
2	3	3	3	5	3	SCI (async/sync channels)	Serial Communication
2	3	3	3	5	3	Smart card i/f (channels)	
-	-	-	-	2	-	IIC (channels)	
-	-	-	-	1	-	IrDA (channels)	
-	-	-	1	-	-	CAN V2.0B (channels)	
8	8	8	16	16	8	10-bit ADC (channels)	Analog
2	2	2	-	4	2	8-bit DAC (channels)	
16	-	16	8	8	16	TPC (bit) / PPG (bit)	Other Features
Yes	-	Yes	-	Yes	Yes	Refresh controller /DRAM interface	
8	8	8	-	8	8	Chip select pins	
42	41	52	47	72	52	Interrupts Internal	
9	9	9	7	9	9	External	
95	95	95	70	89	95	I/O pins (incl. input only pins)	
			PLL clock H8S/2626: 32KHz subclock	PLL clock 32KHZ subclock	2655x00 pseudo ROM-less avail.	Others	
8-006	18-005	18-011	TBA	TBA	18-001B	Data book	
P-128 FP-120	FP-128 TFP-120	FP-128 TFP-120	FP-100B	FP-128 TFP-120	FP-128 TFP-120	Package	

In **Brief**

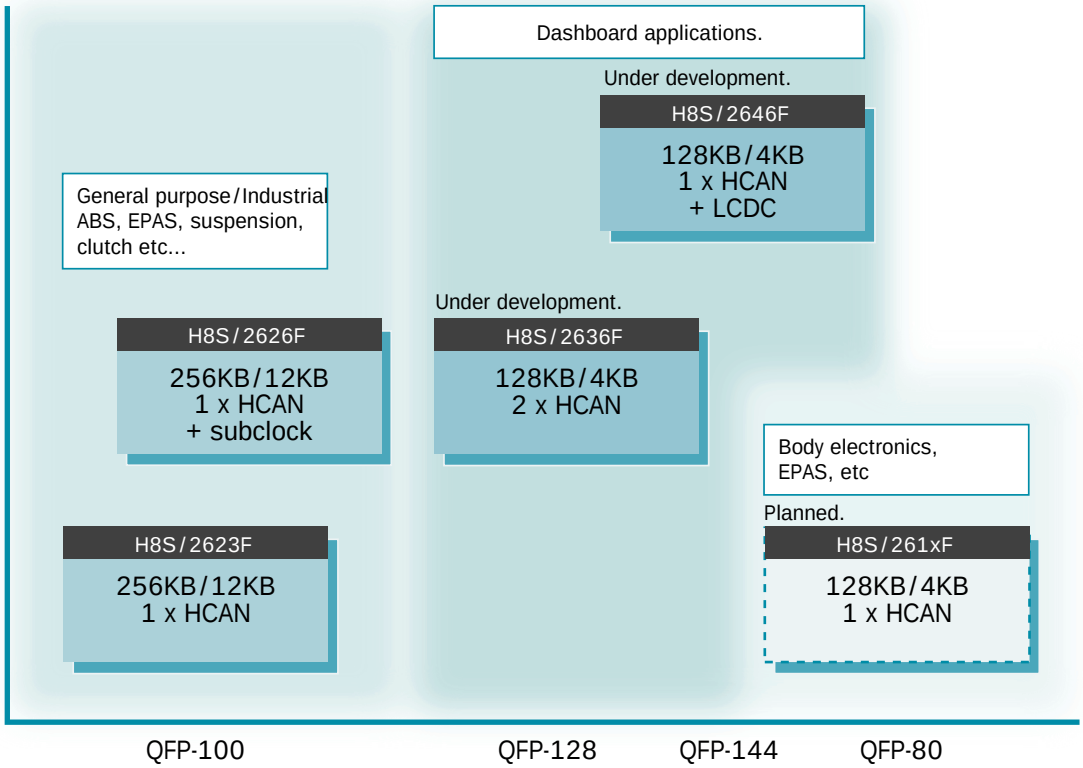
In this brochure an overview is given as to why H8S and H8/300H give you the technical benefits that are demanded by today's applications. The purpose is to give you enough insight into the features of the H8S and H8/300H family to see how you can benefit from the performance, the rich set of peripherals and the memory options available. To summarise this:

- High performance CPU with architecture tailored for high level language software development
- Industry leading low power, low voltage options
- Memory line up from 16K to 256K ROM and 512Byte to 16K RAM, including many Flash versions up to 256K Flash
- Very powerful and sophisticated peripherals designed to reduce CPU overhead and hence to increase system performance
- High memory and peripheral integration to allow single-chip systems, where previously multi-chip systems were necessary. Switching from multi-chip to single-chip will drastically reduce radiation, board space requirements and enables the usage of all pins as ports instead of using them as busses.
- Full European technical and tool support provided by Hitachi Microsystems Europe (HMSE) in Maidenhead (UK)

There is a strong road map that underlines Hitachi's commitment to H8 as an architecture that will be a dominant player in the industry for many years to come. The road map points towards:

- 33MHz at 3.3V H8S devices by the second half of 2000
- more large memory variants (up to 512K Flash) within year 2000
- high-speed Flash as a standard ROM technology, as price is decreasing to fall from OTP levels towards mask
- further decrease in power consumption by shifting Vcc to 2.2V and by adding 32kHz subclock
- future peripherals including 2x CAN-derivatives, high-current stepper motor drivers, on-chip LCDC and much more. As an example the road map below shows Hitachi's 16-bit microcontrollers with integrated CAN.

H8S & CAN derivatives



Smart card interface mode (SIM)

In this mode the SCI conforms to a sub-set ISO7816-3. This standard is used to communicate with so called smart cards, which are frequently used in banking applications (electronic money), GSM phones and many other applications like building entry control or for 'loyalty cards'. Because these applications are expected to grow very rapidly in the next few years, Hitachi has equipped all H8S devices with SCI's that can be set to SIM mode.

According to ISO 7816-3, the communication used is asynchronous, half-duplex (i. e. only either the host or the smart card transmits at a time) and with even parity always. Also, after transmission of the data and within the time normally used as stop bits, ISO7816-3 implements an error bit. That means, that a low level on the RxD/TxD line at a particular position after the data bits has to be recognised by the transmit side as an error in reception on the receive side. The transmitting side shall respond by retransmitting the last data. The SCI in SIM mode also supports direct and inverse convention as set out by ISO 7816-3.

The physical interface between the host and the smart card comprises the RxD/TxD pins tied together and then connected to the I/O pin of the smart card, a clock that must be provided to the smart card and initially has to be 372 times the baudrate and a reset signal. Reset is not tied to the reset pin of the host microcontroller, but is connected to a general purpose IO pin of the host, thus putting the smart card's reset under host software control.

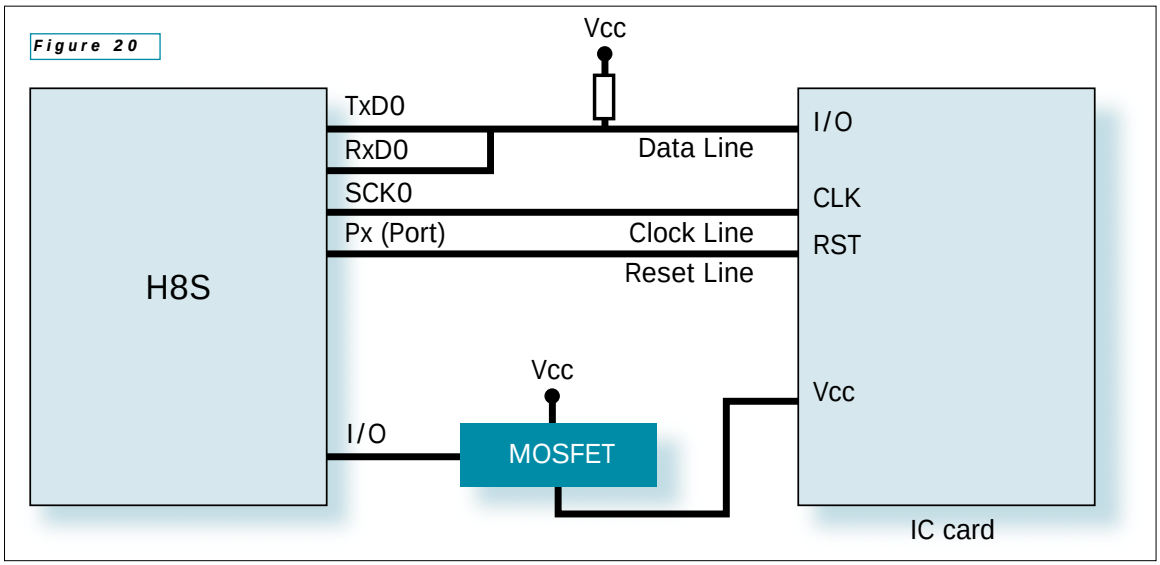
Also, a general purpose IO of the host is used to control a MOSFET that turns on and off the power to the smart card. In banking applications another MOSFET may be used to power a card ejection mechanism.

H8/3048 and first-generation H8S products have the following limitations:

1) The only available speed of the SIM is the default value of clock/372 and
2) There is no support for the so called protocol „T=1"

Latest H8S products add 3 new speeds (clock/32, 64 and 256) and support for „T=1". These are the H8S series H8S/222x, H8S/223x, H8S/231x, H8S/232x, H8S/263x and all future H8S products.

Figure 20



Analogue to **Digital Converter** (ADC)

In many microcontroller based systems, some way of measuring analogue electrical values is necessary. With this in mind, all members of the H8S and H8/300H families are equipped with a 10-bit A/D converter, in most cases with an 8 (up to 16) channel analog multiplexer to allow numerous signals to be processed easily. The converter works using a successive approximation algorithm and conversions take 138 states (or 8. 6µs if ø - 16MHz, respectively 6. 7µs at 20MHz in case of H8S). A sample and hold circuit is used to ensure that once a conversion begins, a change of the input value will not be reflected in a different conversion result. A conversion can be initiated by software or by means of an external trigger input, and in some devices by the timer unit. At the end of the conversion an interrupt may be requested.

As well as being able to perform single conversion (single mode, where only one channel is converted), the A/D converter can also be used to scan up to four channels (scan mode). To support this mode of operation, four A/D result registers (ADDRA to D) are provided. Once the scan mode is selected, each channel specified is converted sequentially with the conversion value being stored in the appropriate result register. This mode of operation allows the user software to sample the current analogue value of an input by simply reading the appropriate data register.

High speed ADC on H8S/2655

On H8S/2655 Hitachi has implemented a new high speed ADC, capable of sustaining a conversion rate of 1 million samples per second. This is achieved by using two sample and hold (S&H) circuits which are used interleaved, i. e. while S&H A is sampling, S&H B is being converted.

But not only is this new ADC faster , but it has also new features to make it more flexible.
These new features include:

- 8 A/D data registers to store the results of each channel individually
- Enhanced conversion modes, created by combining 'select' (one channel) or 'group' (more than one) with 'single' (one shot conversion) or 'scan' (continuous conversion).
    - Select single mode: one shot conversion of one channel
    - Select scan mode: continuous conversion of one channel
    - Group single mode: one shot conversion of a number of channels
    - Group scan mode: continuous conversion of a number of channels
- Buffer operation allows to store results in FIFO-fashion in the ADDR registers. Double or quadruple buffering can be selected.
- Simultaneous sampling operation allows the two S&H to sample simultaneously. An important feature in some applications, e. g. where at least 2 out of the 3 phases of a 3-phase mains have to be observed.
- Conversion can be triggered by software, an external pin or the on-chip timers

Digital to Analogue Converter (DAC)

The H8/304x derivatives within H8/300H and most H8S derivatives feature a two channel, 8-bit resolution Digital-to-Analog-Converter (DAC). The conversion time is 10µs with a 20pF load and the output voltage range is 0V to Vref. The outputs can be maintained during software standby.

Both channels can be enabled or disabled independently. Once a channel is enabled, the corresponding pin becomes an analog output pin and the data in the D/A data register (DADR) is output at the pin after the D/A conversion time has elapsed. The pin remains in that state until DADR is written to again or until the D/A channel or the complete DAC is disabled.

The voltage at the D/A output pin can be calculated as $\frac{\text{DADR contents}}{256} \times \text{Vref.}$

Controller Area **Network** CAN

The HCAN module (Hitachi CAN)* complies to version 2.0B (Full CAN) as defined by Bosch. Additionally, an independent institute has tested the HCAN module for compliance with the standard. CAN (Controller Area Network) has become a widespread standard in the European automotive industry, because it provides very reliable, high-speed, low-latency serial communication for harsh and electromagnetically polluted environments. Therefore CAN has begun to penetrate also industrial applications, where these features are important.

CAN is a non-return to zero (NRZ), bit stuffing protocol for message-orientated serial communication via two wires, at speeds of up to 1Mbit/s. Each message contains up to 8 Byte of user data. Using these short messages is important in harsh environments, where disruption or noise could destroy a message, as the likelihood of such a case increases in proportion to the length of the message. Also, short messages keep latency low. Depending on the actual baudrate chosen, the length of the network can vary between approximately 40m and 1000m (also depending on the transceivers chosen).

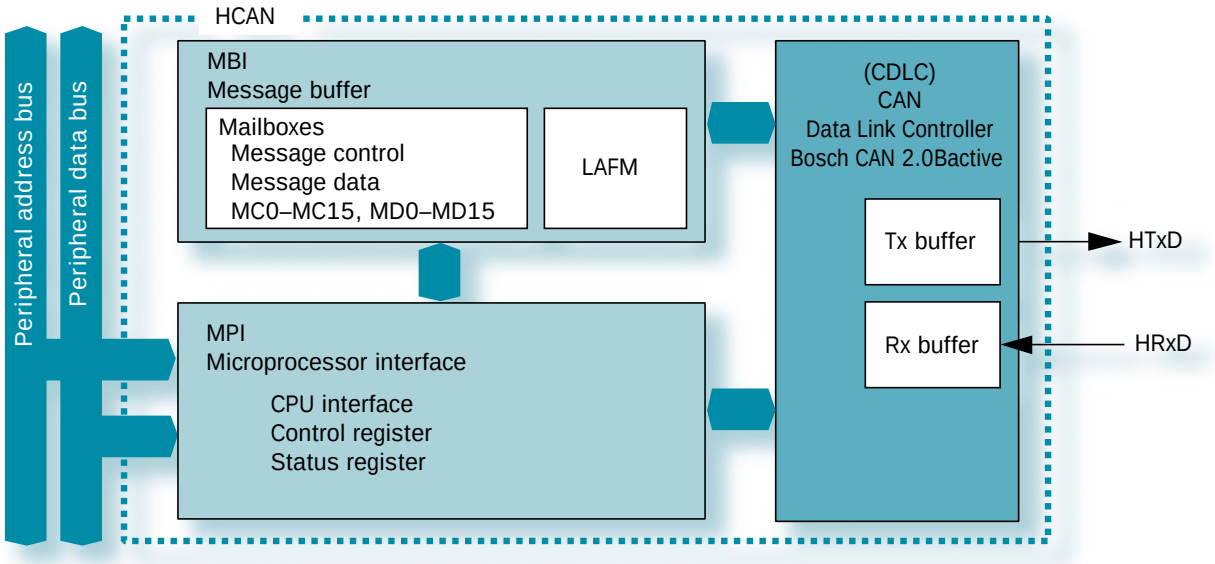
CAN allows broadcasting or multicasting, i.e. sending messages to all or some nodes at a time, hence allows synchronisation of the activities of several nodes.

A key feature of CAN is the prioritisation of messages that allows important messages to gain access to the physical bus with very short latency. CAN also allow arbitration of multiple messages that are trying to occupy the bus simultaneously. The arbitration mechanism will inherently grant access to the bus for the highest priority message.

Hitachi's HCAN module implements the CAN standard by adding sophisticated features, which allows usage in even the most demanding automotive applications like engine management. It features:

- 15 programmable receive/transmit buffers
- 1 receive-only buffer with local acceptance filtering (LAFM)
- internal priority sorting to avoid priority inversion
- flexible interrupt structure to keep CPU load to a minimum
- sleep-mode and auto wake-up, if CAN bus is active
- DMA support for mailbox 0 to reduce CPU overhead

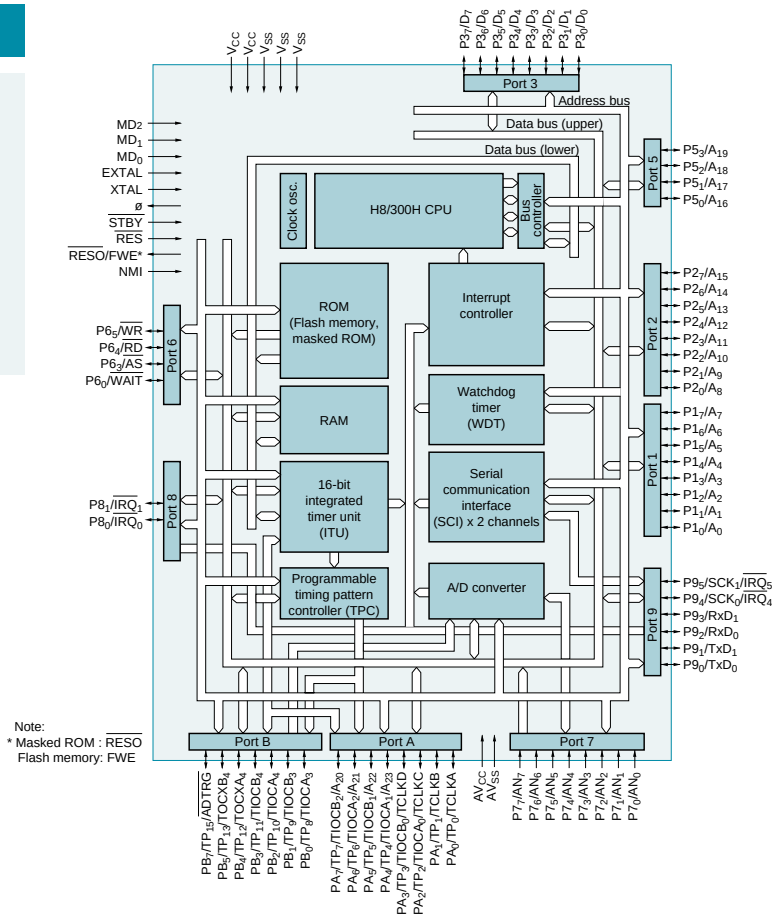
Special emphasis was put on good real time capabilities. An internal state machine sorts the messages by priority to avoid the inherent priority-inversion problem.



** For a complete Roadmap of H8 microcontrollers with HCAN please refer to page 27.*

Lowest cost H8/300H with Flash

- ROM 16k-128k, RAM 512Byte-4k, 128K Flash
- 18MHz clock yields 111ns min. instruction
- pin compatible with other H8/303x, but with 2x SCI
- popular ITU timer unit with AC motor drive modes
- Ideal for many industrial applications

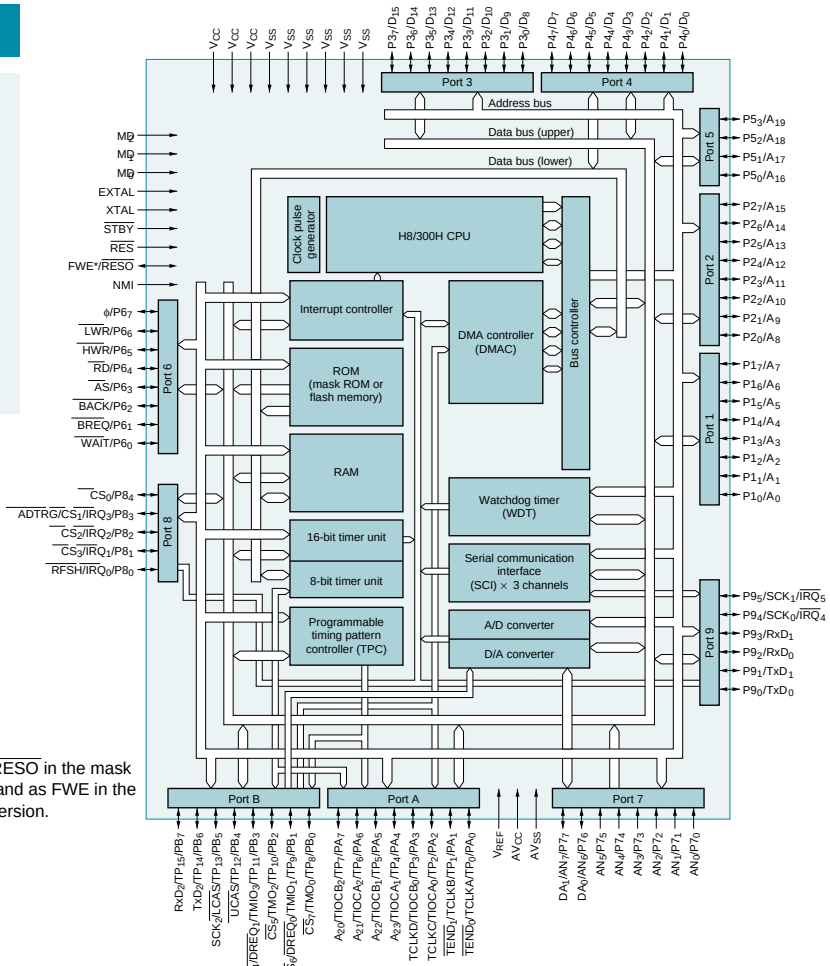


Note:
* Masked ROM : RESO
Flash memory: FWE

H 8 / 3 0 6 7

Enhanced successor of popular H8/3048

- nearly pin compatible with H8/3048
- single voltage Flash requires no Vpp
- 20MHz clock for 20% higher performance
- now 3x USART, modified timers without AC motor drive modes
- Lower cost variant H8/3062 without DMA and with 2x SCI
- please refer to application note APPS/072/1.0

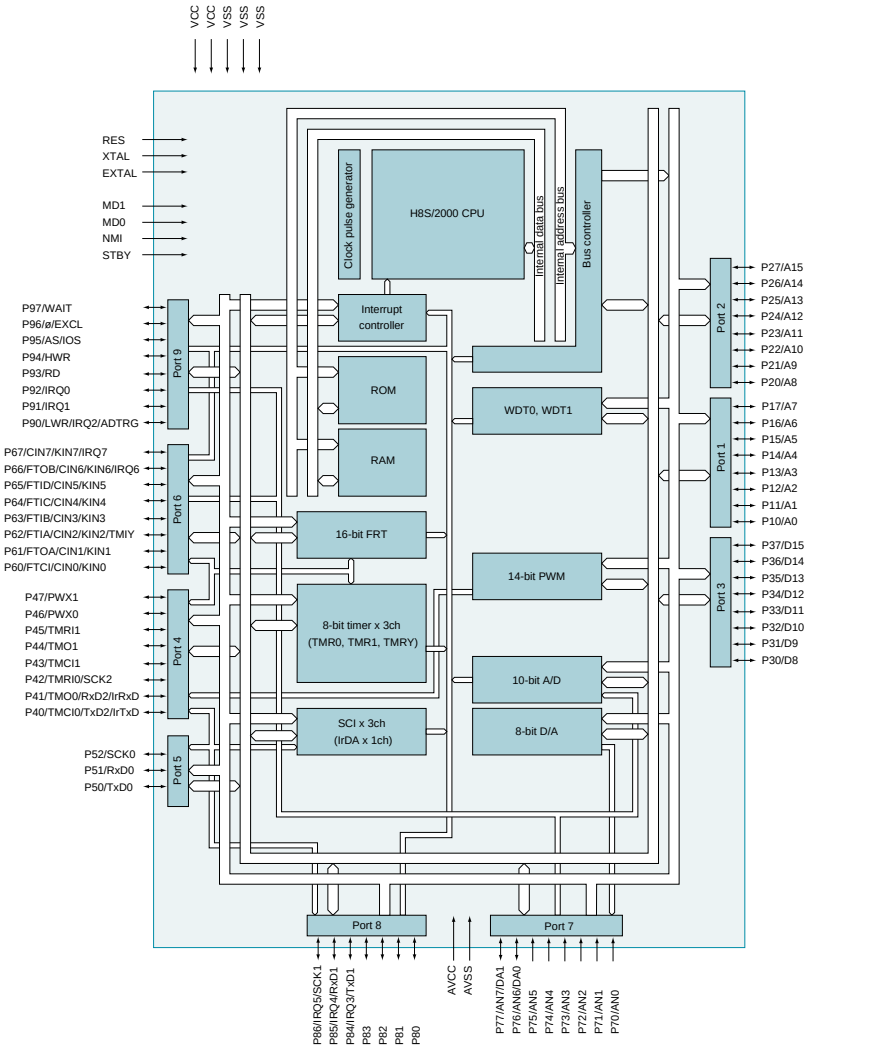


Note:
*Functions as $\overline{\text{RESO}}$ in the mask ROM versions and as FWE in the flash memory version.

H 8 S / 2 1 3 4

Very low cost H8S device in 80-pin package

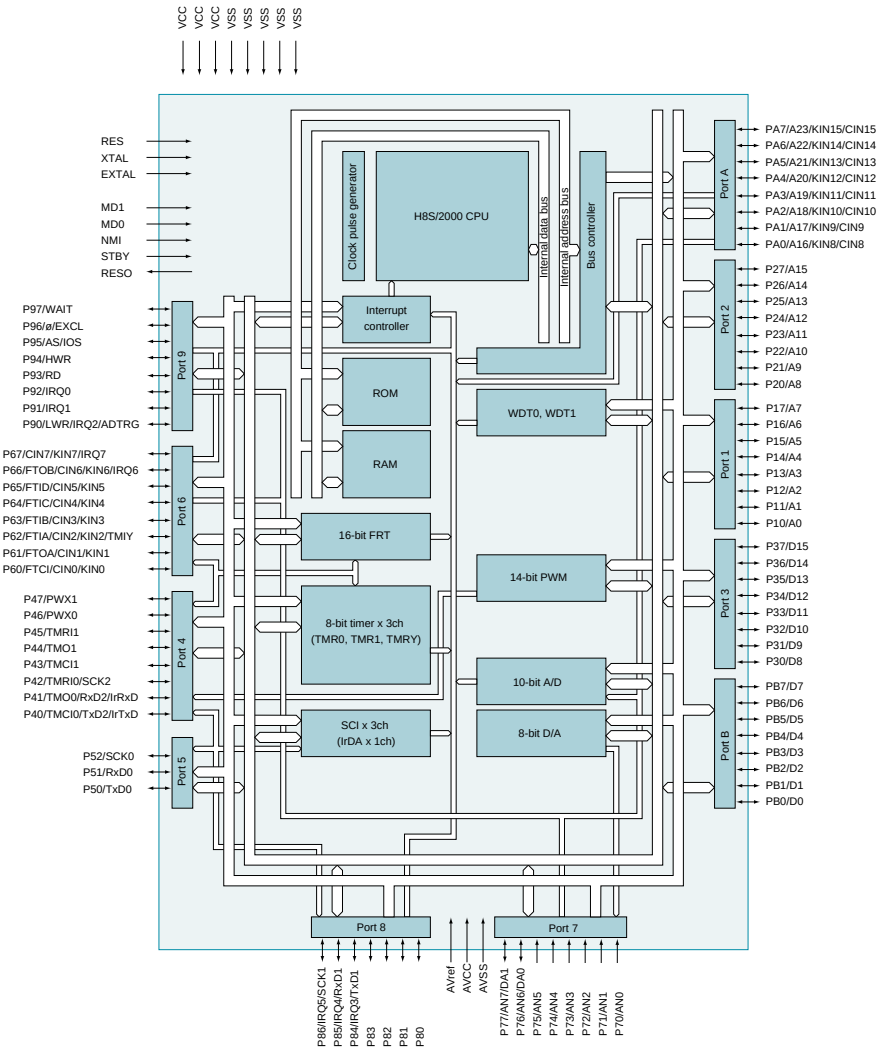
- high performance CPU delivering 6 MIPS Dhrystone
- 64k / 128K single voltage Flash, 2K / 4K RAM and several ROM sizes
- IrDA compliant infra red interface
- subclock mode
- also version with IIC, DTC and enhanced timers (H8S / 2138)
- nearly pin compatible with H8 / 3337 series



H 8 S / 2 1 4 4

Very low cost H8S device in 100-pin package

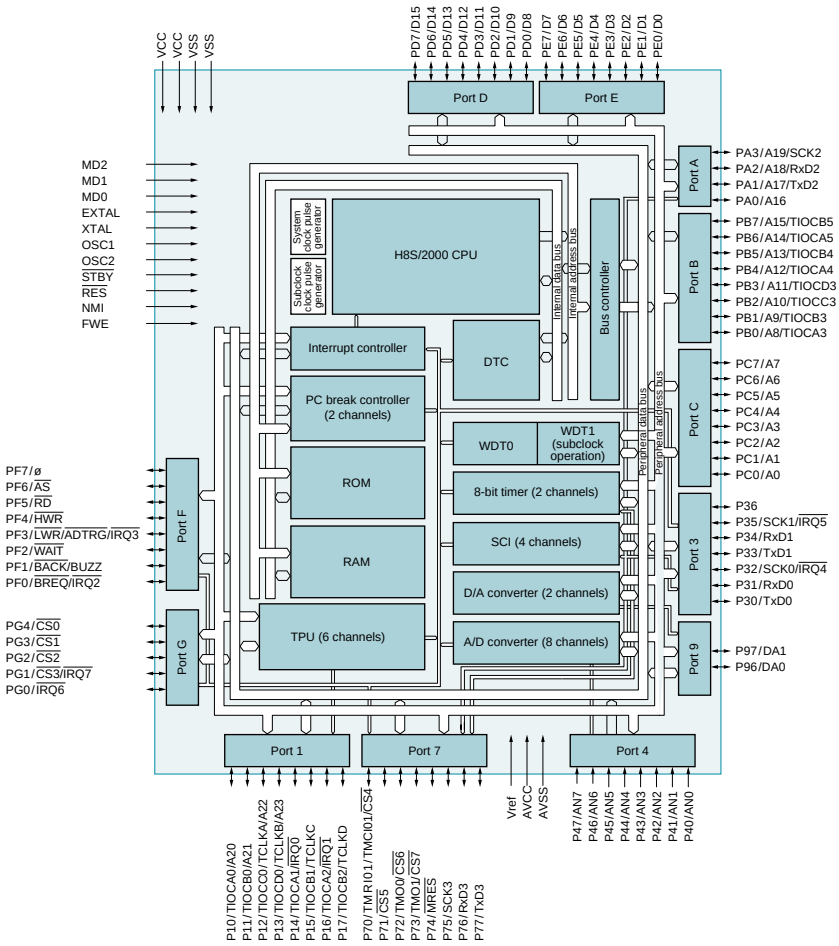
- high performance CPU delivering 6 MIPS Dhrystone
- 64k / 128K single voltage Flash, 2K / 4K RAM and several ROM sizes
- IrDA compliant infra red interface
- subclock mode
- also version with IIC, DTC and enhanced timers (H8S / 2148)
- nearly pin compatible with H8 / 3437 series



H8S/2237

Super low power, low voltage H8S with large RAM

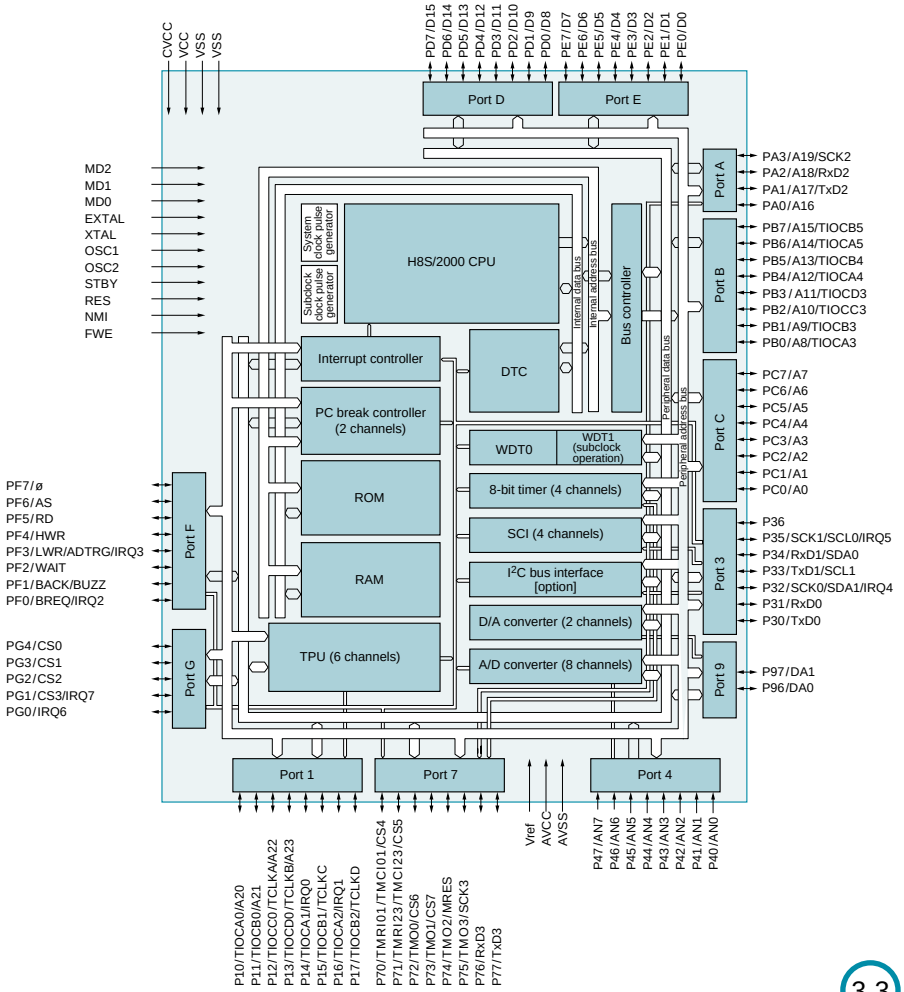
- power consumption as low as 14mA (typ.) at 3V/10MHz
- excellent power management, incl. 32KHz subclock
- large RAM to avoid using external busses
- 4 USART (SCI), supporting a subset of ISO7816-3
- pin compatible low cost variant H8S/222x
- mask derivatives available down to 2.2V operation



H8S/2238

3rd Generation 256K Flash, 16K RAM, low power H8S

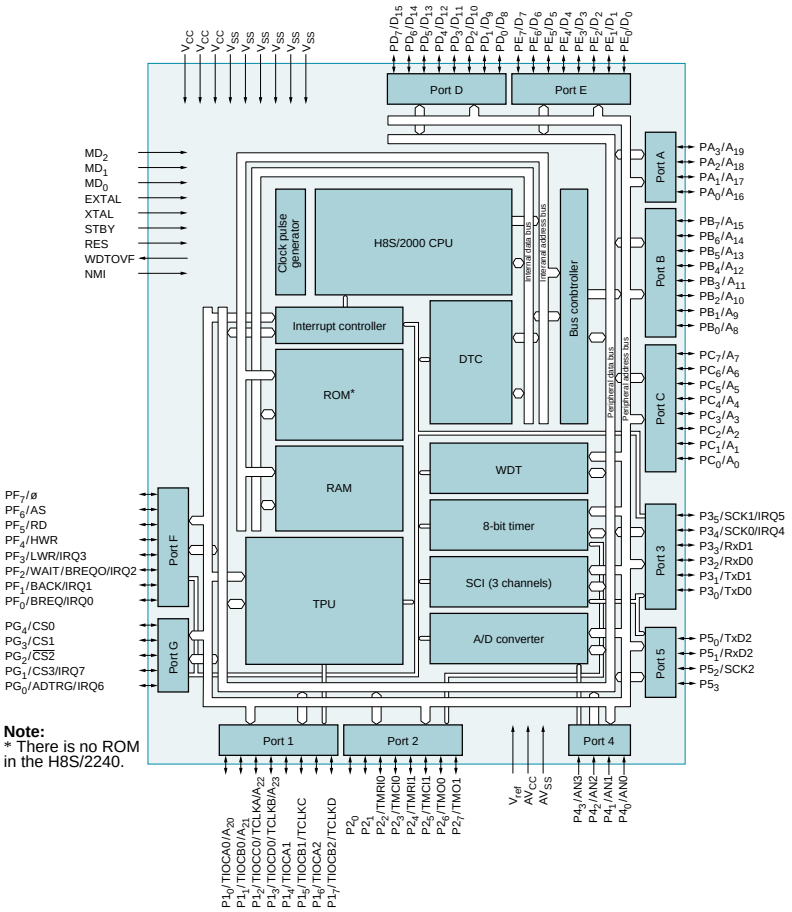
- nearly pin compatible with H8S/2237 series
- advanced on-chip power supply for 3 to 5V operation
- very low power consumption and excellent power management
- large RAM to avoid using external busses
- low cost mask derivatives (H8S/222x), available in 2.2V



H 8 S / 2 2 4 5

General purpose, low power, low cost H8S

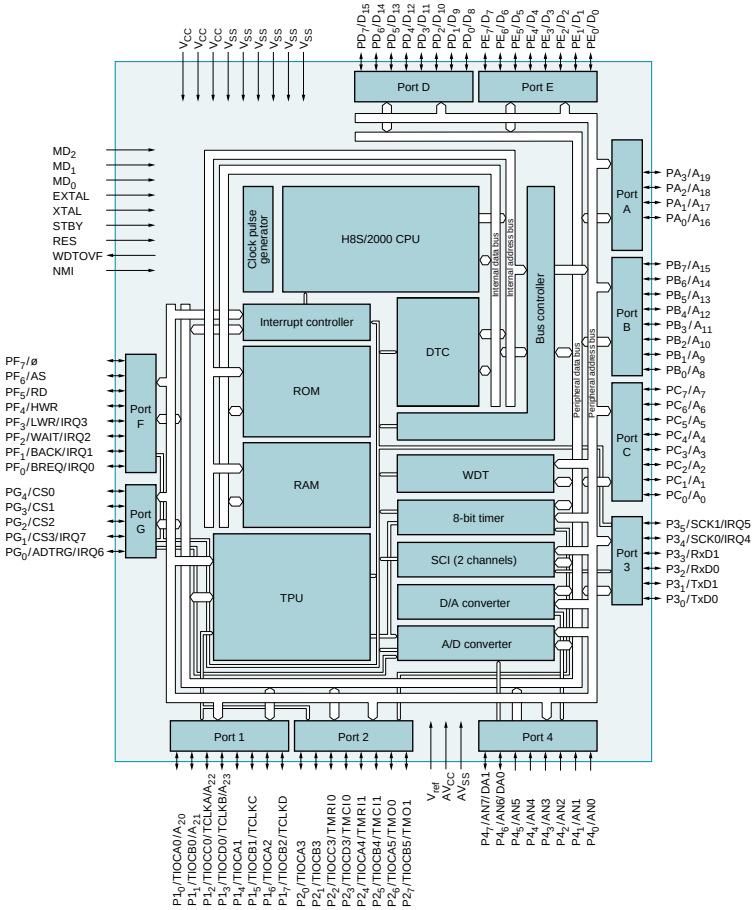
- 32k to 128K ROM, 4k or 8K RAM
- very popular, low cost H8S/2240 ROM-less device
- 3x SCI, 3x 16-bit timer with 8 IC/OC, DTC, etc.
- 3V and 5V operation
- ideal for many industrial and telecom applications



H 8 S / 2 3 4 5

General purpose H8S with 128K Flash, 4K RAM option

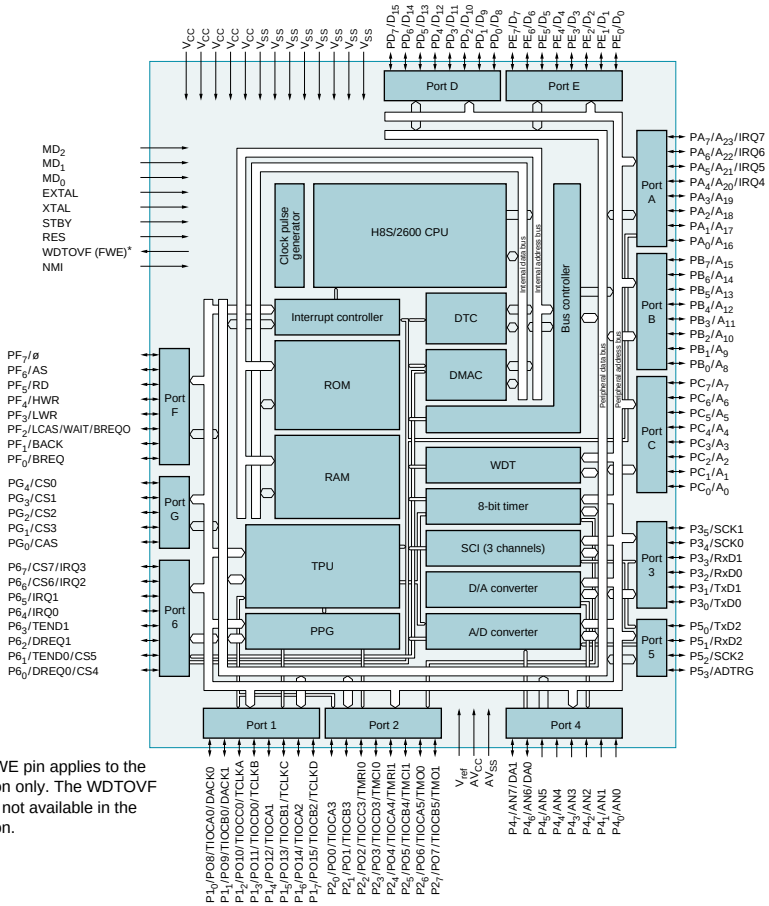
- very popular 100-pin, single volt age Flash device
- 6x 16-bit timer, 2x 8-bit timer, DTC, etc.
- ADC as well as DAC
- very small TFP-100G package (14x14mm incl. pins)



H 8 S / 2 3 5 7

General purpose H8S with 128k Flash, 8K RAM option

- high performance CPU delivering 6 MIPS Dhrystone
- very popular 120/128 pin, single voltage Flash device
- full set of peripherals, all one could ask for!
- abundant IO port resources due to high pin count
- very small TFP-120 package (16x16mm incl. pins)

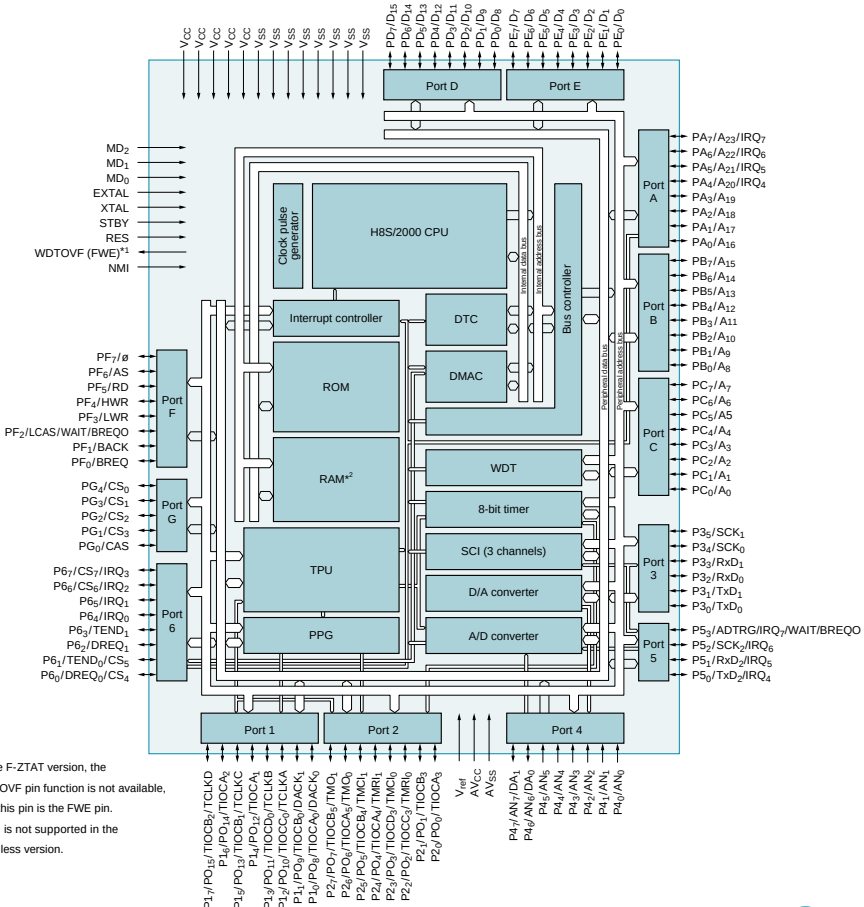


Note: *The FWE pin applies to the F-ZTAT version only. The WDTOVF pin function is not available in the F-ZTAT version.

H 8 S / 2 3 2 8

3rd Generation, 256K Flash memory H8S

- pin compatible with H8S/2357, but 3V/25MHz operation
- performance increase to 8 MIPS Dhrystone
- Full set of peripherals, all one could ask for!
- abundant IO port resources due to high pin count
- very small TFP-120 package (16x16mm incl. pins)

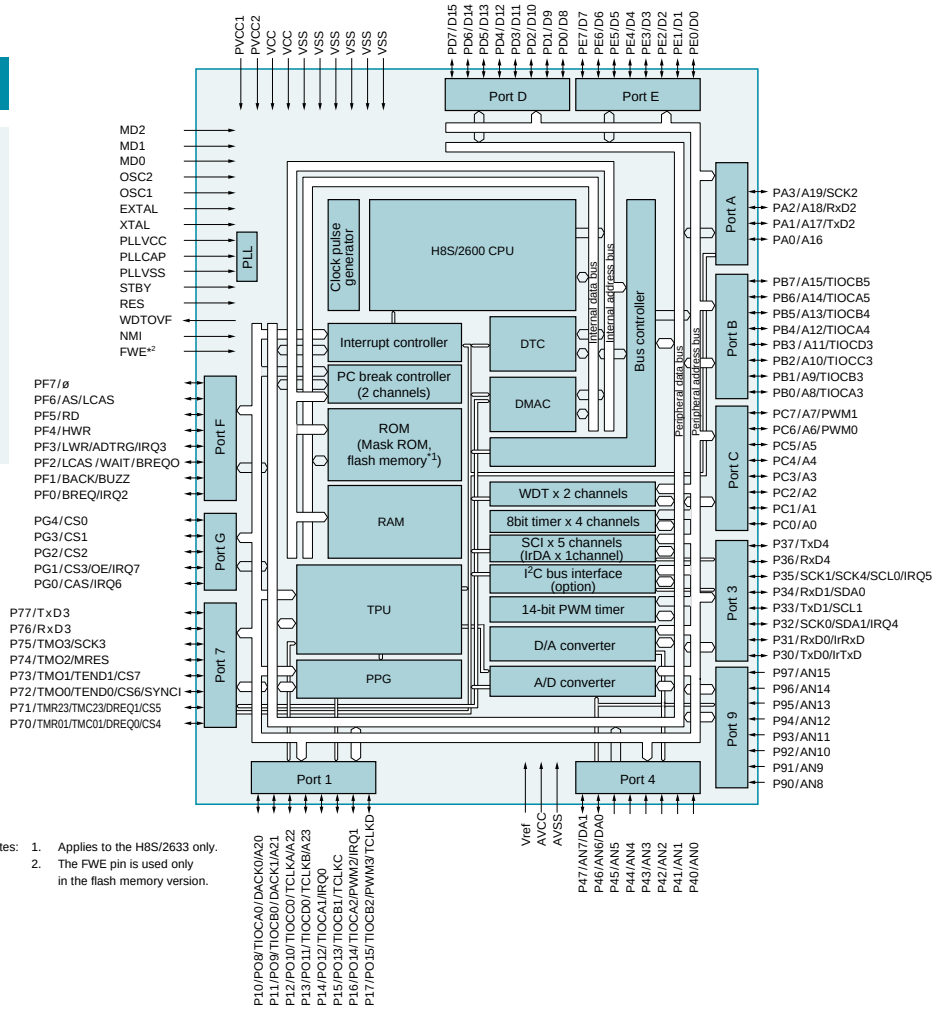


Notes: 1. In the F-ZTAT version, the WDTOVF pin function is not available, and this pin is the FWE pin.
2. ROM is not supported in the ROMless version.

H8S/2633

Super high integration H8S

- 25MHz with Multiply-Accumulate hardware (MAC)
- Delivers almost 10 MIPS Dhrystone
- 3rd generation 256K Flash and 16K RAM
- Very large set of peripherals, incl. 5x SCI, IIC, IrDA, etc.
- Separate power supply for IO ports, for 5V tolerance

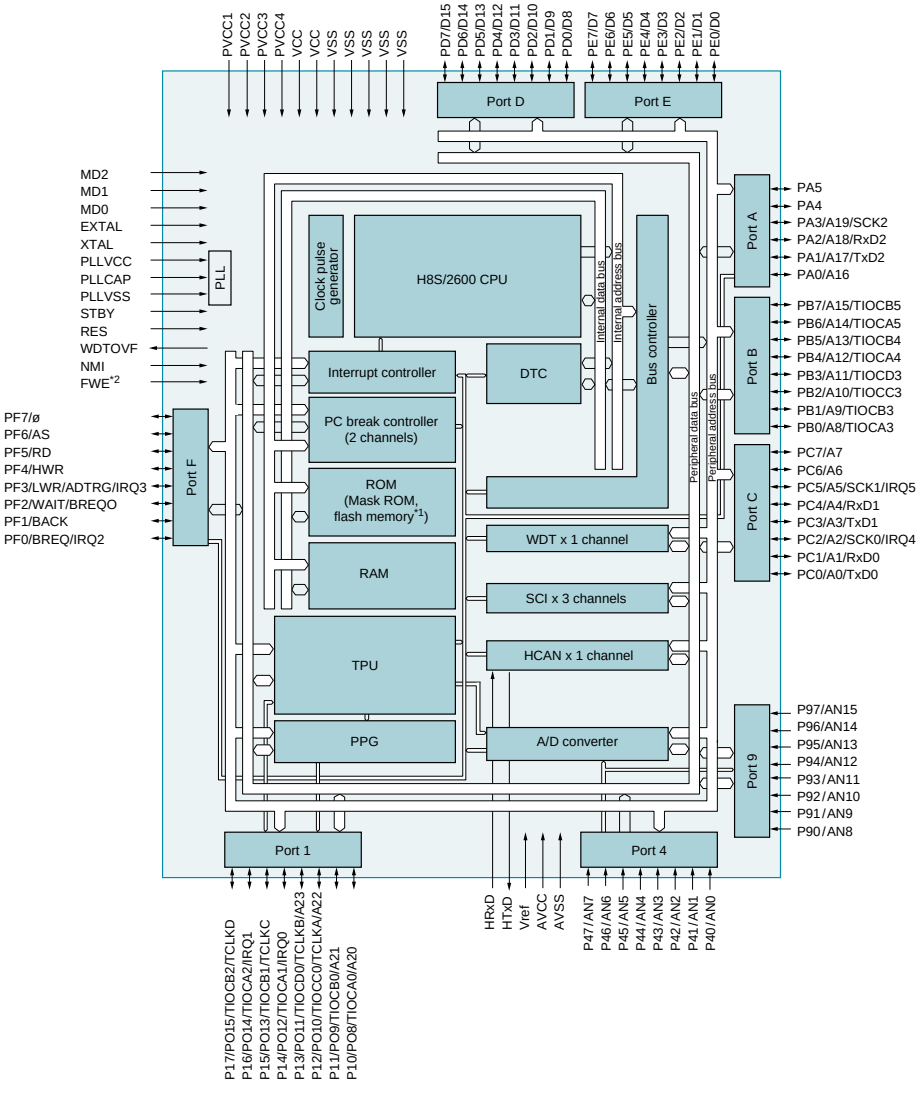


Notes: 1. Applies to the H8S/2633 only.
2. The FWE pin is used only in the flash memory version.

H8S/2623

H8S with integrated CAN V2.0B

- 20MHz with Multiply-Accumulate harware (MAC)
- 3rd generation 256K Flash and 12K RAM
- sophisticated CAN V2.0B module
- Excellent peripherals mix incl. 16ch ADC, 3x SCI, DTC, etc.
- Separate power supply for IO ports, for 5V tolerance



Ordering **Information**

The following tables show the available derivatives for each series within the H8/300H and H8S families. To build the actual part name append the desired clock rate to the part name's body.

Example: HD6413001F16 = H8/3001 in FP-80A package, 5V (±10%), 16MHz.

For details (tolerance) of the operating voltage range, please refer to the selector guide in the middle of this brochure.

H8/3001 (ROM-less)

Body	Package suffix	Package/Voltage/Temp.	available clock
HD6413001	F	FP-80A/5V	16
	TF	TFP-80C/5V	16
	VF	FP-80A/low	8,13
	VTF	TFP-80C/low	8,13
	FI	FP-80A/5V/-40°C..85°C	16
	TFI	TFP-80C/5V/-40°C..85°C	16
	VFI	FP-80A/low/-40°C..85°C	8,13
	VTFI	TFP-80C/low/-40°C..85°C	8,13
	FJ	FP-80A/5V/-40°C..85°C	16

H8/3002 (ROM-less)

Body	Package suffix	Package/Voltage/Temp.	available clock
HD6413002	F	FP-100B/5V	16
	TF	TFP-100B/5V	16
	VF	FP-100B/low	8,10
	VTF	TFP-100B/low	8,10
	FI	FP-100B/5V/-40°C..85°C	16
	TFI	TFP-100B/5V/-40°C..85°C	16
	VFI	FP-100B/low/-40°C..85°C	8,10
	VTFI	TFP-100B/low/-40°C..85°C	8,10
	FJ	FP-100B/5V/-40°C..85°C	16

H8/3003 (ROM-less)

Body	Package suffix	Package/Voltage/Temp.	available clock
HD6413003	RF	FP-112/5V	16
	RTE	TFP-120/5V	16
	TF	FP-112/5V	16
	TTE	TFP-120/5V	16
	RVF	FP-112/low	8,10
	RVTE	TFP-120/low	8,10
	TVF	FP-112/low	8,10
	TVTE	TFP-120/low	8,10
	RFI	FP-112/5V/-40°C..85°C	16
	RTEI	TFP-120/5V/-40°C..85°C	16
	TFI	FP-112/5V/-40°C..85°C	16
	TTEI	TFP-120/5V/-40°C..85°C	16
	RVFI	FP-112/low/-40°C..85°C	8,10
	RVTEI	TFP-120/low/-40°C..85°C	8,10
	TVFI	FP-112/low/-40°C..85°C	8,10
	TVTEI	TFP-120/low/-40°C..85°C	8,10
	RFJ	FP-112/5V/-40°C..85°C	16
	TFJ	FP-112/5V/-40°C..85°C	16

Note: For H8/3003 derivatives with a package suffix starting 'R', a crystal with double frequency is required, because of an internal divider by 2.

H8/3004 and H8/3005 (ROM-less)

Body	Package suffix	Package/Voltage/Temp.	available clock
HD6413004	F	FP-80A/5V	16,18
HD6413005	TE	TFP-80C/5V	16,18
	VF	FP-80A/low	8,10
	VTE	TFP-80C/low	8,10
	FI	FP-80A/5V/-40°C..85°C	16,18
	TEI	TFP-80C/5V/-40°C..85°C	16,18
	VFI	FP-80A/low/-40°C..85°C	8,10
	VTEI	TFP-80C/low/-40°C..85°C	8,10
	FJ	FP-80A/5V/-40°C..85°C	16,18

H8/3006 and H8/3007 (ROM-less)

Body	Package suffix	Package/Voltage/Temp.	available clock
HD6413006	F	FP-100B/5V	20
HD6413007	TE	TFP-100B/5V	20
	VF	FP-100B/low	13
	VTE	TFP-100B/low	13
	VF	FP-100B/low	10
	VTE	TFP-100B/low	10
	FI	FP-100B/5V/-40°C..85°C	20
	TEI	TFP-100B/5V/-40°C..85°C	20
	VFI	FP-100B/low/-40°C..85°C	13
	VTEI	TFP-100B/low/-40°C..85°C	13
	VFI	FP-100B/low/-40°C..85°C	10
	VTEI	TFP-100B/low/-40°C..85°C	10
	FJ	FP-100B/5V/-40°C..85°C	20

H8/3032 (OTP)

Body	Package suffix	Package/Voltage/Temp.	available clock
HD6473032	F	FP-80A/5V	16
	TF	TFP-80C/5V	16
	VF	FP-80A/low	8,10
	VTF	TFP-80C/low	8,10
	FI	FP-80A/5V/-40°C..85°C	16
	TFI	TFP-80C/5V/-40°C..85°C	16
	VFI	FP-80A/low/-40°C..85°C	8,10
	VTFI	TFP-80C/low/-40°C..85°C	8,10
	FJ	FP-80A/5V/-40°C..85°C	16

H8/3035 (OTP)

Body	Package suffix	Package/Voltage/Temp.	available clock
HD6473035	F	FP-80A/5V	18
	TE	TFP-80C/5V	18
	VF	FP-80A/low	8,10
	VTE	TFP-80C/low	8,10
	FI	FP-80A/5V/-40°C..85°C	18
	TEI	TFP-80C/5V/-40°C..85°C	18
	VFI	FP-80A/low/-40°C..85°C	8,10
	VTEI	TFP-80C/low/-40°C..85°C	8,10
	FJ	FP-80A/5V/-40°C..85°C	18

H8/3039 (Flash)

Body	Package suffix	Package/Voltage/Temp.	available clock
HD64F3039	F	FP-80A/5V	18
	TE	TFP-80C/5V	18
	VF	FP-80A/low	10
	VTE	TFP-80C/low	10
	FI	FP-80A/5V/-40°C..85°C	18
	TEI	TFP-80C/5V/-40°C..85°C	18
	VFI	FP-80A/low/-40°C..85°C	10
	VTEI	TFP-80C/low/-40°C..85°C	10
	FJ	FP-80A/5V/-40°C..85°C	18

H8/3042 (OTP)

Body	Package suffix	Package/Voltage/Temp.	available clock
HD6473042S	F	FP-100B/5V	16
	TF	TFP-100B/5V	16
	VF	FP-100B/low	8,10
	VTF	TFP-100B/low	8,10
	FI	FP-100B/5V/-40°C..85°C	16
	TFI	TFP-100B/5V/-40°C..85°C	16
	VFI	FP-100B/low/-40°C..85°C	8,10
	VTFI	TFP-100B/low/-40°C..85°C	8,10
	FJ	FP-100B/5V/-40°C..85°C	16

H8S Ordering Information

H8/3048 (OTP)

Body	Package suffix	Package/Voltage/Temp.	available clock
HD6473048S	F	FP-100B/5V	16
	TF	TFP-100B/5V	16
	VF	FP-100B/low	8,13
	VTF	TFP-100B/low	8,13
	FI	FP-100B/5V/-40°C..85°C	16
	TFI	TFP-100B/5V/-40°C..85°C	16
	VFI	FP-100B/low/-40°C..85°C	8,13
	VTFI	TFP-100B/low/-40°C..85°C	8,13
	FJ	FP-100B/5V/-40°C..85°C	16

H8/3048 (Flash)

Body	Package suffix	Package/Voltage/Temp.	available clock
HD64F3048	F	FP-100B/5V	16
	TF	TFP-100B/5V	16
	VF	FP-100B/low	8
	VTF	TFP-100B/low	8
	FI	FP-100B/5V/-40°C..85°C	16
	TFI	TFP-100B/5V/-40°C..85°C	16
	VFI	FP-100B/low/-40°C..85°C	8
	VTFI	TFP-100B/low/-40°C..85°C	8
	FJ	FP-100B/5V/-40°C..85°C	16

H8/3062 and H8/3067 (Flash)

Body	Package suffix	Package/Voltage/Temp.	available clock
HD64F3062R	F	FP-100B/5V	20
HD64F3067R	TE	TFP-100B/5V	20
	VF	FP-100B/low	13
	VTE	TFP-100B/low	13
	FI	FP-100B/5V/-40°C..85°C	20
	TEI	TFP-100B/5V/-40°C..85°C	20
	VFI	FP-100B/low/-40°C..85°C	13
	VTEI	TFP-100B/low/-40°C..85°C	13
	FJ	FP-100B/5V/-40°C..85°C	20

H8/3040 (pseudo ROM-less version)

Body	Vcc/clock suffix	Package suffix	Package/Temp.
HD6433040S	A, P, T, V	00F	FP-100B
	A, P, T, V	00TF	TFP-100B
	A, P, T, V	00FI	FP-100B/-40°C..85°C
	A, P, T, V	00TFI	TFP-100B/-40°C..85°C
	A, P	00FJ	FP-100B/-40°C..85°C

Vcc/clock suffix:

A	16MHz/5V
P	17MHz/5V
T	10MHz/3.0..5.5V
V	8MHz/2.7..5.5V

H8/3044 (pseudo ROM-less version)

Body	Vcc/clock suffix	Package suffix	Package/Temp.
HD6433044S	A, M, S, V	00F	FP-100B
	A, M, S, V	00TF	TFP-100B
	A, M, S, V	00FI	FP-100B/-40°C..85°C
	A, M, S, V	00TFI	TFP-100B/-40°C..85°C
	A, M	00FJ	FP-100B/-40°C..85°C

Vcc/clock suffix:

A	16MHz/5V
M	18MHz/5V
S	13MHz/3.15..5.5V
V	8MHz/2.7..5.5V

H8S/2128 (Flash)

Body	Package suffix	Package/Voltage
HD64F2128	FA20	FP-64A/5V
	PS20	DP-64S/5V
	TF20	TFP-80C/5V
	VFA10	FP-64A/low
	VPS10	DP-64S/low
	VTF10	TFP-80C/low

H8S/2132 and H8S/2134 (Flash)

Body	Package suffix	Package/Voltage/Temp.
HD64F2132	FA20	FP-80A/5V
HD64F2134	TF20	TFP-80C/5V
	VFA10	FP-80A/low
	VTF10	TFP-80C/low
	FA20J	FP-80A/5V/-40°C..85°C
	TF20I	TFP-80C/5V/-40°C..85°C

H8S/2138 (Flash)

Body	Package suffix	Package/Voltage
HD64F2138	FA20	FP-80A/5V
	TF20	TFP-80C/5V
	VFA10	FP-80A/low
	VTF10	TFP-80C/low

H8S/2142 and H8S/2144 (Flash)

Body	Package suffix	Package/Voltage/Temp.
HD64F2142	FA20	FP-100B/5V
HD64F2144	TE20	TFP-100B/5V
	VFA10	FP-100B/low
	VTE10	TFP-100B/low
	FA20J	FP-100B/5V/-40°C..85°C
	TE20I	TFP-100B/5V/-40°C..85°C

H8S/2148 (Flash)

Body	Package suffix	Package/Voltage
HD64F2148	FA20	FP-100B/5V
	TE20	TFP-100B/5V
	VFA10	FP-100B/low
	VTE10	TFP-100B/low

H8S/2237 (OTP)

Body	Package suffix	Package/Voltage/Temp.
HD6472237	F10	FP-100A/low
	FA10	FP-100B/low
	TE10	TFP-100B/low
	TF10	TFP-100G/low
	F10I	FP-100A/low/-40°C..85°C
	FA10I	FP-100B/low/-40°C..85°C
	TE10I	TFP-100B/low/-40°C..85°C
	TF10I	TFP-100G/low/-40°C..85°C

H8S/2238 (Flash)

Body	Package suffix	Package/Voltage/Temp.
HD64F2238	F13	FP-100A/low
	FA13	FP-100B/low
	TE13	TFP-100B/low
	TF13	TFP-100G/low
	F13I	FP-100A/low/-40°C..85°C
	FA13I	FP-100B/low/-40°C..85°C
	TE13I	TFP-100B/low/-40°C..85°C
	TF13I	TFP-100G/low/-40°C..85°C

H8S/2240 (ROM-less)

Body	Package suffix	Package/Voltage/Temp.
HD6412240	FA20	FP-100B/5V
	TE20	TFP-100B/5V
	FA13	FP-100B/low
	TE13	TFP-100B/low
	FA10	FP-100B/low
	TE10	TFP-100B/low
	FA20I	FP-100B/5V/-40°C..85°C
	TE20I	TFP-100B/5V/-40°C..85°C
	FA13I	FP-100B/low/-40°C..85°C
	TE13I	TFP-100B/low/-40°C..85°C
	FA10I	FP-100B/low/-40°C..85°C
	TE10I	TFP-100B/low/-40°C..85°C

H8S/2242 (pseudo ROM-less version)

Body	Vcc/clock suffix	Package suffix	Package/Temp.
HD6432242	A,M,K	00FA	FP-100B
		00TE	TFP-100B
		00FAI	FP-100B/-40°C..85°C
		00TEI	TFP-100B/-40°C..85°C

Vcc/clock suffix: A=5V/20MHz, M=low/13MHz, K=low/10MHz

H8S/2246 (OTP)

Body	Package/clock suffix	Package/Voltage/Temp.
HD6472246	FA20	FP-100B/5V
	TE20	TFP-100B/5V
	FA10	FP-100B/low
	TE10	TFP-100B/low
	FA20I	FP-100B/5V/-40°C..85°C
	TE20I	TFP-100B/5V/-40°C..85°C
	FA10I	FP-100B/low/-40°C..85°C
	TE10I	TFP-100B/low/-40°C..85°C

H8S/2322 (ROM-less) and H8S/2328 (Flash)

Body	Package/clock suffix	Package/Voltage/Temp.
HD6412322	VF20	FP-128/low
HD64F2328	VTE20	TFP-120/low
	VF25	FP-128/low
	VTE25	TFP-120/low
	VF20I	FP-128/low/-40°C..85°C
	VTE20I	TFP-120/low/-40°C..85°C
	VF25I	FP-128/low/-40°C..85°C
	VTE25I	TFP-120/low/-40°C..85°C

H8S/2340 (ROM-less)

Body	Package/clock suffix	Package/Voltage/Temp.
HD6412340	F20	FP-100A/5V
	FA20	FP-100B/5V
	TE20	TFP-100B/5V
	TF20	TFP-100G/5V
	F10	FP-100A/low
	FA10	FP-100B/low
	TE10	TFP-100B/low
	TF10	TFP-100G/low
	F20I	FP-100A/5V/-40°C..85°C
	FA20I	FP-100B/5V/-40°C..85°C
	TE20I	TFP-100B/5V/-40°C..85°C
	TF20I	TFP-100G/5V/-40°C..85°C
	F10I	FP-100A/low/-40°C..85°C
	FA10I	FP-100B/low/-40°C..85°C
	TE10I	TFP-100B/low/-40°C..85°C
	TF10I	TFP-100G/low/-40°C..85°C

H8S/2345 (Flash)

Body	Package/clock suffix	Package/Voltage
HD64F2345	F20	FP-100A/5V
	FA20	FP-100B/5V
	TE20	TFP-100B/5V
	TF20	TFP-100G/5V

H8S/2350 (ROM-less)

Body	Package/clock suffix	Package/Voltage/Temp.
HD6412350	F20	FP-128/5V
	TE20	TFP-120/5V
	F10	FP-128/low
	TE10	TFP-120/low
	F20I	FP-128/5V/-40°C..85°C
	TE20I	TFP-120/5V/-40°C..85°C
	F10I	FP-128/low/-40°C..85°C
	TE10I	TFP-120/low/-40°C..85°C

H8S/2352 (ROM-less)

Body	Package/clock suffix	Package/Voltage/Temp.
HD6412352	F20	FP-128/5V
	TE20	TFP-120/5V
	F13	FP-128/low
	TE13	TFP-120/low
	F10	FP-128/low
	TE10	TFP-120/low
	F20I	FP-128/5V/-40°C..85°C
	TE20I	TFP-120/5V/-40°C..85°C
	F13I	FP-128/low/-40°C..85°C
	TE13I	TFP-120/low/-40°C..85°C
	F10I	FP-128/low/-40°C..85°C
	TE10I	TFP-120/low/-40°C..85°C

H8S/2355 (OTP)

Body	Package/clock suffix	Package/Voltage/Temp.
HD6472355	F20	FP-128/5V
	TE20	TFP-120/5V
	F10	FP-128/low
	TE10	TFP-120/low
	F20I	FP-128/5V/-40°C..85°C
	TE20I	TFP-120/5V/-40°C..85°C
	F10I	FP-128/low/-40°C..85°C
	TE10I	TFP-120/low/-40°C..85°C

H8S/2357 (OTP)

Body	Package/clock suffix	Package/Voltage/Temp.
HD6472357	F20	FP-128/5V
	TE20	TFP-120/5V
	F13	FP-128/low
	TE13	TFP-120/low
	F10	FP-128/low
	TE10	TFP-120/low
	F20I	FP-128/5V/-40°C..85°C
	TE20I	TFP-120/5V/-40°C..85°C
	F13I	FP-128/low/-40°C..85°C
	TE13I	TFP-120/low/-40°C..85°C
	F10I	FP-128/low/-40°C..85°C
	TE10I	TFP-120/low/-40°C..85°C

H8S/2357 (Flash)

Body	Package/clock suffix	Package/Voltage/Temp.
HD64F2357	F20	FP-128/5V
	TE20	TFP-120/5V
	VF13	FP-128/low
	VTE13	TFP-120/low
	F20I	FP-128/5V/-40°C..85°C
	TE20I	TFP-120/5V/-40°C..85°C
	VF13I	FP-128/low/-40°C..85°C
	VTE13I	TFP-120/low/-40°C..85°C

H8S/2623 (Flash)

Body	Package/clock suffix	Package/Voltage/Temp.
HD64F2623	FA20J	FP-100B/low/-40°C..85°C

H8S/2633 (Flash)

Body	Package/clock suffix	Package/Voltage/Temp.
HD64F2633	F25	FP-128/low
	TE25	TFP-120/low
	F25I	FP-128/low/-40°C..85°C
	TE25I	TFP-120/low/-40°C..85°C

H8S/2655 (OTP)

Body	Package/clock suffix	Package/Voltage/Temp.
HD6472655R	F	FP-128/5V
	TE	TFP-120/5V
	VF	FP-128/low
	VTE	TFP-120/low
	FI	FP-128/5V/-40°C..85°C
	TEI	TFP-120/5V/-40°C..85°C
	VFI	FP-128/low/-40°C..85°C
	VTEI	TFP-120/low/-40°C..85°C

H8S/2655 (pseudo ROM-less version)

Body	Package/clock suffix	Package/Voltage/Temp.
HD6432655A00	F	FP-128/5V
	TE	TFP-120/5V
	FI	FP-128/5V/-40°C..85°C
	TEI	TFP-120/5V/-40°C..85°C

Ordering Information and **Packages**

Naming rule for H8/300H mask ROM parts

HD643 + device body+ revision + code/speed + ROM code + package + temperature

device body	4-digit code of desired H8/300H derivative, e. g. 3042 for H8/3042	
revision	S for mask revision or omitted, for new inquiries always use 'S' (where applicable)	
ROM code	2-digit number assigned to mask after customer code submission	
code/speed	A. . E	16MHz/5V
	F. . H	12MHz/5V
	K,L	10MHz/5V
	M	18MHz/5V
	P	17MHz/5V
	S	13MHz/3.15 . . . 5. 5V
	T,U	10MHz/3. 0 (or 3. 15V) . . . 5. 5V
	V,W	8MHz/2. 7 . . 5. 5V

When the "ROM code" overflows (>99) the "code/speed" digit advances, e. g. from A99 to B00.

package		
F	QFP	14mm x 14mm (except H8/3003)
FP	QFP	14mm x 20mm
TF	TQFP	14mm x 14mm
temperature		
	I, J	-40°C. . 85°C (J-spec has special reliability)
	JE	-40°C. . 105°C
	K	-40°C. . 125°C

Example: HD6433032SMxxF is a mask ROM H8/3032S (mask revision), with 18MHz/5V in FP-80A package (14mm x 14mm) in standard spec. xx will be determined after ROM code submission.

Naming rule for H8S mask ROM parts

HD643 + device body+ revision + code/speed + ROM code + package + temperature

device body	4-digit code of desired H8S derivative, e. g. 2653 for H8S/2653	
revision (2653 only)	B for mask revision	
ROM code	2-digit number assigned to mask after customer code submission	
code/speed	A	20MHz/5V
	K	10MHz/2. 7. . 5. 5V
	L	16MHz/4. 0. . 5. 5V
	M	13MHz/2. 7 (or 3. 0). . 5. 5V

When the "ROM code" overflows (>99) the "code/speed" digit advances, e. g. from A99 to B00.

package		
F	QFP	20mm x 14mm
FA	QFP	14mm x 14mm
TE	TQFP	14mm x 14mm
TF	TQFP	12mm x 12mm
temperature		
	I, J	-40°C. . 85°C (J-spec has special reliability)
	JE	-40°C. . 105°C
	K	-40°C. . 125°C

Example: HD6432357AxxFI is a mask ROM H8S/2357, with 20MHz/5V in FP-128 package (20mm x 14mm) in I-spec. xx will be determined after ROM code submission.

Pseudo ROM-less derivatives

These devices are mask ROM H8/300H or H8S with a blank ROM, for which standard ROM-less commercial criteria apply (e. g. minimum order quantity). The part names comply with the masked ROM naming rule (please see above).

Microcontrollers for wide temperature range (WTR)

All of Hitachi's microcontrollers are available in several temperature ranges. The standard temperature range is -20°C. . 75°C and is not indicated in the package suffix.

-40°C. . 85°C (I and J-spec)

Hitachi offers two specifications for -40°C. . 85°C. These are indicated in the package suffix by I and J. I-spec has a wider temperature range compared with standard spec, but has the same reliability. J-spec has improved reliability compared with standard spec. Hitachi recommends to use J-spec for critical applications, particularly in industrial and automotive applications.

-40°C. . 105°C (JE-spec)

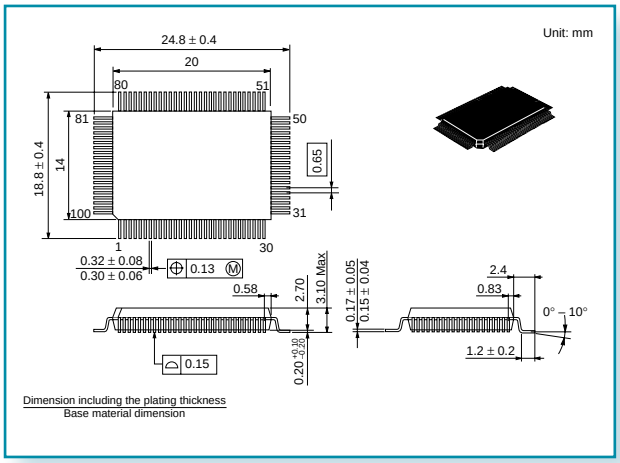
JE-spec has the same reliability as J-spec but extends the operating temperature range to 105°C. This should - for example - be used in critical applications for automotive safety.

-40°C. . 125°C (K-spec)

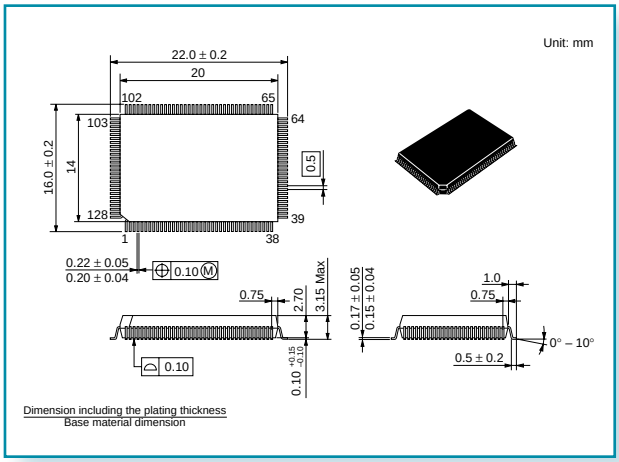
K-spec further extends the temperature range to 125°C and also improves reliability over JE-spec. We recommend this for important safety features in the automotive market, where the product is installed e. g. near the engine.

If you require JE- or K-spec, please contact your Hitachi sales office or authorized distributor.

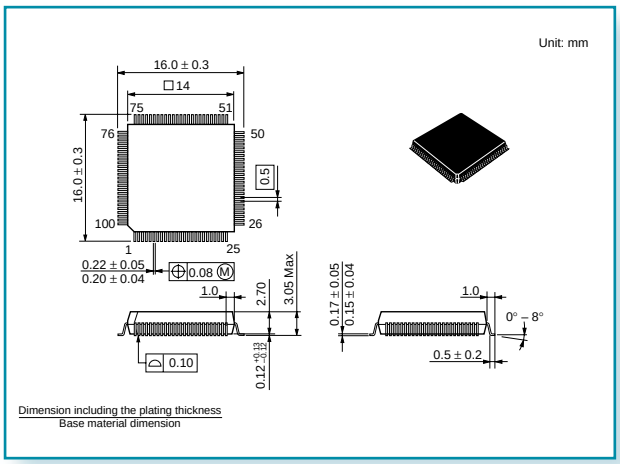
P a c k a g e s



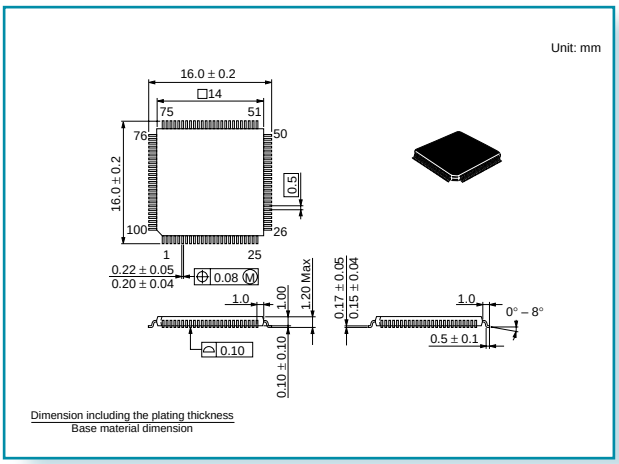
F P - 1 0 0 A



F P - 1 2 8

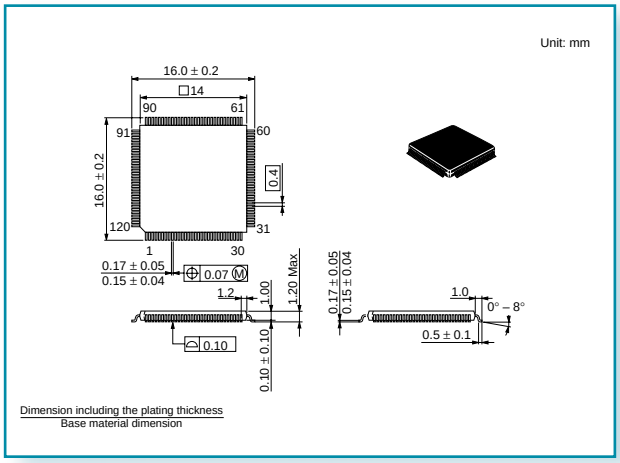


F P - 1 0 0 B

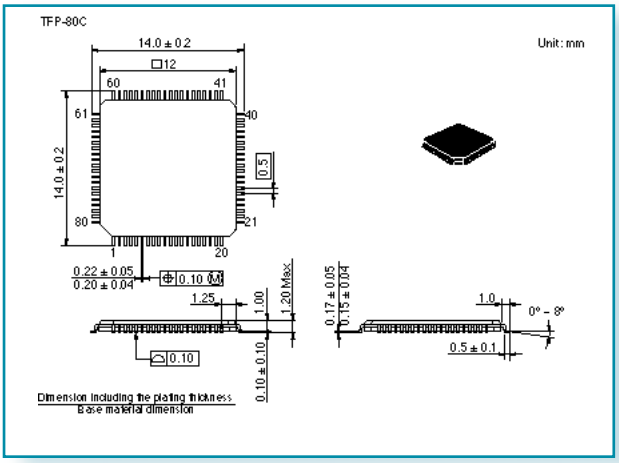


T F P - 1 0 0 B

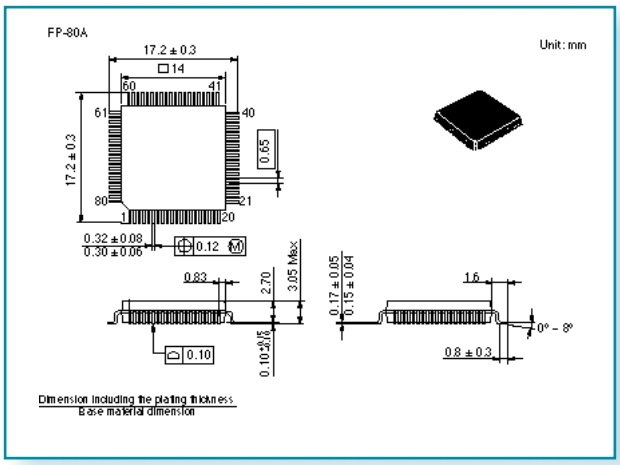
P a c k a g e s



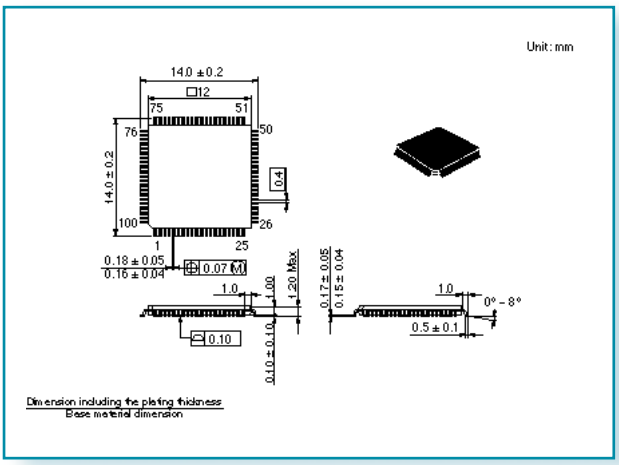
T F P - 1 2 0



T F P - 8 0 C

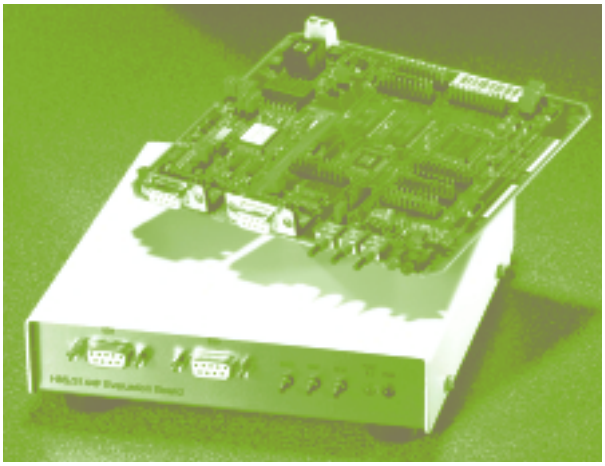


F P - 8 0 A



T F P - 1 0 0 G

Tools *



Good tools are paramount to the successful development of a microcontroller based application. The trend to greater system integration and the increased complexity of new designs has demanded that high quality, professional support tools are available for all stages of the design process. Hitachi has chosen not only to follow the market trend, but to develop support tools which are powerful, highly integrated, innovative and simple to use, and thus to provide it's customers with market leading development tools.

Evaluation boards

Hitachi provides a full set of quality, low cost Evaluation boards for its 16-bit microcontrollers. These can be used to:

- evaluate suitability of the device for an application, e. g. to run benchmarks
- develop software, while the hardware engineers use emulators
- build prototypes of a system quickly.

Each kit contains everything an engineer needs to get started (only a power supply is needed in addition):

- evaluation board in a metal case (CE marked), containing H8/H8S microcontroller, external SRAM, 2 serial ports, LED's, RESET and NMI push buttons and headers to access all microcontroller signals
- serial cable
- HDI-M monitor software
- GNU and in most cases IAR C-Compiler software (IAR Compiler in evaluation version)
- Tutorials, installation manual incl. Circuit diagrams, device manuals and all the software manuals in electronic format
- For evaluation boards using Flash microcontrollers, also Hitachi's Flash programming software is included.

These Evaluation boards are available for the following microcontrollers

Device family	Evaluation Board
H8/3048F (also H8/304x)	EVB3048F
H8/3067F (also H8/3062F)	EVB3067F
H8S/2144F (also H8S/2134F)	EVB2144F
H8S/2655	EVB2655
H8S/2357F (also other 23xx)	EVB2357F
H8S/2633F	EVB2633F
H8S/2623F	EVB2623F

Emulators

Hitachi provides fully-featured in-circuit, real-time emulators for all of its devices, at a very competitive price/performance ratio.
The first-generation H8/300H devices are supported by PCE's (PC based emulators). These feature:

- zero-wait, real-time, in-circuit emulation up to 16MHz
- soft- and hardware breakpoints
- trace buffer for address, data, transfer type, interrupt mask and user probes
- 3V and 5V support (were appropriate)
- emulator control via HDI software, featuring the same GUI like HDI-M on the Evaluation boards
- .... and much more

H8S as well as the second-generation H8/300H devices are supported by Hitachi's new highly sophisticated E6000 emulator. While remaining low cost, E6000 provides a wealth of state-of-the-art features that allow design engineers to quickly get their system up and running:

- zero-wait, real-time, in-circuit emulation up to 40MHz
- soft- and hardware breakpoints based on a 'Complex event system' (CES) that allows event sequencing
- trace buffer for address, data, transfer type, interrupt mask and user probes, featuring acquisition filtering
- timing/performance analysis with a resolution as low as 20ns
- 3V and 5V support (were appropriate)
- emulator control via HDI software, featuring the same GUI like HDI-M on the Evaluation boards

*For a detailed description of our tools order literature number 17-001

All of Hitachi's emulators can also be bought together wit a full kit of software, including Assembler, C-Compiler, HDI debugger and MakeApp (see below). These popular kits are listed below, please inquire with Hitachi or your authorised Hitachi distributor if you require the emulator hardware (incl. HDI) only.

Device families	Emulator kit
H8/3001, 2,3,4,5 H8/3032, 3042	S5-3003
H8/3048, 3052	S6-3048
H8/3048-series	S5-3048F
H8/306x, 3039	S6-3067
H8S/21xx	S6-2148R
H8S/265x, 234x,5x, 224x	S6-2655/4
H8S/231x, 2x	S6-2338**
H8S/233x, 223x	S6-2633**
H8S/262x	S6-2623**

*** available in 1Q00*

Please note that these kits do not contain the target cables, which are needed to connect the emulator to your target hardware, because each emulator supports many devices of various packages and pin outs.

C-Compiler / Hitachi Workbench

Hitachi's C-Compiler is designed to exercise close control over the hardware of the microcontroller, for example using in-line function calls, or by allowing interrupt service routines being written directly in 'C'. It is also highly optimising for the H8/H8S families, with the ability to select optimisation for speed or code size.

It is being operated under a user-friendly, project oriented Windows 95 GUI, called Hitachi Workbench (HWB). Therefore engineers can quickly concentrate on writing their software instead of trying to make the Compiler work. The time spent on learning how to operate the tool is short, errors in usage are reduced and the project is kept under tight control.

Features of the HWB are:

- split screen viewing
- multiple edit windows open at one time
- context sensitive coloration
- bookmarks, templates, brace matching and much more...
- automatic placement of the cursor at the location causing a compilation error, displaying a button to jump from one error to the next, if there are several errors.
- Graphical configuration of Compiler and Linker options

The following table lists the target cables for each family/package.

Family	Series	Footprint	Header*
H8/300H	H8/3001	FP-80A1	PHB300HQ80A1
		TFP-80C1	PHB300HT80C1
	H8/3030,1,2,3,4,5	FP-80A2	PHB300HQ80A2
		TFP-80C2	PHB300HT80C2
	H8/3004,5	FP-80A3	PHB300HQ80A3
		TFP-80C3	PHB300HT80C3
	H8/3002, H8/3040,1,2, H8/3044,7,8	FP-100B, TFP-100B	PHB300HQ100B
	H8/3003	FP-112	PHB300HQ112
	H8/3036,7,8,9	FP-80A	EHB3039Q80A
	H8/306x, 3006, 7	FP-100B, TFP-100B	EHB3067Q100B
H8S	H8S/212x	DP-64S	EHB2128D64S
		FP-64A	EHB2128Q64A
	H8S/213x	FP-80A	EHB2138Q80A
		TFP-80C	EHB2138T80C
	H8S/214x	FP-100B, TFP-100B	EHB2148Q100B
	H8S/223x	FP-100B, TFP-100B	EHB2238Q100B
		TFP-100G	EHB2238T100G
	H8S/224x	FP-100B, TFP-100B	EHB2200Q100B
	H8S/232x	FP-128	EHB2328Q128
		TFP-120	EHB2328T120
	H8S/234x	FP-100B, TFP-100B	EHB2345Q100B
	H8S/235x, H8S/265x	FP-128	EHB2600Q128
		TFP-120	EHB2600T120
	H8S/2623	FP-100B	EHB2623Q100B
	H8S/2633	FP-128	EHB2633Q128
		TFP-120	EHB2633T120

**Note: PHB - are for PCE emulators*
EHB - are for E6000 emulators

HDI Debugger

HDI is Hitachi's debugging interface used for all development tools ranging from evaluation boards to emulators. This enables engineers to move painlessly from one platform to the next, without having to learn another user interface.

HDI is a C-source-level debugger, that allows to display 'C' code and for example single-step through it or to set breakpoints on C-statements. The corresponding assembler code can be displayed as well, or the C statements can be shown interleaved with assembler.

HDI allows to display CPU registers, control registers, memory, variables, etc.

Control over the hardware is exercised via convenient menus using for example radio buttons for mutually exclusive options, thus reducing usage errors.

MakeApp

MakeApp is a visual development tool, which automatically creates device drivers for all the on-chip peripherals. It provides a point and click mechanism to configure all of the peripherals and then to generate well tested and documented 'C' source code.

Each peripheral is presented to the user to configure, dialogues are clear and provide the user with selections rather than edit boxes.

MakeApp also checks for resource conflicts, ensuring that there will be no problem when several pieces of code are integrated into one.

Advanced drivers, for example a DMA transfer triggered by a timer, can be created with a few simple mouse strokes.

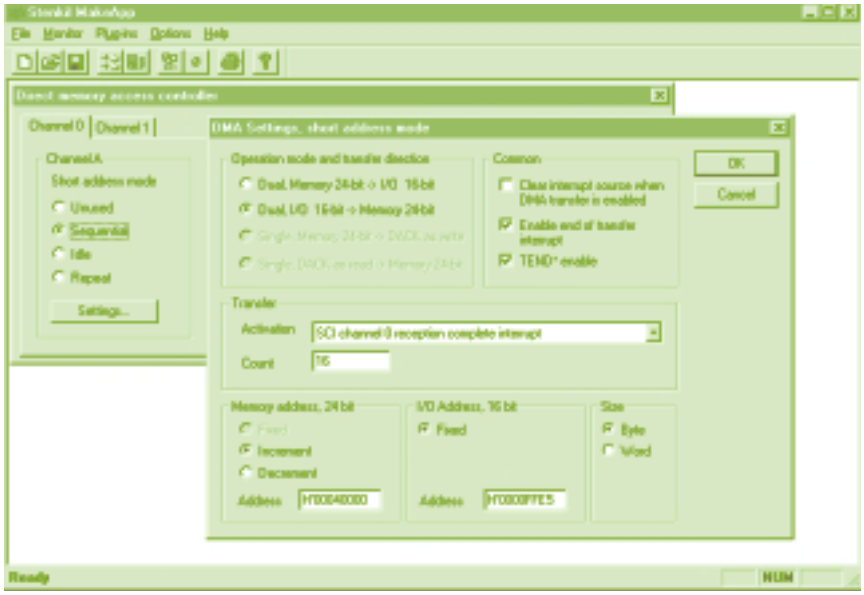
The 'C' source code files created can be easily included in HWB projects.

FLASH programming software (FDT)

Hitachi provides free Windows software which conveniently supports programming its Flash microcontrollers. The software provides the following functions (excerpt):

- Blank check
- Read flash memory
- Program flash memory (with verify)
- Erase flash memory

The software is designed to operate with Hitachi's programming boards (supplied with the evaluation boards) or with customers hardware. The boot kernel (the part of the software which is downloaded into the H8) is supplied as 'C' source code, to allow customization.



Third Party **Tools**

Third Party Emulators

H8/300H and H8S are being supported by several renowned third party emulator manufacturers. These are:

UK: **01256 811998**
email: sales@ash-uk.demon.co.uk

Germany: **08233/32681**
email: ashling.ger@t_online.de

France: **(1) 46 66 27 50**
email: ash-fr@world_net.sct.fr

Rest of Europe: **353 61 334466**
email: ashling@iol.ie

Lauterbach Datentechnik GmbH,
Fichtenstr. 27,
D-85649 Hofolding, Germany.
Tel: +49 (08104)-8943-0
Fax: +49 (08104)-8943-30
E-mail: info@lauterbach.com
www:
http://www.lauterbach.com

Third Party **Operating** Systems

Third party operating systems that support H8/300H and H8S are available from ATI and TECSI. Both companies offer modern real time operating systems that feature a compact memory footprint of only a few Kbyte of memory and a fast interrupt response in the order of only 20µs.
Please find the contact details below:

Accelerated Technology
INCORPORATED

Information can be found on the WWW at
http://www.atinucleus.com

Geoff Gibson (UK)
Phone: +44 152 766 632
Fax: +44 152 764 487
geoffatuk@cityscape.co.uk

Michelle Anderson (USA)
Tel: +1 334 661 5770
Fax: +1 334 661 5788
manderson@atinucleus.com

Michel Genard (France)
Phone: +33 160 924 111
Fax: +33 169 290 919

Udo Nuelle (Germany)
Phone: +49 5143 93543
Fax: +49 5143 93544

Tecsi, 18, place des Reflets,
92975 Paris La Defense Cedex;
Tel: +33 1 47 78 67 67
Fax: +33 1 47 78 67 68
E-mail nc@tecsi.com

EPROM Programmers

In order to program H8/H8S OTP and Flash devices EPROM programmers and programming adapters are required. These are available from the following companies:

Data I/O
Contact: +44-1280-700262
Dataman
Contact: +44-1300-320719
Lloyd Research
Contact: +44-1489-574040
Minato Electronics Inc
Contact: +44-181 953 9292
MPQ
Contact: +44-1666-825666
SMS Holdings
Contact: +49-7521-97280
Stag Micro-systems
Contact: +44-1707-332148

Related Literature / Internet / CD-ROM

Shortforms for Hitachi Microcontroller	Literature no.
'H8/300 & H8/300L' Hitachi's single chip, low power H8 family	21-017
'Microcontrollers support tools'	17-001
'Integrated Systems LSI'	02-038
'LCD controllers/drivers'	06-003
'SuperH RISC engine'	19-017

Data books	Literature no.
H8/3001	21-092
H8/3002	21-078
H8/3003	21-033
H8/3004 and 3005	21-106
H8/3032 series	21-093
H8/3035 series	21-111
H8/3048 series	21-095
H8/3067F series	21-115
H8/3062F series	21-116
Programming manual	21-032
H8S/2655 series	18-001
H8S/2245 series	18-004
H8S/2237,2227 series	18-012
H8S/2238F	18-020
H8S/2345 series	18-010
H8S/2350 series	18-006
H8S/2357F series	18-011
H8S/2328 series	18-021, 022
H8S/212x series	18-016
H8S/213x series	18-018
H8S/214x series	18-017
H8S technical Q&A	18-007
Programming manual	18-003

Hitachi CD-ROM 'Hitachi Electronic Components Databook 16-008

This CD-ROM is available free of charge from Hitachi or our authorized distributors.
Please ring ++49-(0)89-99180-128 to order your copy or send a fax to ++49-(0)89-99180-265.
It contains appr. 20. 000 pages of Hitachi documentation about microcontrollers, memories and packages. This includes the actual hardware manuals for almost all our microcontrollers, as well as application notes, programming manuals and overviews.
A powerful selection tool allows you to run a selection to find out which Hitachi microcontrollers are suitable for your application. The CD-ROM is usable under Windows and Macintosh.

Internet access / WWW

Under Hitachi's Electronic Components Group (ECG) homepage (address URL: www. hitachi-eu.com/micro) you can access detailed technical product information about Hitachi's microcontrollers, memory, displays, ASIC, discretes & power modules and optoelectronic components. For memory and microcontroller products each user can download complete data sheets and application notes in PDF format.
You will also find a complete overview over Hitachi's European Microcontroller development tools with a short description, the package contents and the ordering information (part names).

The application notes listed are available for Hitachi's 16-bit microcontrollers. You will find them on our CD-ROM as well as on Hitachi's web-site (address URL: http://www. hitachi-eu. com/hel/ecg/index. htm). Please note that most of these application notes are easily modified to be used on H8S.

Application Notes	No.
DMA request and Transfer time on H8/300H	Apps/012/1.0
Interfacing various bit-size DRAMS to the H8/300H	Apps/013/1.0
Add. the damping resistor to the osc. line of the H8/3003	Apps/014/1.0
Enabling DMA end-of-transfer interrupts on the H8/300H	Apps/015/1.0
Multiplexed I/O Functions on the H8/3003 & H8/304x	Apps/016/1.0
H8/300H Instruction Timing	Apps/017/1.0
H8-3042 Framework Program	Apps/032/1.1
300H ITU Configuration Example 1	Apps/033/1.0
H8/300H Software UART implem. using 2 Timer and 2 DMA channels	Apps/036/1.0
SPI simulation using Synch. Comm. Interface of the 300H	Apps/037/1.0
H8/300H Bootloader	Apps/042/1.0
H8/300H DMAC Example	Apps/044/1.0
H/300H DMAC-Serial Communication Example	Apps/045/1.0
H8/300H CS0 During Software Standby	Apps/047/2.1
LCD character module control using H8/300H	Apps/048/1.1
Producing Optimised C for 300/300H Controllers	Apps/049/1.1
Access Speed on the H8/300H	Apps/050/1.2
MakeApp + output patterns with the TPC, ITU and DMAC of the H8/3003	Apps/056/1.0
Interfacing the H8/3334, 3048 and the HD44780 LCD driver	Apps/059/1.0
Interfacing the H8 300H to the LCM EVB	Apps/062/1.0
Connecting an external power supply to the PCE300H	Apps/065/1.0
Current Dissipation of H8/3003 measured using the EVB3003	Apps/066/1.0
Using QFP sockets and Hitachi Emulators	Apps/067/1.0
Interfacing the H8 and the HD66712 LCD driver	Apps/068/1.0
Dhrystone performance H8, H8S, SH	Apps/073/1.0
Generating H8S code with GNU compiler V97RIA	Apps/079/1.0
Understanding the H8 Series Instruction Prefetch	Apps/082/1.0
Key Matrix on H8S/21xx	Apps/083/1.0


H8S/2238
HD
64F2238TE
JAPAN

HITACHI http://www.hitachi-eu.com/hel/ecg/

Hitachi Europe Ltd
Electronic Components Group
(Northern Europe)

Headquarters:
Whitebrook Park, Lower Cookham Road,
Maidenhead, Berkshire SL6 8YA UK
Tel: (Local) (01628) 585000
(INT) (+44) 1628 585000
Fax: (Local) (01628) 585160
(INT) (+44) 1628 585160

Sales Offices:
Denmark
Egebækvej 98, 2850 Nærum
Tel: (+45) 45 80 77 11
Fax: (+45) 45 80 77 54

Finland
Tap House Tapiolan Keskustorni 11 krs
02100 Espoo.
Tel: (+358) 9 455 2488
Fax: (+358) 9 455 2152

Norway
P.O.Box 153, Østre Strandvei 4B,
N-3482 Tofte
Tel: (+47) 32 79 51 11
Fax: (+47) 32 79 52 30

Sweden
Haukadalsgaten 10, Box 1062,
S-16421 Kista, Stockholm
Tel: (+46) 85 62 712 00
Fax: (+46) 87 51 50 73

Eire
Odeon House, Eyre Square
Galway, Eire
Tel: (+353) 91 56 20 20
Fax: (+353) 91 56 20 14

France
Hitachi Europe (France) S.A.
18, rue Grange Dame Rose, B.P 134
F-78148 Veliz Cedex, France
Tel: (+33) 1 34 63 05 00.
Fax: (+33) 1 34 65 34 31

Hitachi Europe GmbH
Electronics Components Group
Continental Europe

Sales Offices:
Germany
Dornacher Str. 3; D-85622 Feldkirchen
Postfach 2 01: D-85619 Feldkirchen
Tel: (Local) (0 89) 9 91 80 0
(INT) (+49) 89 99 1800
Fax: (Local) (0 89) 9 29 30 00
(INT) (+49) 89 929 3000

North Germany/Benelux
Am Seestern 18; D40547 Dusseldorf
Postfach 11 05 36; D-40505 Dusseldorf
Tel: (+49) 02 11 52 83-0
Fax: (+49) 02 11 52 83-7 79

Central Germany
Friedrich-List-Str. 42;
D-70771 Leinfelden-Echterdingen
Tel: (+49) 7 11 9 90 85-5
Fax : (+49) 7 11 9 90 85-99

South Germany/Austria
Dornacher Str. 3;D-85622 Feldkirchen
Tel: (+49) 089 9 91 80.
Fax: (+49) 089 9 91 80-266

Italy
Via Tommaso Gulli, 39 1-20147, Milano
Tel: (+39) 2 48 78 61
Fax: (+39) 2 48 78 63 91

Via F.D'Ovidio, 1-00135 Roma
Tel: (+39) 6 82 00 18 24
Fax: (+39) 6 82 00 18 25

South Africa
7th Floor, Nedbank Gardens, 33 Bath Avenue,
Rosebank 2196 (Jb)
Tel: (+27) 11 44 290 80
Fax: (+27) 11 442 9745

Spain
c/Bunganvilla , 5; E-28036 Madrid
Tel: (+34) 91 7 67 27 82, - 92
Fax: (+34) 91 3 83 85 11

Nissei Sangyo GmbH*

Nissei Sangyo GmbH (Deutschland)
Germany
Dorncher Str. 3, D-85622 Feldkirchen
Tel: (Local) (0 89) 9 91 30 0
(INT) (+49) 89 9 91 30 0
Fax: (Local) (0 89) 9 29 11 85
(INT) (+49) 89 9 29 11 85

Kurfurstendamm 115b
D-10711 Berlin
Tel: (+49) 30 89 36 81-0
Fax: (+49) 30 8 91 10 31

Hungary
East-West Business Center; Rakoczi UT 1-3
H-1088 Budapest
Tel: (+36-1) 2 66 66 58.
Fax: (+36-1) 2 66 - 49 27

Spain
Gran Via Carlos III, 101 1°;
E-08028 Barcelona
Tel: (+34) 34 90 - 78 01
Fax: (+34) 33 39 - 78 39

Nissei Sangyo France S.A.R.L.*
France
Immeuble Ariene; 18 rue Grange Dame Rose
F-78140 Velizy Cedex
Tel: (+33) 1 30 70 69 70
Fax: (+33) 1 34 65 77 28

Nissei Sangyo Co. Ltd.* United Kingdom
Whitebrook Park, Lower Cookham Road,
Maidenhead, Berkshire SL6 8YA
Tel: (Local) (01628) 585000
(INT) (+44) 1628 585000
Fax: (Local) (01628) 585160
(INT) (+44) 1628 585160

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