National Semiconductor

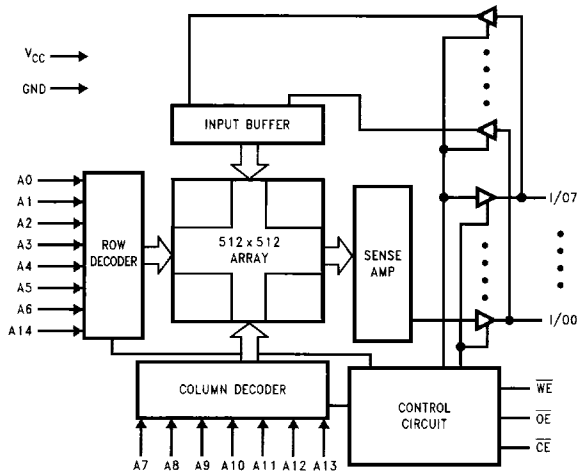
ADVANCE INFORMATION

NMS256X8LV
High Performance 32K x 8 CMOS SRAM with Low Operating Voltage

Features

- Organization: 32,768 words x 8 bits
- Power Supply: V_{CC} = 3.3V ±0.3V
- Specifications optimized for notebook/laptop applications at 25/33/40 MHz
- High Speed:
  — 20/25/35 ns t_{AA} access time
  — 5/5/8 ns t_{OE} access time
- Low Standby Current:
  Full standby current of 50 µA maximum
- 2V Data Retention for battery back-up operations
  Data Retention current of 20 µA maximum
- TTL compatible inputs and outputs
- Reduced power consumption after initial access for notebook/laptop computer applications
- Automatic power-down when de-selected
- Completely static memory. No clocks or timing strobe required
- Equal access and cycle times
- JEDEC standard compatible pinout
- Slim 300 mil 28-pin plastic DIP as well as a J-bend, SOJ package for high board density
- ESD protection exceeds 2000V
- Latch-up current ≥ 200 mA

Logic Block Diagram



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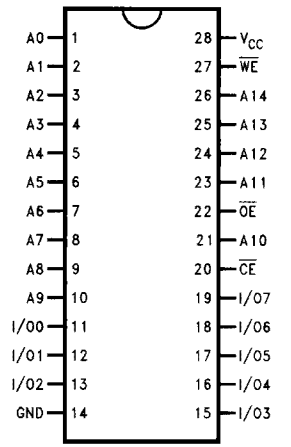
Pin Arrangement

28-Pin DIP/SOJ



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Selection Guide

		NMS256X8LV-20	NMS256X8LV-25	NMS256X8LV-35
Maximum Access Time (ns)		20	25	35
Maximum Operating Current (mA)		60	55	55
	L	55	50	50
Maximum Standby Current (mA)		1.0	1.0	1.0
	L	0.05	0.05	0.05