μPD27C512
65,536 x 8-BIT CMOS UV EPROM

Description

The μPD27C512 is an ultraviolet erasable, electrically programmable 524,288-bit ROM fabricated with an advanced CMOS process for substantial power savings. The device is organized as 64K words by 8 bits and operates from a single +5-volt power supply. All inputs and outputs are TTL-compatible. The device is available in a 28-pin cerdip package with quartz window.

Features

- ☐ 64K x 8-bit organization
- ☐ Ultraviolet erasable and electrically programmable
- ☐ High-speed programming mode
- ☐ Low power dissipation
  - — 30 mA max (active)
  - — 100 μA max (standby)
- ☐ TTL-compatible inputs and outputs
- ☐ Single +5-volt power supply
- ☐ Three-state outputs
- ☐ Advanced CMOS technology
- ☐ 28-pin cerdip with quartz window

Ordering Information

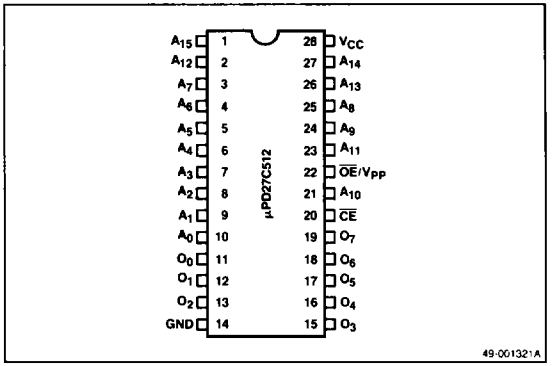
Part Number	Access Time (max)	Package
μPD27C512D-15	150 ns	28-pin cerdip with quartz window
D-20	200 ns	

Pin Identification

Symbol	Function
A_0-A_{15}	Address inputs
O_0-O_7	Data outputs
$\overline{CE}$	Chip enable
$\overline{OE}/V_{PP}$	Output enable/program voltage
GND	Ground
V_{CC}	Power supply

Pin Configuration

28-Pin Cerdip

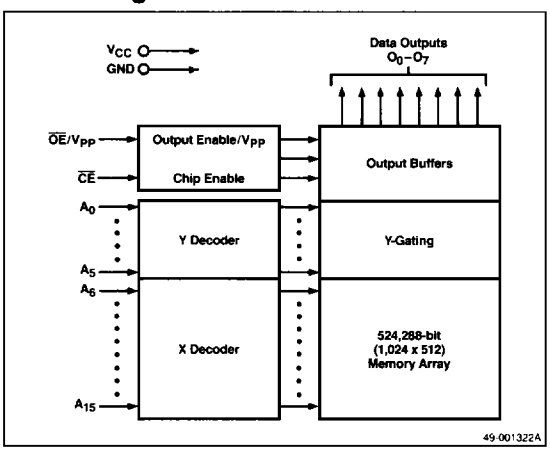


Absolute Maximum Ratings

Output voltage, V_O	−0.6 to +7.0 V
Input voltage, V_I	−0.6 to +7.0 V
Input voltage, A_9	−0.6 to +13.5 V
Supply voltage, V_{CC}	−0.6 to +7.0 V
Supply voltage, V_{PP}	−0.6 to +13.5 V
Operating temperature, T_{OPR}	−10 to +80°C
Storage temperature, T_{STG}	−65 to +125°C

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Block Diagram



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Mode Selection

Mode	$\overline{CE}$	$\overline{OE}/V_{PP}$	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	+5 V	D_{OUT}
Output disable	V_{IL}	V_{IH}	+5 V	High-Z
Standby	V_{IH}	X	+5 V	High-Z
Program	V_{IL}	V_{PP}	+6 V	D_{IN}
Program verify	V_{IL}	V_{IL}	+6 V	D_{OUT}
Program inhibit	V_{IH}	V_{PP}	+6 V	High-Z

Notes:

(1) X = V_{IL} or V_{IH}

Capacitance

T_A = 25 °C; f = 1 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IN1}			6	pF	V_I = 0 V
	C_{IN2}			20	pF	$\overline{OE}/V_{PP}$; V_I = 0 V
Output capacitance	C_{OUT}			12	pF	V_O = 0 V

DC Characteristics

T_A = 0 to +70 °C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Read and Standby Modes						
Input voltage, high	V_{IH}	2.0		V_{CC} + 0.3	V	
Input voltage, low	V_{IL}	−0.3		0.8	V	
Output voltage, high	V_{OH1}	2.4			V	I_{OH} = −400 μA
	V_{OH2}	V_{CC} − 0.7			V	I_{OH} = −100 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Output leakage current	I_{LO}			10	μA	V_O = 0 to V_{CC}; $\overline{OE}$ = V_{IH}
Input leakage current	I_{LI}			10	μA	V_I = 0 to V_{CC}
V_{CC} current, active	I_{CCA1}			30	mA	$\overline{CE}$ = V_{IL}; V_I = V_{IH}
	I_{CCA2}			30	mA	f = 5 MHz; I_{OUT} = 0 mA
V_{CC} current, standby	I_{CCS1}			1	mA	$\overline{CE}$ = V_{IH}
	I_{CCS2}		1	100	μA	$\overline{CE}$ = V_{CC}; V_I = 0 to V_{CC}
Programming Modes						
T_A = 25 ±5 °C; V_{CC} = 6.0 ±0.25 V; V_{PP} = 12.5 ±0.3 V						
Input voltage, high	V_{IH}	2.0		V_{CC} + 0.3	V	
Input voltage, low	V_{IL}	−0.3		0.8	V	
Input leakage current	I_{LI}			10	μA	V_I = V_{IL} or V_{IH}
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −400 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
V_{PP} current	I_{PP}			30	mA	$\overline{CE}$ = V_{IL}; $\overline{OE}/V_{PP}$ = V_{IH}
V_{CC} current	I_{CC}			30	mA	

AC Characteristics, Read and Standby Modes

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	Limits μPD27C512-15 Min	Limits μPD27C512-15 Max	Limits μPD27C512-20 Min	Limits μPD27C512-20 Max	Unit	Test Conditions
Address to output delay	t_{ACC}		150		200	ns	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$
$\overline{CE}$ to output delay	t_{CE}		150		200	ns	$\overline{OE}/V_{PP} = V_{IL}$
$\overline{OE}/V_{PP}$ to output delay	t_{OE}		75		75	ns	$\overline{CE} = V_{IL}$
$\overline{OE}/V_{PP}$ high to output float	t_{DF}	0	60	0	60	ns	$\overline{CE} = V_{IL}$
Output hold from address, $\overline{CE}$ or $\overline{OE}$, whichever transition occurs first	t_{OH}	0		0		ns	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$

Notes:

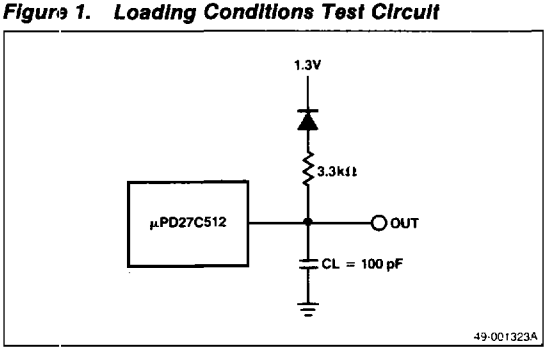
(1) Output load: see figure 1. Input rise and fall times ≤ 20 ns. Input pulse levels: 0.45 and 2.4 V. Timing measurement reference levels: inputs and outputs = 0.8 and 2.0 V

AC Characteristics, Programming Modes

T_A = 25 ±5°C; V_{CC} = 6.0 ±0.25 V; V_{PP} = 12.5 ±0.3 V

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Address setup time	t_{AS}	2			μs	
$\overline{OE}$ setup time	t_{OES}	2			μs	
Data setup time	t_{DS}	2			μs	
Address hold time	t_{AH}	2			μs	
Data hold time	t_{DH}	2			μs	
$\overline{CE}$ to output float time	t_{DF}	0		130	ns	
V_{CC} setup time	t_{VCS}	2			μs	
Initial program pulse width	t_{PW}	0.95	1.0	1.05	ms	
Overprogram pulse width	t_{OPW}	2.85		78.75	ms	
$\overline{CE}$ to output delay	t_{DV}			1	μs	$\overline{OE}/V_{PP} = V_{IL}$
$\overline{OE}/V_{PP}$ hold time	t_{OEH}	2			μs	
$\overline{OE}/V_{PP}$ recovery time	t_{VR}	2			μs	
$\overline{OE}/V_{PP}$ rise time	t_{PRT}	50			ns	

Figure 1. Loading Conditions Test Circuit



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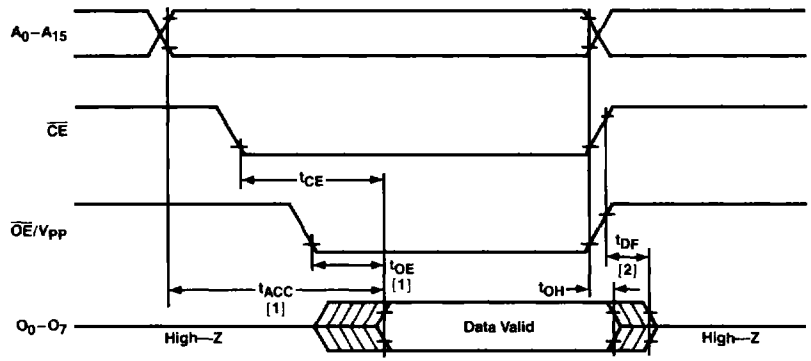
Timing Waveforms

Read Mode



Notes:

[1] $\overline{OE}/V_{PP}$ *may be delayed up to* $t_{ACC}-t_{OE}$ *after the falling edge of* $\overline{CE}$ *for read cycles without affecting* t_{ACC}.

[2] t_{DF} *is specified from* $\overline{OE}/V_{PP}$ *or* $\overline{CE}$, *whichever occurs first.*

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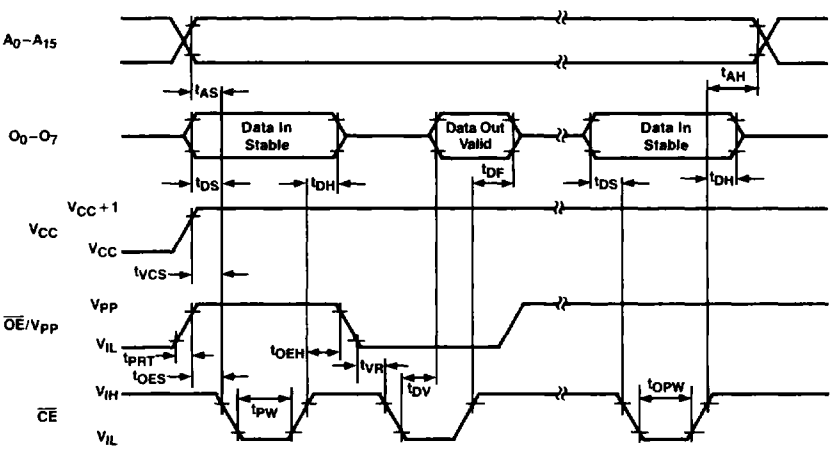
Programming Mode



Notes:

[1] V_{CC} *must be applied before or simultaneously with* $\overline{OE}/V_{PP}$ *and removed after or simultaneously with* $\overline{OE}/V_{PP}$.

[2] V_{PP} *must not be greater than +13.0 V, including overshoot.*

[3] *Removing and reinserting the device while a voltage of 12.5 V is applied to pin* V_{PP} *may affect device reliability.*

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Programming Operation

High-Speed Programming Mode

Begin programming by erasing all data; this places all bits in the high-level (1) state. Enter data by programming a low-level (0) TTL signal into the chosen bit location.

Address the first location and apply valid data at the eight output pins. Raise V_{CC} to +6 V ±0.25 V; then raise $\overline{CE}/V_{PP}$ to +12.5 V ±0.3 V. Apply a 1-ms (±5%) program pulse to $\overline{CE}$ as shown in the programming mode timing waveform. The bit is verified and the program/no-program decision is made. If the bit is not programmed, apply another 1-ms pulse to $\overline{CE}$, up to a maximum of 25 times. If the bit is programmed within 25 tries, apply an additional overprogram pulse of "x" ms (where "x" equals the number of tries multiplied by 3) and input the next address. If the bit is not programmed in 25 tries, reject the device as a program failure.

Programming Inhibit Mode

Use the programming inhibit mode to program multiple μPD27C512s connected in parallel. All like inputs (except $\overline{CE}$, but including $\overline{OE}/V_{PP}$) may be common. Program individual devices by applying a low-level (0) TTL pulse to the $\overline{CE}$ input of the μPD27C512 to be programmed. Applying a high level (1) to the $\overline{CE}$ input of the other devices prevents them from being programmed.

Program Verify Mode

Perform verification on the programmed bits to determine that the data was correctly programmed. The program verification can be performed with $\overline{CE}$ and $\overline{OE}/V_{PP}$ at low levels (0).

Erasure

Erase data on the μPD27C512 by exposing it to light with a wavelength shorter than 400 nm. Exposure to direct sunlight or fluorescent light could also erase the data. Consequently, mask the window to prevent unintentional erasure by ultraviolet rays.

Data is typically erased by 254-nm ultraviolet rays. A minimum lighting level of 15 W sec/cm^2 (ultraviolet ray intensity multiplied by exposure time) is required to completely erase written data.

An ultraviolet lamp rated at 12,000 μW/cm^2 takes approximately 15 to 20 minutes to complete erasure. Place the μPD27C512 within 2.5 cm of the lamp tubes. Remove any filter on the lamp.

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