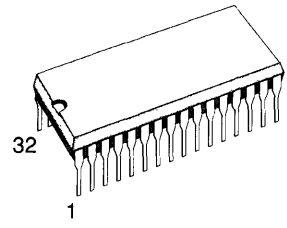
1024K (128K x 8) CMOS ROM

- VERY FAST ACCESS TIME : 100 ns (Chip select or address access time)
- LOW POWER "CMOS" CONSUMPTION :
  - Operating current 40 mA Max.
  - Standby current 20 µA Max.
- SINGLE +5V ± 10% POWER SUPPLY.
- STATIC OPERATION.
- INPUTS AND OUTPUTS TTL COMPATIBLE.
- THREE STATE OUTPUTS.
- MASK PROGRAMMABLE ACTIVE LOW/HIGH $\overline{CE}$.
- AUTOMATIC POWER DOWN.



PDIP-32

(Ordering information at the end of the datasheet)

DESCRIPTION

The M23C1001 Is a 1, 048,576 bit, CMOS Masked Read Only Memory (ROM), organized as 131,072 x 8 bits. It is manufactured in 1.2 micron CMOS technology : Very fast access time of 100 ns makes it ideal for EPROM replacement on high performance, high volume running applications. Chip select line ($\overline{CE}$) is active low or active high by mask programming, as per user's choice When not active, it brings the device into standby mode making it suitable for battery operated systems.

After cycle completion and 50 ns without input change, the M23C1001 automatically goes into power-down mode (I_{CC} = 1 mA), the data remaining latched on the output.

PIN FUNCTIONS

A0-A16	ADDRESS INPUTS
00-07	DATA OUTPUTS
$\overline{CE}$ / CE	CHIP ENABLE INPUT
$\overline{OE}$	OUTPUT ENABLE
V_{CC}	+5V POWER SUPPLY
GND	GROUND

Figure 1 : Pin Connection

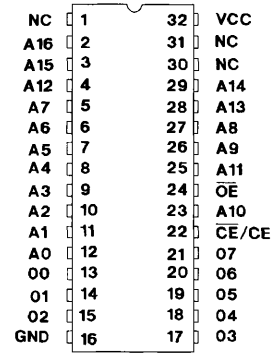
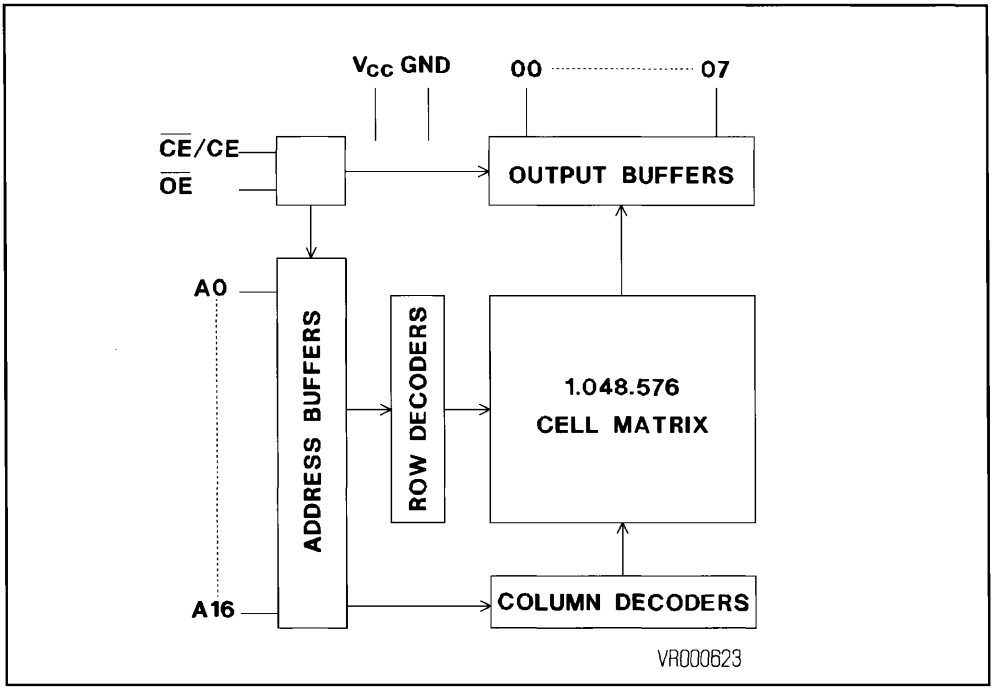


Figure 2 : Block Diagram



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage with respect to Ground	-0.5 to + 7.0	V
Vi	Input or Output voltage with respect to Ground	-0.5 to + 7.0	V
T_{amb}	Operating temperature range	0 to + 70	°C
T_{bias}	Temperature range under bias	0 to + 125	°C
T_{stg}	Storage temperature	-65 to + 150	°C

NOTE : Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation to these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rated conditions for extended periods of time may affect device reliability.

AC TEST CONDITION

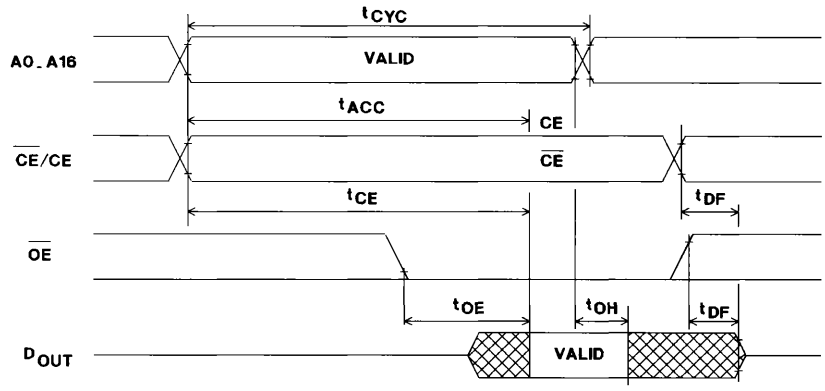
Input Rise and Fall Times : ≤ 10 ns

Input Levels : 0.45V and 2.4V

Timing measurement Reference Levels :

Inputs : 0.8V and 2.0V - Outputs : 0.8V and 2.0V

Figure 3 : Timing Waveforms



OPERATION MODES

MODE	$\overline{CE}$	or ($\overline{CE}$)	$\overline{OE}$ (Note 1)	OUTPUTS
READ	L	(H)	L	DOUT
STANDBY	H	(L)	X	HIGH Z
OUTPUT DISABLE	L	(H)	H	HIGH Z

DC CHARACTERISTICS

T_{AMB} = 0°C to 70°C V_{CC} = 5V ± 10%

Symbol	Parameter	Test Condition	Values		Unit
			Min	Max	
I_{LI}	Input Leakage current	V_{IN} = 0 V to V_{CC}	-10	10	µA
I_{LO}	Output Leakage current	V_{IN} = 0 V to V_{CC}	-10	10	µA
I_{CC1}	V_{CC} Active Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, I_{OUT} = 0 mA (f = 10 MHz)		40	mA
I_{CC1}	V_{CC} Active Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, I_{OUT} = 0 mA (f = 5 MHz)		20	mA
I_{CC2}	V_{CC} Standby Current - TTL	$\overline{CE}$ = V_{IH}		1	mA
I_{CC3}	V_{CC} Standby Current - CMOS	$\overline{CE}$ > V_{CC} - 0.2 V		20	µA
V_{IL}	Input Low Voltage		-0.5	0.8	V
V_{IH}	Input High voltage		2.0	V_{CC} + 1.0	V
V_{OL}	Output Low voltage	I_{OL} = 3.2 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 uA	2.4		V

NOTE 1 : OE may be active high by mask programming.

AC CHARACTERISTICS

Symbol	Parameter	Test Condition	Values		Unit
			Min	Max	
T_{CYC}	Cycle Time			100	ns
T_{ACC}	Address Access Time	$\overline{CE} = V_{IL}$		100	ns
T_{CE}	Chip Enable Access Time	$\overline{CE} = V_{IL}$		100	ns
T_{OE}	Output Enable Access Time	$\overline{CE} = \overline{OE} = V_{IL}$		50	ns
T_{DF} (1)	$\overline{CE}$ High to Output float			30	ns
T_{DH}	Output Hold		10		ns

CAPACITANCE (1)

T_{AMB} = 25°C f = 1 MHz

Symbol	Parameter	Test Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		5 pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		5 pF

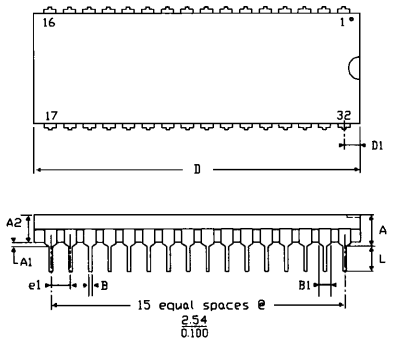
NOTE : (1) This parameter is only sampled and not 100 % tested

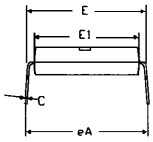
ORDERING INFORMATION

Part Number	Access Time	Supply Voltage	Temp.Range	Package
M23C1001 B1	100 ns	5 V ± -10%	0 to +70°C	PDIP32

PACKAGE MECHANICAL DATA

Figure 4 : 32-PIN - PLASTIC DIP





Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A						
a1	0.38			0.015		
b		0.46			0.018	
b1	0.20		0.30	0.008		0.012
b2		1.27			0.050	
C						
D			42.04			1.655
E		15.24			0.600	
e		2.54			0.100	
e 3		35.60			1.400	
e 4	15.24		15.88	0.600		0.625
F			13.97			0.550
I			4.83			0.190
L	3.18		3.43	0.125		0.135