Preliminary *128K X 8 BIT 3.3V HIGH SPEED CENTER POWER CMOS SRAM*

Features

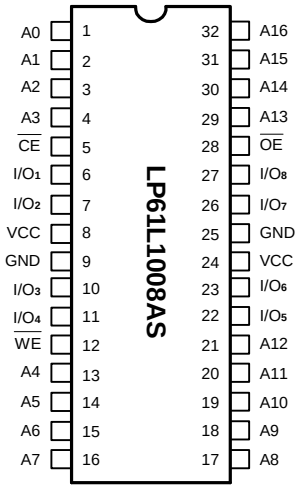
- Single 3.3V ± 10% power supply
- Access times: 8/10/12 ns (max.)
- Current: Operating: 160/155/150mA (max.)
  Standby: 5mA (max.)
- Full static operation, no clock or refreshing required
- All inputs and outputs are directly TTL compatible
- Center Power/Ground Pin Configuration
- Common I/O using three-state output
- Output enable and one chip enable inputs for easy application
- Data retention voltage: 2.0V (min.)
- Available in 32-pin SOJ 300 mil package

General Description

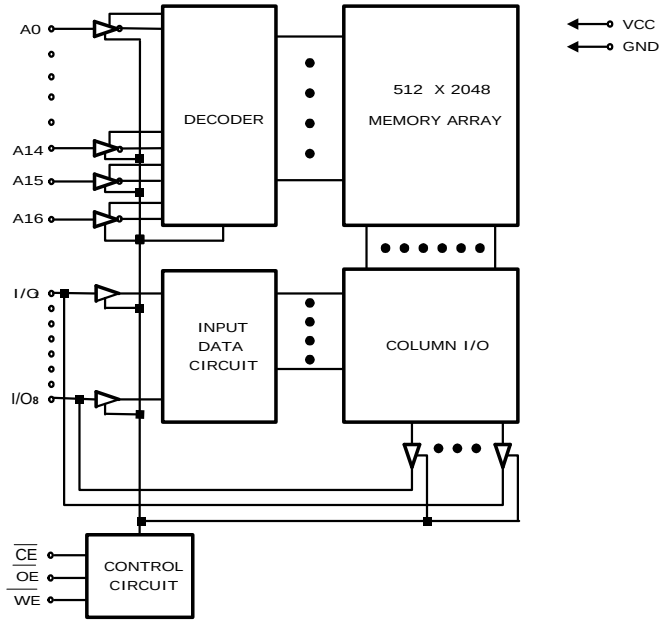
The LP61L1008A is a high speed 1,048,576-bit static random access memory organized as 131,072 words by 8 bits and operates on a single 3.3V power supply.
Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

The chip enable input is provided for POWER-DOWN and device enable and an output enable input is included for easy interfacing.
Data retention is guaranteed at a power supply voltage as low as 2.0V.

Pin Configuration



Block Diagram



Pin Description

Pin No.	Symbol	Description
1 - 4, 13 - 21, 29- 32	A0 - A16	Address Inputs
12	$\overline{WE}$	Write Enable
28	$\overline{OE}$	Output Enable
5	$\overline{CE}$	Chip Enable
6 –7, 10 - 11, 22 – 23, 26 - 27	I/O_1 - I/O_8	Data Input/Outputs
8, 24	VCC	Power Supply
9, 25	GND	Ground

Recommended DC Operating Conditions

(T_A = 0°C to + 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	3.0	3.3	3.6	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	-	VCC + 0.3	V
V_{IL}	Input Low Voltage	-0.3	0	+0.8	V
C_L	Output Load	-	-	30	pF
TTL	Output Load	-	-	1	-

Absolute Maximum Ratings*

VCC to GND ..... -0.5V to +4.6V
IN, IN/OUT Volt to GND .....-0.5V to VCC +0.5V
Operating Temperature, Topr ..... 0°C to +70°C
Storage Temperature, Tstg..... -55°C to +125°C
Power Dissipation, Pt.....1.0W

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(T_A = 0°C to + 70°C, VCC = 3.3V ± 10%, GND = 0V)

Symbol	Parameter		LP61L1008A- 8/10/12		Unit	Conditions
			Min.	Max.		
$\|I_{LI}\|$	Input Leakage Current		-	2	µA	V_{IN} = GND to VCC
$\|I_{LO}\|$	Output Leakage Current		-	2	µA	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = GND to VCC
I_{CC1} (1)	Dynamic Operating Current	-8	-	160	mA	$\overline{CE}$ = V_{IL} $I_{I/O}$ = 0 mA
		-10	-	155		
		-12	-	150		
I_{SB}	Standby Power Supply Current		-	20	mA	$\overline{CE}$ = V_{IH}
I_{SB1}			-	5	mA	$\overline{CE}$ ≥ VCC - 0.2V, V_{IN} ≤ 0.2V or V_{IN} ≥ VCC - 0.2V
V_{OL}	Output Low Voltage		-	0.4	V	I_{OL} = 8 mA
V_{OH}	Output High Voltage		2.4	-	V	I_{OH} = -4 mA

Note: 1. I_{CC1} is dependent on output loading, cycle rates, and Read/Write patterns

Truth Table

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O Operation	Supply Current
Standby	H	X	X	High Z	I_{SB}, I_{SB1}
Output Disable	L	H	H	High Z	I_{CC1}
Read	L	L	H	D_{OUT}	I_{CC1}
Write	L	X	L	D_{IN}	I_{CC1}

Note: X = H or L

Capacitance (T_A = 25°C, f = 1.0MHz)

Symbol	Parameter	Min.	Max.	Unit	Conditions
C_{IN}*	Input Capacitance		6	pF	V_{IN} = 0V
$C_{I/O}$*	Input/Output Capacitance		8	pF	$V_{I/O}$ = 0V

* These parameters are sampled and not 100% tested.

AC Characteristics (T_A = 0°C to +70°C, VCC = 3.3V ± 10%, GND = 0V)

Symbol	Parameter		LP61L1008A-8		LP61L1008A-10		LP61L1008A-12		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle									
t_{RC}	Read Cycle Time		8	-	10	-	12	-	ns
t_{AA}	Address Access Time		-	8	-	10	-	12	ns
t_{ACE}	Chip Enable Access Time	$\overline{CE}$	-	8	-	10	-	12	ns
t_{OE}	Output Enable to Output Valid		-	4	-	5	-	6	ns
t_{CLZ}	Chip Enable to Output in Low Z	$\overline{CE}$	3	-	3	-	5	-	ns
t_{OLZ}	Output Enable to Output in Low Z		0	-	0	-	2	-	ns
t_{CHZ}	Chip Disable to Output in High Z	$\overline{CE}$	-	4	-	5	-	6	ns
t_{OHZ}	Output Disable to Output in High Z		0	4	0	5	2	6	ns
t_{OH}	Output Hold from Address Change		3	-	3	-	5	-	ns

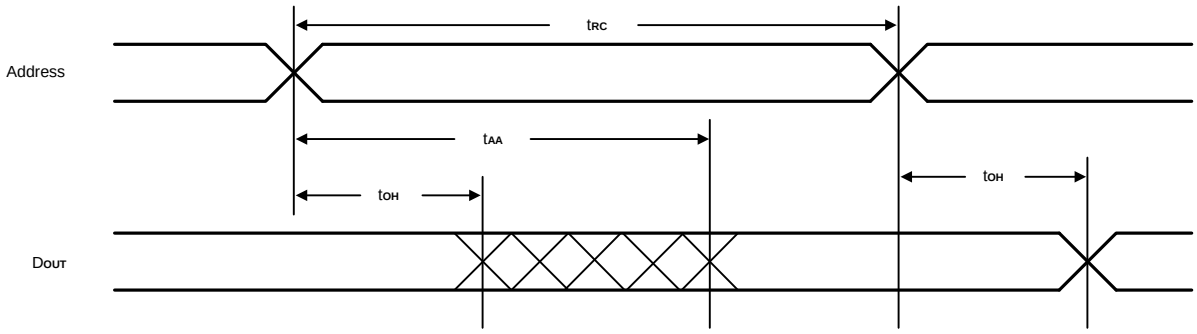
AC Characteristics (continued)

Symbol	Parameter	LP61L1008A-8		LP61L1008A-10		LP61L1008A-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle								
t_{WC}	Write Cycle Time	8	-	10	-	12	-	ns
t_{CW}	Chip Enable to End of Write	6	-	7	-	10	-	ns
t_{AS}	Address Setup Time of Write	0	-	0	-	0	-	ns
t_{AW}	Address Valid to End of Write	6	-	7	-	10	-	ns
t_{WP}	Write Pulse Width	6	-	7	-	8	-	ns
t_{WR}	Write Recovery Time	0	-	0	-	0	-	ns
t_{WHZ}	Write to Output in High Z	0	4	0	5	0	5	ns
t_{DW}	Data to Write Time Overlap	4	-	5	-	8	-	ns
t_{DH}	Data Hold from Write Time	0	-	0	-	0	-	ns
t_{OW}	Output Active from End of Write	3	-	3	-	5	-	ns

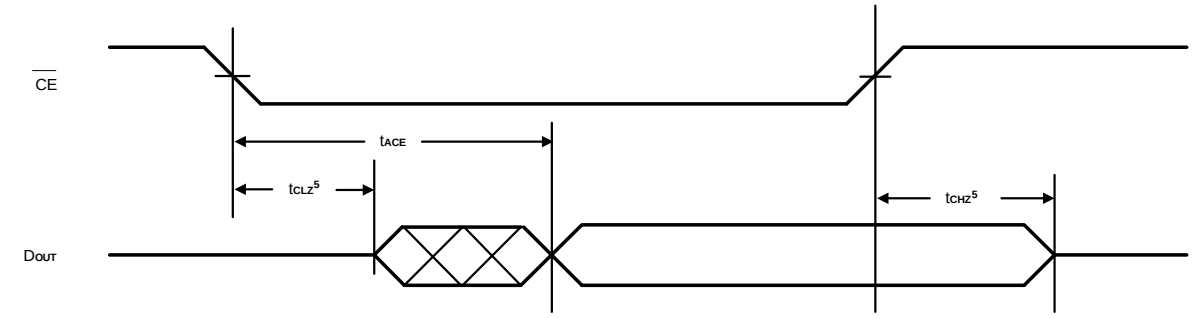
Notes: t_{CHZ1}, t_{CHZ2}, t_{OHZ}, and t_{WHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

Timing Waveforms

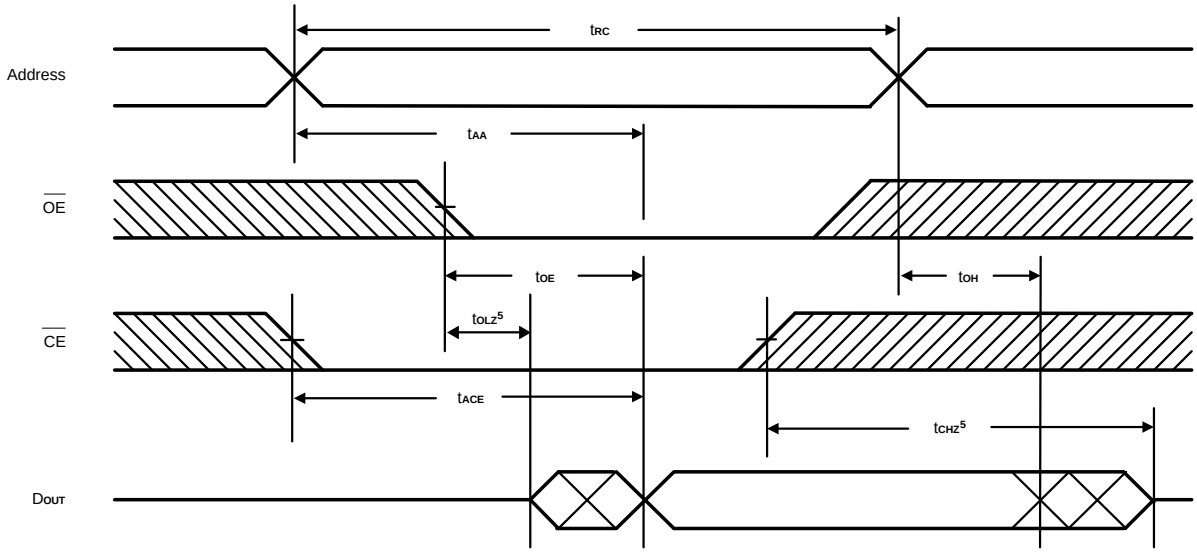
Read Cycle 1 (1, 2, 4)



Read Cycle 2 [1, 3, 4, 6]



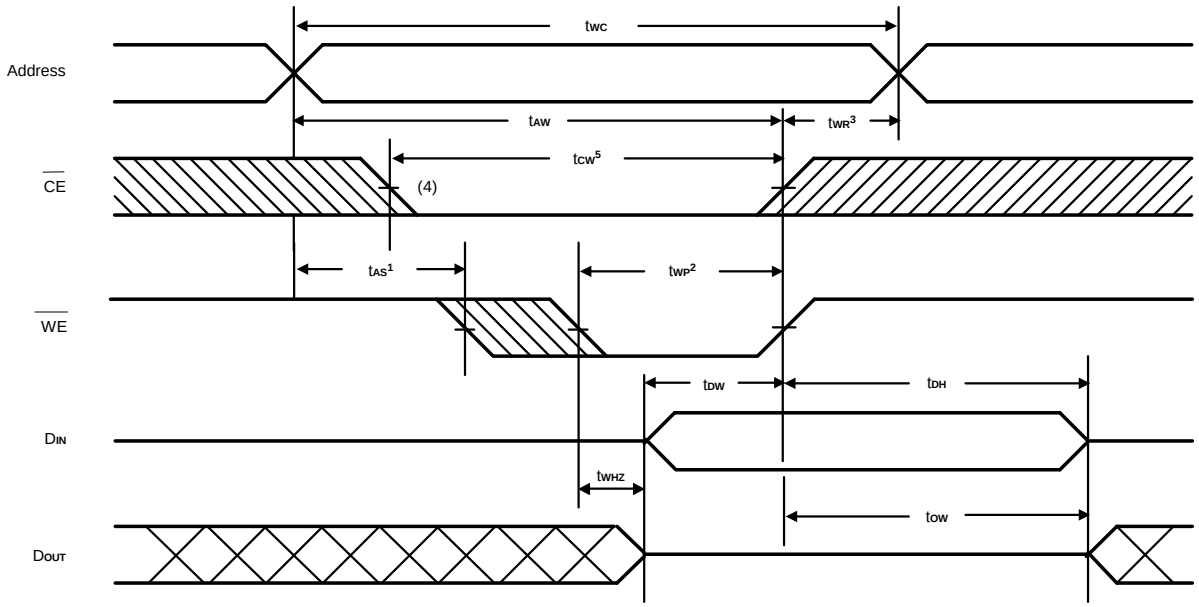
Read Cycle 3 [1]



Notes: 1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously enabled $\overline{CE}$ = V_I.
3. Address valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

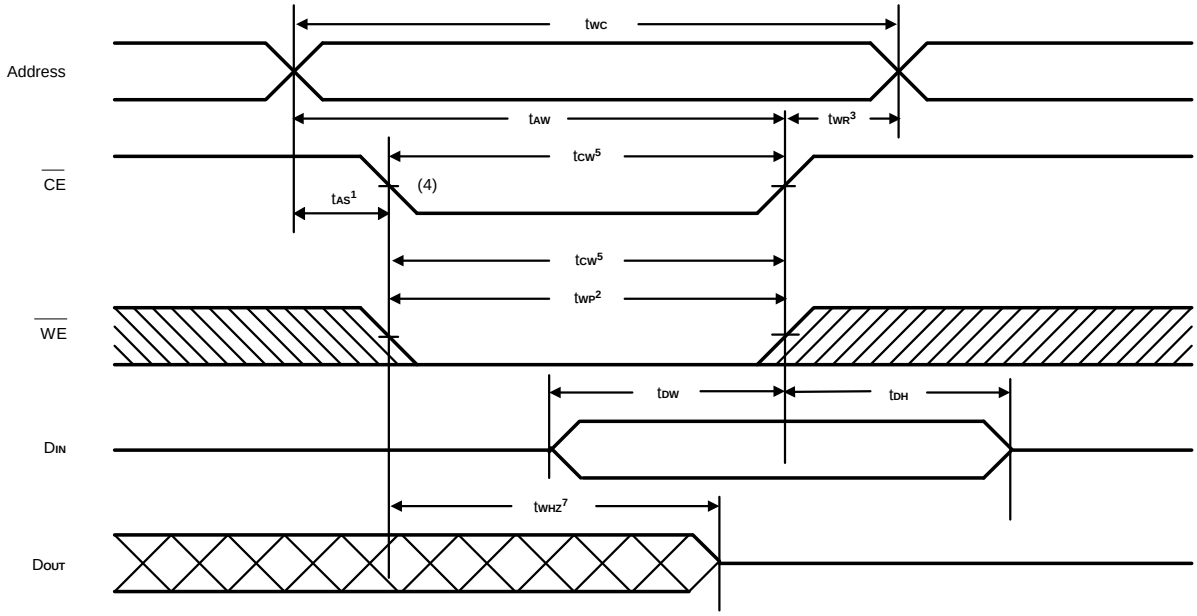
Timing Waveforms (continued)

Write Cycle 1[6]
(Write Enable Controlled)



Timing Waveforms (continued)

Write Cycle 2
(Chip Enable Controlled)



Notes: 1. t_{AS} is measured from the address valid to the beginning of Write.

2. A Write occurs during the overlap (t_{WP}) of a low $\overline{CE}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earliest of $\overline{CE}$ or $\overline{WE}$ going high to the end of the Write cycle.
4. If the $\overline{CE}$ low transition with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
5. t_{CW} is measured from the later of $\overline{CE}$ going low to the end of Write.
6. $\overline{OE}$ is continuously low. ($\overline{OE}$ = V_{IL})
7. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

AC Test Conditions

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Time	3 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Figures 1 and 2

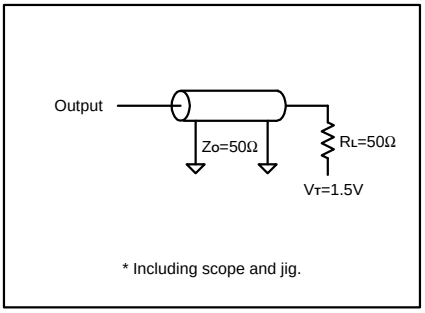


Figure 1. Output Load

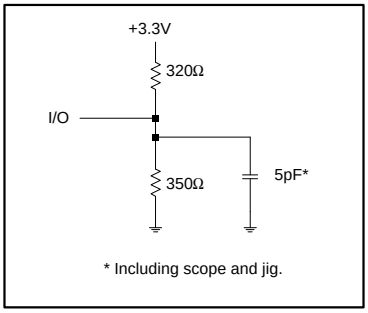
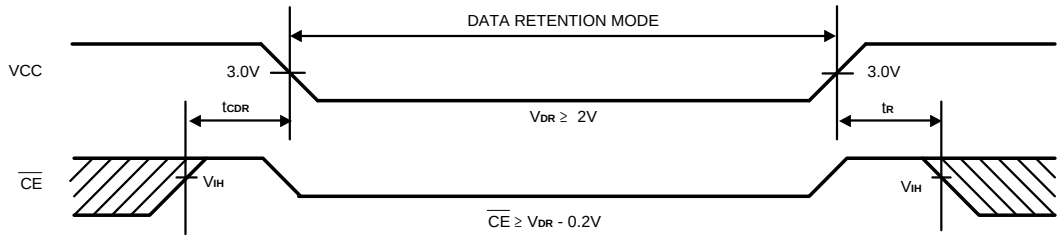


Figure 2. Output Load for t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{CHZ}, t_{WHZ}, and t_{OW}

Data Retention Characteristics (T_A = 0°C to 70°C)

Symbol	Parameter	Min.	Max.	Unit	Conditions
V_{DR1}	VCC for Data Retention	2	3.6	V	$\overline{CE} \geq$ VCC - 0.2V
I_{CCDR1}	Data Retention Current	-	3	mA	VCC = 2V $\overline{CE} \geq$ VCC - 0.2V $V_{IN} \geq$ VCC - 0.2V or $V_{IN} \leq$ 0.2V
t_{CDR}	Chip Disable to Data Retention Time	0	-	ns	See Retention Waveform
t_R	Operation Recovery Time	5	-	ms	

Low VCC Data Retention Waveform ($\overline{CE}$ Controlled)



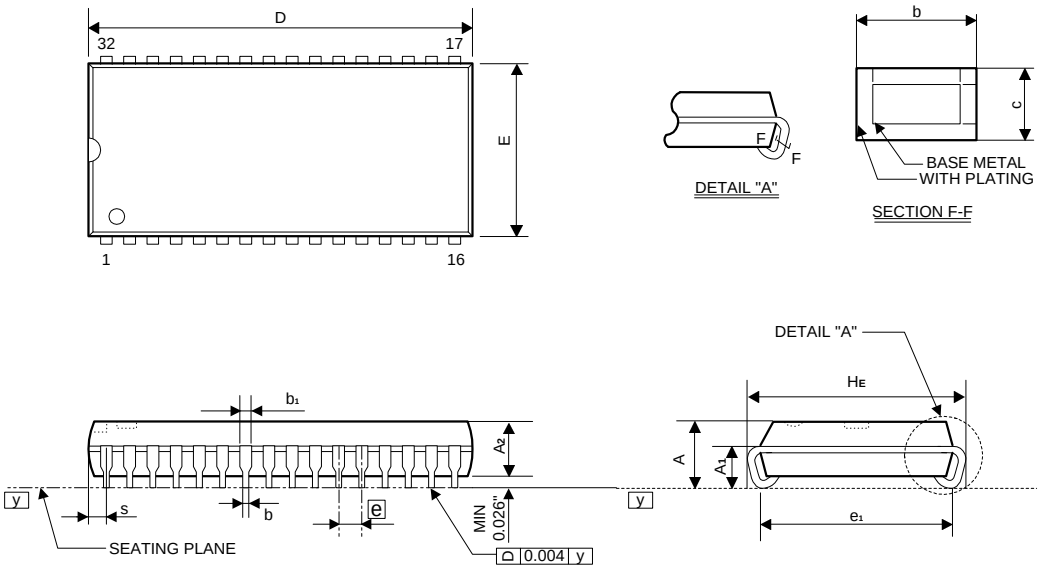
Ordering Information

Part No.	Access Time (ns)	Operating Current Max. (mA)	Standby Current Max. (mA)	Package
LP61L1008AS-8	8	160	5	32L SOJ (300 mil)
LP61L1008AS-10	10	155	5	32L SOJ (300 mil)
LP61L1008AS-12	12	150	5	32L SOJ (300 mil)

Package Information

SOJ 32 (300mil BODY) Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0128	0.132	0.140	3.25	3.35	3.56
A_1	0.052	-	-	2.08	-	-
A_2	0.095	0.100	0.105	2.41	2.54	2.67
b	0.016	0.018	0.020	0.41	0.46	0.51
b_1	0.026	0.028	0.032	0.66	0.71	0.81
c	0.006	0.008	0.012	0.15	0.20	0.30
D	0.820	0.825	0.830	20.83	20.96	21.08
H_E	0.330	0.335	0.340	8.39	8.51	8.63
E	0.295	0.300	0.305	7.49	7.62	7.75
e_1	0.260	0.267	0.274	6.61	6.78	6.96
e	-	0.050	-	-	1.27	-
s	-	-	0.048	-	-	1.22
y	-	-	0.004	-	-	0.10

Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E doesn't include resin fins.
3. Dimension e_1 is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.