PYRAMID SEMICONDUCTOR CORPORATION

P4C187/P4C187L

ULTRA HIGH SPEED 64K X 1 STATIC CMOS RAMS

FEATURES

- **Full CMOS, 6T Cell**
- **High Speed (Equal Access and Cycle Times)**
  - **– 10/12/15/20/25/35/45 ns (Commercial)**
  - **– 12/15/20/25/35 /45 ns (Industrial)**
  - **– 15/20/25/35/45/55/70/85 ns (Military)**
- **Low Power Operation**
- **Single 5V±10% Power Supply**
- **Data Retention with 2.0V Supply (P4C187L)**
- **Separate Data I/O**
- **Three-State Output**
- **TTL Compatible Output**
- **Fully TTL Compatible Inputs**
- **Standard Pinout (JEDEC Approved)**
  - **– 22-Pin 300 mil DIP**
  - **– 24-Pin 300 mil SOJ**
  - **– 22-Pin 290x490 mil LCC**
  - **– 28-Pin 350x550 mil LCC**

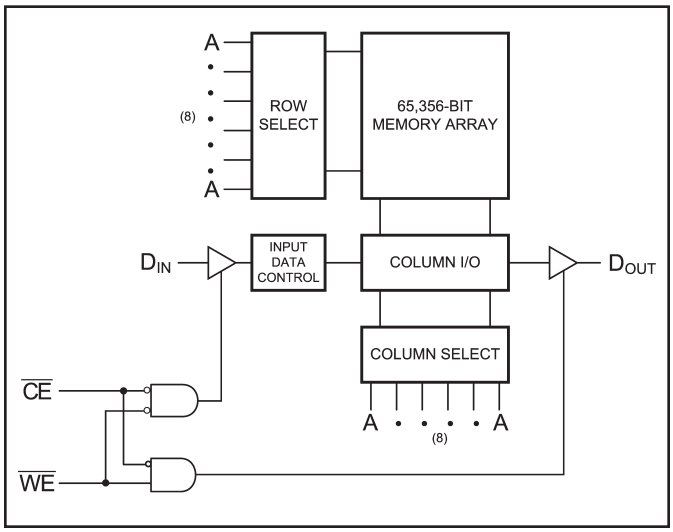
DESCRIPTION

The P4C187/P4C187L are 65, 536-bit ultra high speed static RAMs organized as 64K x 1. The CMOS memories require no clocks or refreshing and have equal access and cycle times. The RAMs operate from a single 5V ± 10% tolerance power supply. Data integrity is maintained for supply voltages down to 2.0V for the Low Power version, typically drawing 10µA.

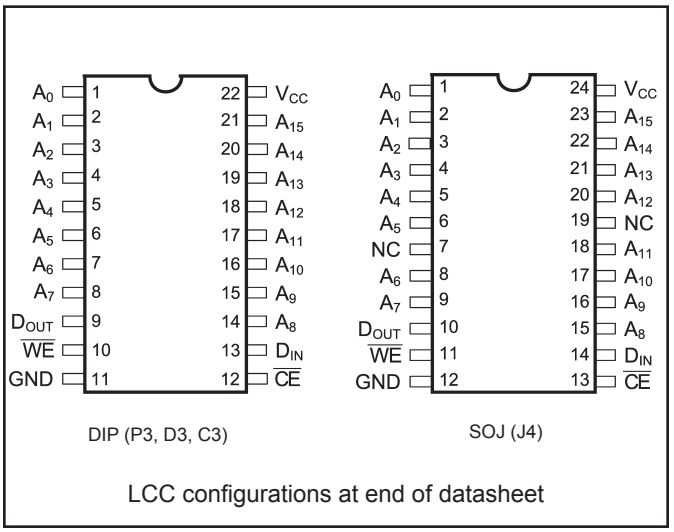
Access times as fast as 10 nanoseconds are available, greatly enhancing system speeds. CMOS reduces power consumption to a low 743mW active, 193/83mW standby for TTL/CMOS inputs and only 5.5 mW standby for the P4C187L.

The P4C187/P4C187L are available in 22-pin 300 mil DIP, 24-pin 300 mil SOJ, 22-pin and 28-pin LCC packages providing excellent board level densities.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



DIP (P3, D3, C3) SOJ (J4)

LCC configurations at end of datasheet

MAXIMUM RATINGS[1]

Sym	Parameter	Value	Unit
V_{CC}	Power Supply Pin with Respect to GND	-0.5 to +7	V
V_{TERM}	Terminal Voltage with Respect to GND (up to 7.0V)	-0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W

RECOMMENDED OPERATING CONDITIONS

Grade[2]	Ambient Temp	GND	V_{CC}
Commercial	0°C to 70°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%
Military	-55°C to +125°C	0V	5.0V ± 10%

CAPACITANCES[4]

(V_{CC} = 5.0V, T_A = 25°C, f = 1.0MHz)

Sym	Parameter	Conditions	Typ	Unit
C_{IN}	Input Capacitance	V_{IN}=0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	7	pF

DC ELECTRICAL CHARACTERISTICS

(Over Recommended Operating Temperature & Supply Voltage)[2]

Sym	Parameter	Test Conditions		P4C187 Min	P4C187 Max	P4C187L Min	P4C187L Max	Unit
V_{IH}	Input High Voltage			2.2	V_{CC} + 0.5	2.2	V_{CC} + 0.5	V
V_{IL}	Input Low Voltage			-0.5[3]	0.8	-0.5[3]	0.8	V
V_{HC}	CMOS Input High Voltage			V_{CC} - 0.2	V_{CC} + 0.5	V_{CC} - 0.2	V_{CC} + 0.5	V
V_{LC}	CMOS Input Low Voltage			-0.5[3]	0.2	-0.5[3]	0.2	V
V_{CD}	Input Clamp Diode Voltage	V_{CC} = Min, I_{IN} = 18 mA			-1.2		-1.2	V
V_{OL}	Output Low Voltage (TTL Load)	I_{OL} = +8 mA, V_{CC} = Min			0.4		0.4	V
V_{OH}	Output High Voltage (TTL Load)	I_{OH} = -4 mA, V_{CC} = Min		2.4		2.4		V
I_{LI}	Input Leakage Current	V_{CC} = Max, V_{IN} = GND to V_{CC}	MIL	-10	+10	-5	+5	µA
			IND/COM	-5	+5	N/A	N/A	
I_{LO}	Output Leakage Current	V_{CC} = Max, $\overline{CE}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL	-10	+10	-5	+5	µA
			IND/COM	-5	+5	N/A	N/A	
I_{SB}	Standby Power Supply Current (TTL Input Levels)	$\overline{CE}$ ≥ V_{IH}, V_{CC} = Max, f = Max, Outputs Open	MIL	—	40	—	40	mA
			IND/COM	—	35	—	N/A	
I_{SB1}	Standby Power Supply Current (CMOS Input Levels)	$\overline{CE}$ ≥ V_{HC}, V_{CC} = Max, f = 0, Outputs Open V_{IN} ≤ V_{LC} or V_{IN} ≥ V_{HC}	MIL	—	20	—	1.0	mA
			IND/COM	—	15	—	N/A	

N/A = Not applicable

Notes:

1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
2. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
3. Transient inputs with V_{IL} and I_{IL} not more negative than –3.0V and –100mA, respectively, are permissible for pulse widths up to 20ns.
4. This parameter is sampled and not 100% tested.

POWER DISSIPATION CHARACTERISTICS VS. SPEED

Sym	Parameter	Temperature Range	-10	-12	-15	-20	-25	-35	-45	-55	-70	-85	Unit
I_{CC}	Dynamic Operating Current*	Commercial	180	170	160	155	150	N/A	N/A	N/A	N/A	N/A	mA
		Industrial	N/A	180	170	160	155	150	N/A	N/A	N/A	N/A	mA
		Military	N/A	N/A	170	160	155	150	145	145	145	145	mA

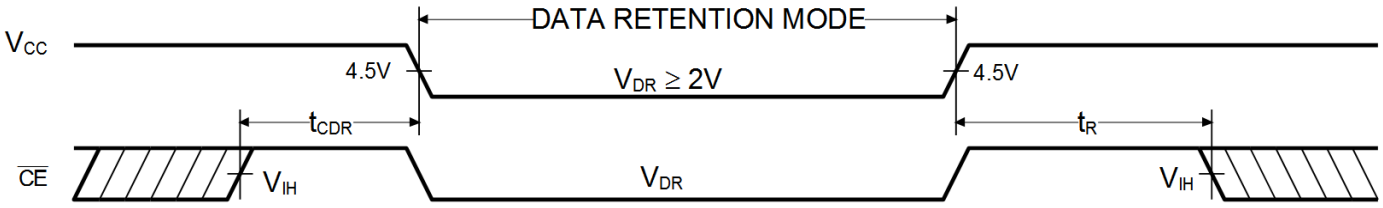
* V_{CC} = 5.5V. Tested with outputs open. f = Max. Switching inputs are 0V and 3V. $\overline{CE}$ = V_{IL}.

DATA RETENTION CHARACTERISTICS (P4C187L Military Temperature Only)

Sym	Parameter	Test Conditions	Min	Typ* V_{cc}=		Max V_{cc}=		Unit
				2.0V	3.0V	2.0V	3.0V	
V_{DR}	V_{CC} for Data Retention		2.0					V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{CC}$ -0.2V, $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq 0.2V$		10	15	600	900	µA
t_{CDR}	Chip Deselect to Data Retention Time		0					ns
t_R†	Operation Recovery Time		t_{RC}§					ns

* T_A = +25°C
§ t_{RC} = Read Cycle Time
† This Parameter is guaranteed but not tested

DATA RETENTION WAVEFORM

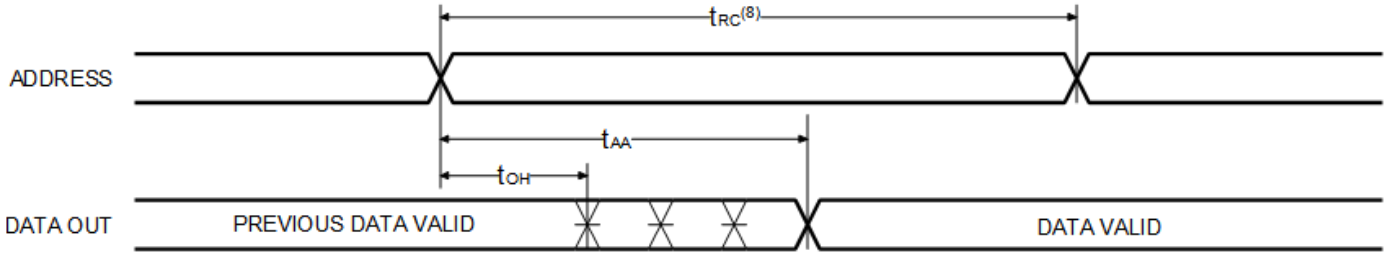


AC ELECTRICAL CHARACTERISTICS—READ CYCLE

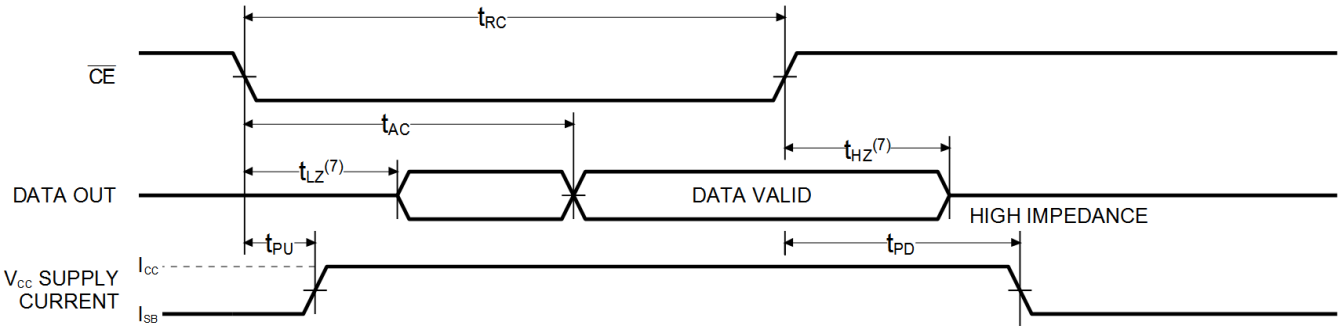
(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

Sym	Parameter	-10		-12		-15		-20		-25		-35		-45		-55		-70		-85		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	10		12		15		20		25		35		45		55		70		85		ns
t_{AA}	Address Access Time		10		12		15		20		25		35		45		55		70		85	ns
t_{AC}	Chip Enable Access Time		10		12		15		20		25		35		45		55		70		85	ns
t_{OH}	Output Hold from Address Change	2		2		2		2		2		2		2		2		2		2		ns
t_{LZ}	Chip Enable to Output in Low Z	2		2		2		2		2		2		2		2		2		2		ns
t_{HZ}	Chip Disable to Output in High Z		5		6		8		10		12		17		20		25		30		35	ns
t_{PU}	Chip Enable to Power Up Time	0		0		0		0		0		0		0		0		0		0		ns
t_{PD}	Chip Disable to Power Down		10		12		15		20		25		35		45		55		70		85	ns

TIMING WAVEFORM OF READ CYCLE NO. 1[5]



TIMING WAVEFORM OF READ CYCLE NO. 2[6]



Notes:

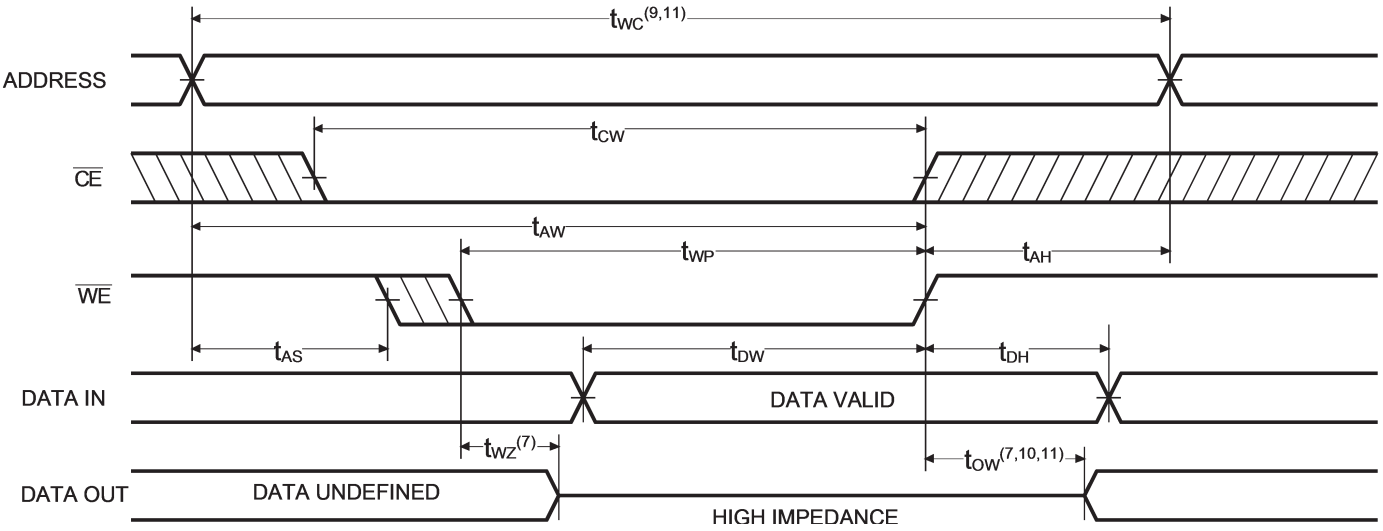
5. $\overline{CE}$ is LOW and $\overline{WE}$ is HIGH for READ cycle.
6. $\overline{WE}$ is HIGH, and address must be valid prior to or coincident with $\overline{CE}$ transition LOW.
7. Transition is measured ± 200 mV from steady state voltage prior to change with specified loading in Figure 1. This parameter is sampled and not 100% tested.
8. Read Cycle Time is measured from the last valid address to the first transitioning address.

AC CHARACTERISTICS—WRITE CYCLE

(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

Sym	Parameter	-10		-12		-15		-20		-25		-35		-45		-55		-70		-85		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	10		12		15		20		25		35		45		55		70		85		ns
t_{CW}	Chip Enable Time to End of Write	8		10		12		15		20		25		30		35		40		45		ns
t_{AW}	Address Valid to End of Wrtite	8		10		12		15		20		25		30		35		40		45		ns
t_{AS}	Address Set-up Time	0		0		0		0		0		0		0		0		0		0		ns
t_{WP}	Write Pulse Width	8		10		12		15		20		25		30		35		40		40		ns
t_{AH}	Address Hold Time from End of Write	0		0		0		0		0		0		0		0		0		0		ns
t_{DW}	Data Valid to End of Write	6		7		10		13		15		20		25		30		35		40		ns
t_{DH}	Data Hold Time	0		0		0		0		0		0		0		0		0		0		ns
t_{WZ}	Write Enable to Output in High Z		6		7		8		12		15		17		20		25		30		35	ns
t_{OW}	Output Active from End of Write	0		0		0		0		0		0		0		0		0		0		ns

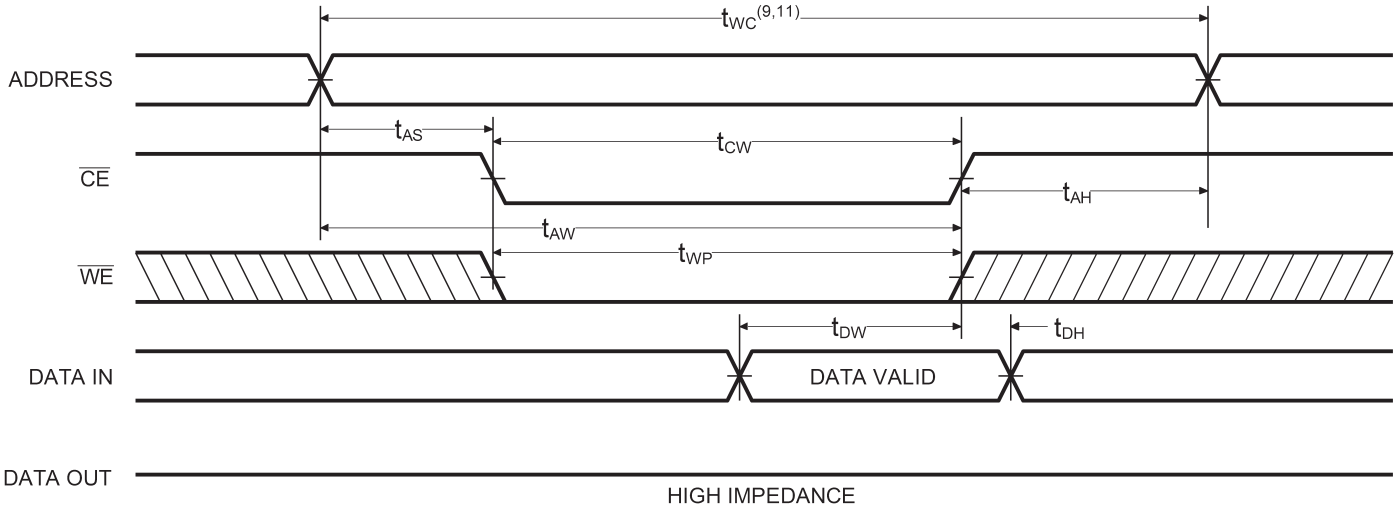
TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)[9]



Notes:

9. $\overline{CE}$ and $\overline{WE}$ must be LOW for WRITE cycle.
10. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high impedance state.
11. Write Cycle Time is measured from the last valid address to the first transition address.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CE}$ CONTROLLED)[10]



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Figures 1 and 2

TRUTH TABLE

Mode	$\overline{CE}$	$\overline{WE}$	Output	Power
Standby	H	X	High Z	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	High Z	Active

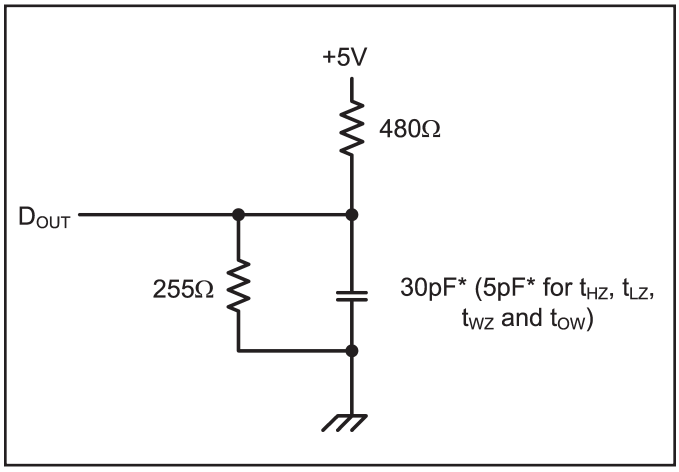


Figure 1. Output Load

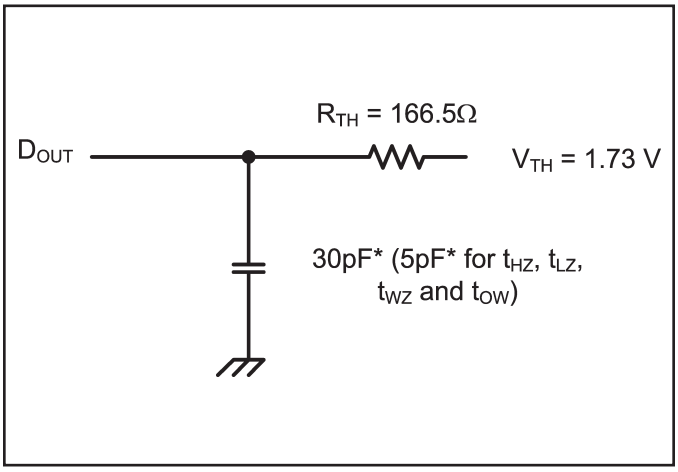
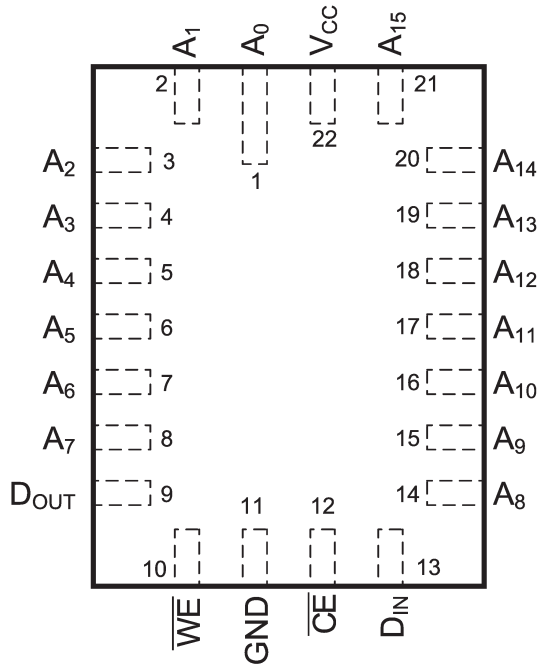


Figure 2. Thevenin Equivalent

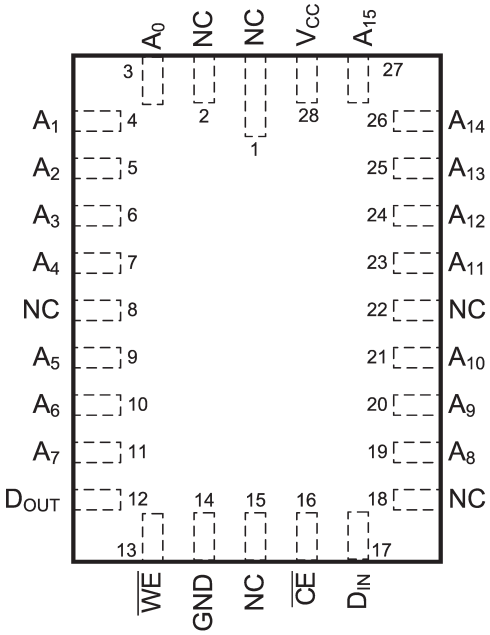
* including scope and test fixture.

Note:
Because of the ultra-high speed of the P4C187/L, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116Ω resistor must be used in series with D_{OUT} to match 166Ω (Thevenin Resistance).

LCC PIN CONFIGURATIONS

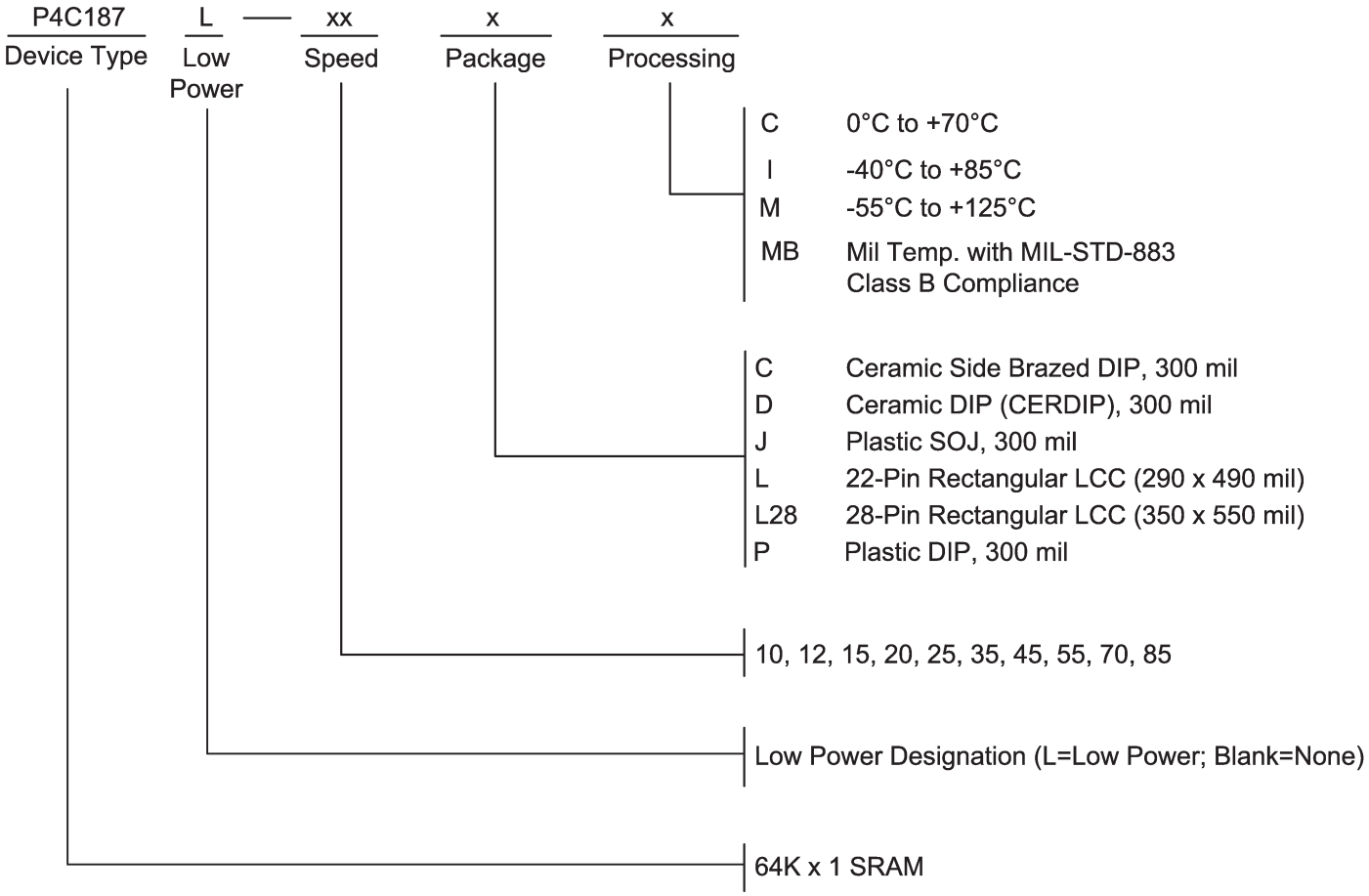


22-Pin LCC (L3)



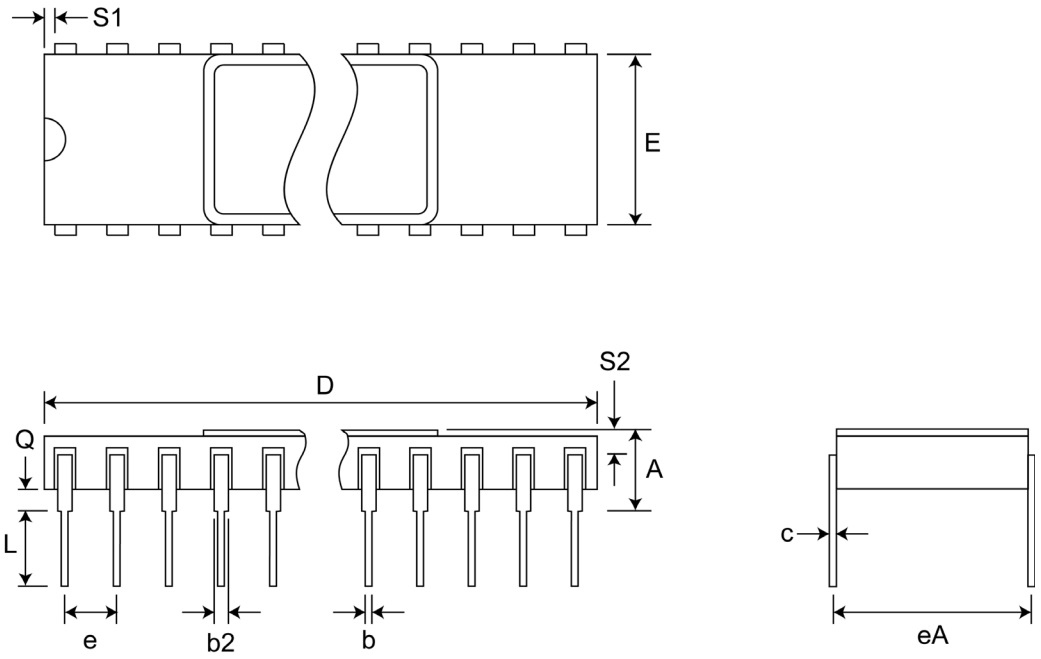
28-Pin LCC (L5)

ORDERING INFORMATION



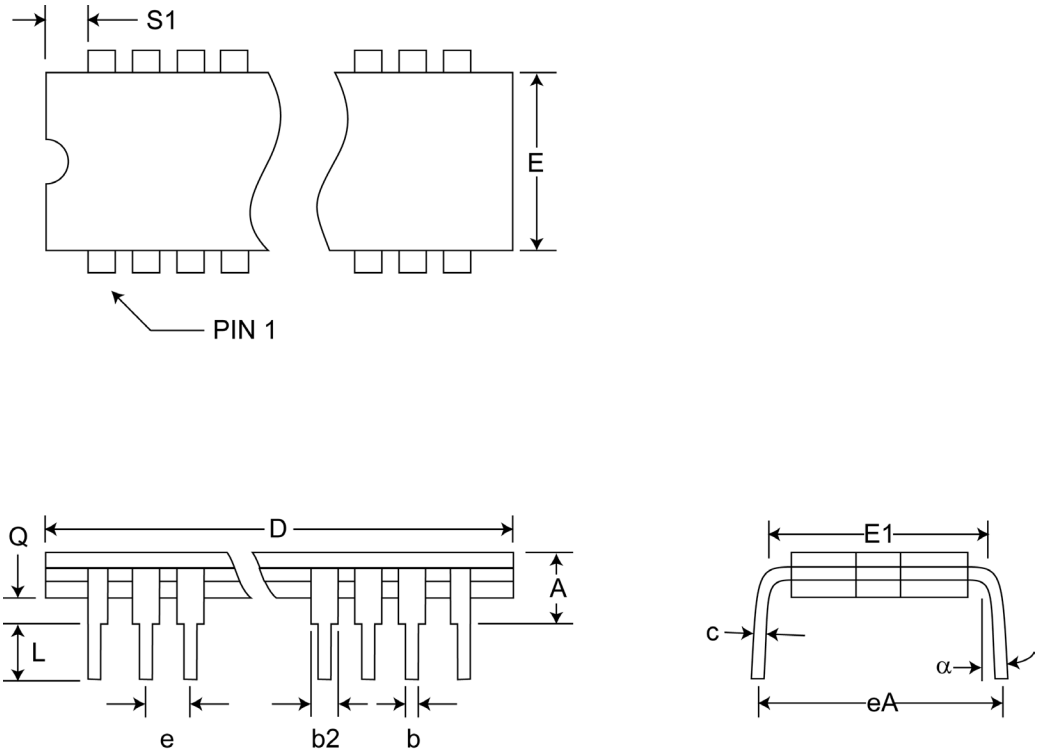
Pkg #	C3	
# Pins	22 (300 mil)	
Symbol	**Min**	**Max**
A	0.100	0.200
b	0.014	0.023
b2	0.030	0.060
C	0.008	0.015
D	1.050	1.260
E	0.260	0.310
eA	0.300 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.070
S1	0.005	-
S2	0.005	-

SIDEBRAZED DUAL IN-LINE PACKAGE



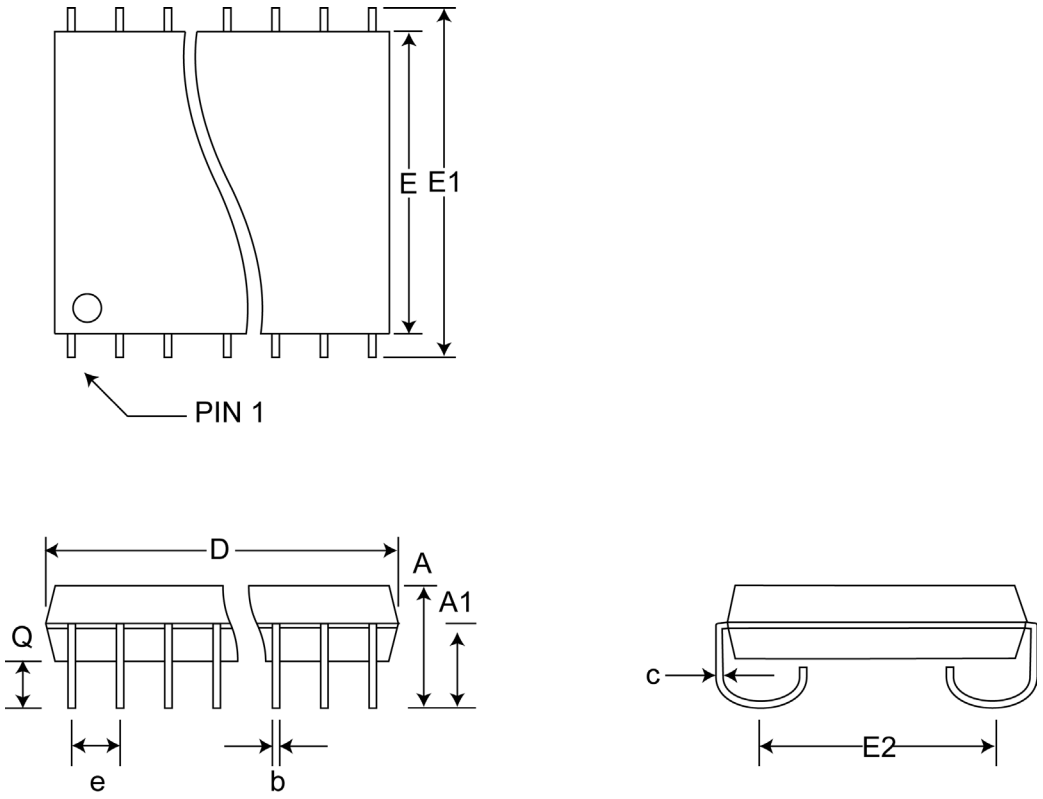
Pkg #	D3	
# Pins	22 (300 mil)	
Symbol	**Min**	**Max**
A	-	0.225
b	0.015	0.020
b2	0.045	0.065
C	0.009	0.012
D	1.060	1.110
E	0.290	0.320
eA	0.300 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.060
S1	0.005	-
α	0°	15°

CERDIP DUAL IN-LINE PACKAGE



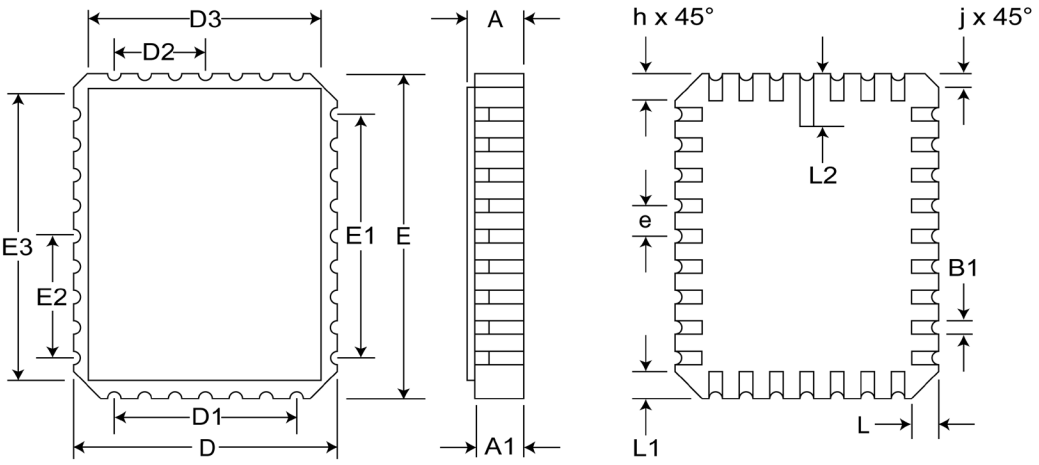
Pkg #	J4	
# Pins	24 (300 mil)	
Symbol	**Min**	**Max**
A	0.128	0.148
A1	0.082	-
b	0.016	0.020
C	0.007	0.010
D	0.620	0.630
e	0.050 BSC	
E	0.335 BSC	
E1	0.292	0.300
E2	0.267 BSC	
Q	0.025	-

SOJ SMALL OUTLINE IC PACKAGE



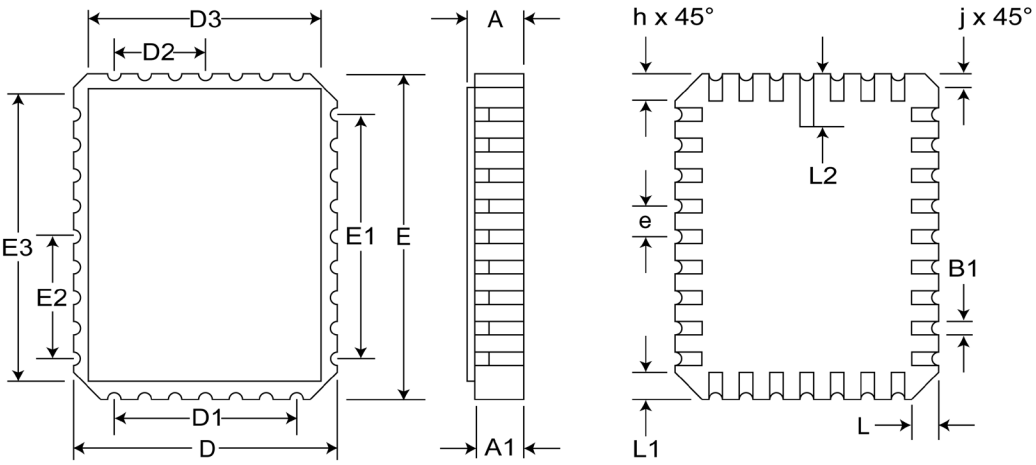
Pkg #	L3	
# Pins	22	
Symbol	**Min**	**Max**
A	0.060	0.080
A1	0.050	0.068
B1	0.022	0.028
D	0.284	0.296
D1	0.150 BSC	
D2	0.075 BSC	
D3	-	0.296
E	0.484	0.496
E1	0.300 BSC	
E2	0.150 BSC	
E3	-	0.496
e	0.050 BSC	
h	R = .012	
j	R = .012	
L	0.039	0.051
L1	0.039	0.051
L2	0.058	0.072
ND	4	
NE	7	

RECTANGULAR LEADLESS CHIP CARRIER



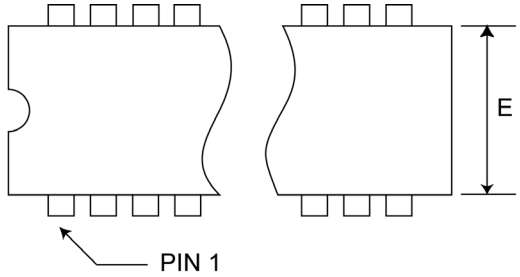
Pkg #	L5	
# Pins	28	
Symbol	**Min**	**Max**
A	0.060	0.075
A1	0.050	0.065
B1	0.022	0.028
D	0.342	0.358
D1	0.200 BSC	
D2	0.100 BSC	
D3	-	0.358
E	0.540	0.560
E1	0.400 BSC	
E2	0.200 BSC	
E3	-	0.558
e	0.050 BSC	
h	0.040 REF	
j	0.020 REF	
L	0.045	0.055
L1	0.045	0.055
L2	0.075	0.095
ND	5	
NE	9	

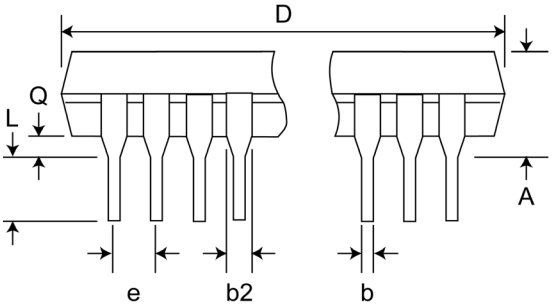
RECTANGULAR LEADLESS CHIP CARRIER

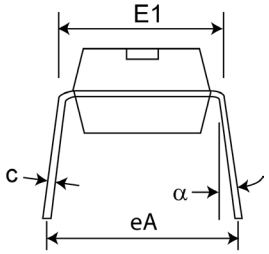


Pkg #	P3	
# Pins	22 (300 Mil)	
Symbol	**Min**	**Max**
A	-	0.210
A1	0.015	-
b	0.014	0.022
b2	0.045	0.070
C	0.008	0.014
D	1.145	1.165
E1	0.240	0.280
E	0.300	0.325
e	0.100 BSC	
eB	-	0.430
L	0.115	0.150
α	0°	15°

PLASTIC DUAL IN-LINE PACKAGE







REVISIONS

DOCUMENT NUMBER	SRAM 110
DOCUMENT TITLE	P4C116 / P4C116L ULTRA HIGH SPEED 2K X 8 STATIC CMOS RAMS

REV	ISSUE DATE	ORIGINATOR	DESCRIPTION OF CHANGE
OR	1997	DAB	New Data Sheet
A	Oct-2005	JDB	Changed logo to Pyramid
B	Apr-2007	JDB	Added 55, 70, and 85ns speeds
C	Oct-2011	JDB	Minor correction on LCC pinout; reformatting
D	Oct-2013	JDB	Minor correction to Write Cycle 1 timing diagram