# M5L 2708K, S; K-65, S-65

## 8192-BIT (1024-WORD BY 8-BIT) ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

### DESCRIPTION

This is a family of FAMOS (floating-gate avalanche-injection MOS) ultraviolet-light erasable and electrically reprogrammable 8192-bit (1024-word by 8-bit) EPROMs. They incorporate N-channel silicon-gate MOS technology, are designed for microcomputer system applications, and have direct TTL-compatibility for all inputs and outputs, without extra interface circuits.

### FEATURES

- Fast programming: 100s/8192 bits (typ)
- Access time:
  M5L 2708K, S: 450ns (max)
  M5L 270K-65, S-65: 650ns (max)
- Low power dissipation during programming
- No clocks required; the circuitry is entirely static
- Data inputs and outputs TTL-compatible during read and program modes
- Easy memory expansion by chip-select/write-enable ($\overline{CS}$/WE) input
- Typical power supply voltages: 12V, 5V, −5V
- For large volume production; pin compatible with the Mitsubishi M58730-XXXS mask-programmable ROM
- Interchangeable with Intel's 2708 in pin configuration and electrical characteristics

### APPLICATION

- Computers and peripheral equipment

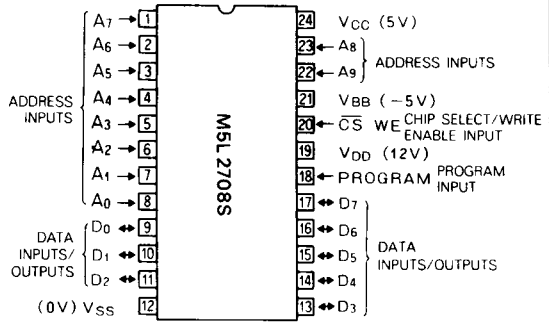
### FUNCTION

**Read**—Set the $\overline{CS}$/WE terminal to the read mode (0~5V). Low-level input to $\overline{CS}$/WE and address signals to the address input ($A_0 \sim A_9$) make the data contents of the designated address location available at the data inputs/outputs ($D_0 \sim D_7$). When the $\overline{CS}$/WE signal is high, data inputs/outputs ($D_0 \sim D_7$) are in a floating state.

**Write**—Set the $\overline{CS}$/WE terminal to the write mode (12V). A program pulse will effect the write operation for the data at each address loaded via data inputs/outputs ($D_0 \sim D_7$). For details refer to the description of the programming mode.

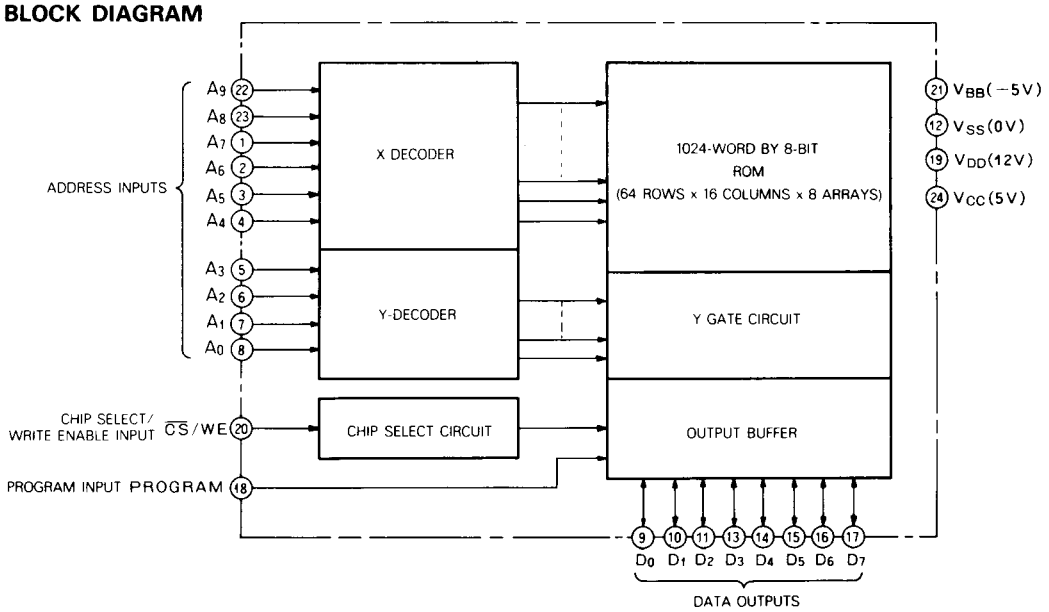
**Erase**—Erase is effected by exposure to ultraviolet light through the transparent window.

### PIN CONFIGURATION (TOP VIEW)




**Outline 24K10 (M5L 2708K)**
**24S10 (M5L 2708S)**

### BLOCK DIAGRAM



## 8192-BIT (1024-WORD BY 8-BIT) ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

### FUNCTIONAL OPERATIONS

#### Programming Procedure

These devices are in the '1' state (with high-level output) after erase, and go into the '0' state (with low-level output) after programming. All bits of the M5L 2708S, S-65 are initially in the '1' state, and must be programmed according to the following procedures.

The chip enters the program mode when 12V is supplied to the $\overline{CS}$/WE input (pin 20). Data to be programmed are presented, 8 bits in parallel, to the data inputs/outputs ($D_0 \sim D_7$) and the addresses are set up by the address inputs. After address and data set-up, one program pulse is applied to the program input (pin 18) for each address from 0 to 1023. This pass through all addresses, known as a program loop, must be repeated a number of times, N, which depends upon the width of the program pulse and must satisfy the condition $N \cdot t_{W(P)} \geqq 100ms$.

#### Erase Procedure

These devices can be erased by exposure to high-intensity short-wave ultraviolet light at a wavelength of 2537Å through the transparent lid provided. The required exposure is approximately $15Ws/cm^2$. If the energy of the lamp used is unknown, find the total time ($t_E$) required to erase all bits and use a short-wave ultraviolet-light exposure time of 3 to 5 times this value.

### HANDLING PRECAUTIONS FOR FAMOS DEVICES

In addition to general handling precautions for MOS devices, the following points apply to FAMOS devices.

1. High voltages are used when programming, and the conditions under which it is performed must be carefully controlled to prevent the application of excessively high voltages.
2. Before erasing, clean the surface of the transparent lid to remove completely oily impurities, which may impede irradiation and affect the erasing characteristics.
3 This ultraviolet-light erasable PROM is erasable by ultraviolet-light with wavelengths under 4000Å. For use involving long exposure to direct sunlight or to lamps radiating at these wavelengths, the transparent window should be covered with opaque tape.

# 8192-BIT (1024-WORD BY 8-BIT) ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{I1}$ | Input voltage, $V_{DD}$ and $\overline{CS}/WE$ write mode | With respect to $V_{BB}$ | −0.3 ~ 20 | V |
| $V_{I2}$ | Input voltage, $V_{CC}$, $V_{SS}$, address and data signal | | −0.3 ~ 15 | V |
| $V_{I3}$ | Input voltage, program mode | | −0.3 ~ 35 | V |
| $T_{opr}$ | Operating free-air temperature range | | 0 ~ 70 | ℃ |
| $T_{stg}$ | Storage temperature range | | −65 ~ 125 | ℃ |

## READ OPERATION

### Recommended Operating Conditions ($T_a$ = 0 ~ 70 ℃, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.75 | 5 | 5.25 | V |
| $V_{DD}$ | Supply voltage | 11.4 | 12 | 12.6 | V |
| $V_{BB}$ | Supply voltage | −4.75 | −5 | −5.25 | V |
| $V_{SS}$ | Supply voltage (GND) | | 0 | | V |
| $V_{IL}$ | Low-level input voltage | $V_{SS}$ | | 0.65 | V |
| $V_{IH}$ | High-level input voltage | 3 | | $V_{CC}$+1 | V |

### Electrical Characteristics

$T_a$ = 0 ~ 70 ℃, $V_{CC}$ = 5 V ±5%, $V_{DD}$ = 12 V ±5%, $V_{BB}$ = −5 V ±5%, $V_{SS}$ = 0 V, unless otherwise noted. Note 1)

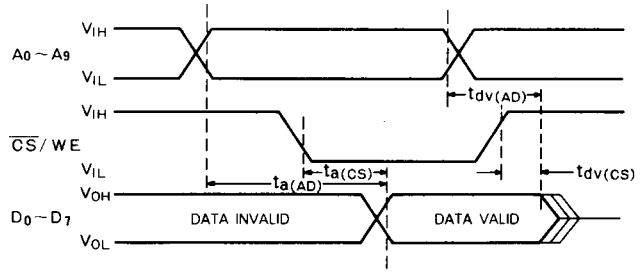
| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $I_{IL}$ | Low-level input current, address, chip select input | $V_I$ = 5.25 V | | | 10 | μA |
| $I_{OZ}$ | Off-state (high-impedance-state) output current | $V_O$ = 5.25 V, $V_{O(\overline{CS}\ WE)}$ = 5 V | | | 10 | μA |
| $I_{DD}$ | Supply current from $V_{DD}$ | Worst case, all inputs high, $V_{O(\overline{CS}\ WE)}$ = 5 V, $T_a$ = 0 ℃ | | 50 | 65 | mA |
| $I_{CC}$ | Supply current from $V_{CC}$ | | | 6 | 10 | mA |
| $I_{BB}$ | Supply current from $V_{BB}$ | | | 30 | 45 | mA |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 1.6 mA | | | 0.45 | V |
| $V_{OH1}$ | High-level output voltage | $I_{OH}$ = −100 μA | 3.7 | | | V |
| $V_{OH2}$ | High-level output voltage | $I_{OH}$ = −1 mA | 2.4 | | | V |
| $P_d$ | Power dissipation | $T_a$ = 70 ℃ | | | 800 | mW |
| $C_i$ | Input capacitance | $V_I$ = 0 V, f = 1 MHz | | 4 | 6 | pF |
| $C_o$ | Output capacitance | | | 8 | 12 | pF |

Note 1 : Typical values are at $T_a$ = 25 ℃ and nominal supply voltage.

### Switching Characteristics ($T_a$ = 0 ~ 70 ℃, $V_{CC}$ = 5 V ±5%, $V_{DD}$ = 12 V ±5%, $V_{BB}$ = −5 V ±5%, $V_{SS}$ = 0 V, unless otherwise noted)

| Symbol | Parameter | | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $t_{a(AD)}$ | Address access time | M5L 2708K, S | | | 280 | 450 | ns |
| | | M5L 2708K-65, S-65 | | | | 650 | ns |
| $t_{a(CS)}$ | Chip select access time | | | | 60 | 120 | ns |
| $t_{dv(CSLH)}$ | Data valid time with respect to chip select low-to-high | | | 0 | | 120 | ns |
| $t_{dv(AD)}$ | Data valid time with respect to address | | | 0 | | | ns |

### Timing Diagram




The center line indicates a floating (high-impedance) state.

**Test Conditions for Switching Characteristics**

Input voltage : $V_{IL}$ = 0.65 V, $V_{IH}$ = 3 V
Reference voltage at timing measurement : Input 0.8 ~ 2.8 V
output 0.8 ~ 2.4 V

## 8192-BIT (1024-WORD BY 8-BIT) ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

### PROGRAM OPERATION

**Recommended Operating Conditions** ($T_a$=25℃, $V_{CC}$=5V±5%, $V_{DD}$=12V±5%, $V_{BB}$=−5V±5%, $V_{SS}$=0V, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{IL1(P)}$ | Low-level input voltage, except program input | $V_{SS}$ | | 0.65 | V |
| $V_{IH1(P)}$ | High-level input voltage, address, data input | 3 | | $V_{CC}$+1 | V |
| $V_{IH2(P)}$ | High-level input voltage, $\overline{CS}$/WE | 11.4 | | 12.6 | V |
| $V_{IH3(P)}$ | High-level input voltage, program mode [2] | 25 | | 27 | V |
| $V_{IL2(P)}$ | Low-level input voltage, program mode [3] | $V_{SS}$ | | 1 | V |

Note 2 : With respect to $V_{SS}$
3 : Where $V_{IH3(P)} - V_{IL2(P)}$ = 25V (min)

**Electrical Characteristics** ($T_a$=25℃, $V_{CC}$=5V±5%, $V_{DD}$=12V±5%, $V_{BB}$=−5V±5%, $V_{SS}$=0V, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $I_{IL1(P)}$ | Low-level input current, address, chip select input | $V_I$ = 5.25V | | | 10 | μA |
| $I_{IL2(P)}$ | Low-level input current, program input | | | | 3 | mA |
| $I_{IH1(P)}$ | High-level current, program input | | | | 20 | mA |
| $I_{DD}$ | $V_{DD}$ supply current | Worst case, | | 50 | 65 | mA |
| $I_{CC}$ | $V_{CC}$ supply current | all inputs high [4] | | 6 | 10 | mA |
| $I_{BB}$ | $V_{BB}$ supply current | $\overline{CS}$/WE=5V, $T_a$=0℃ | | 30 | 45 | mA |

Note 4 : Typical values are at $T_a$=25℃ and nominal supply voltage.

**Timing Requirements** ($T_a$=25℃, $V_{CC}$=5V±5%, $V_{DD}$=12V±5%, $V_{BB}$=−5V±5%, $V_{SS}$=0V, unless otherwise noted)

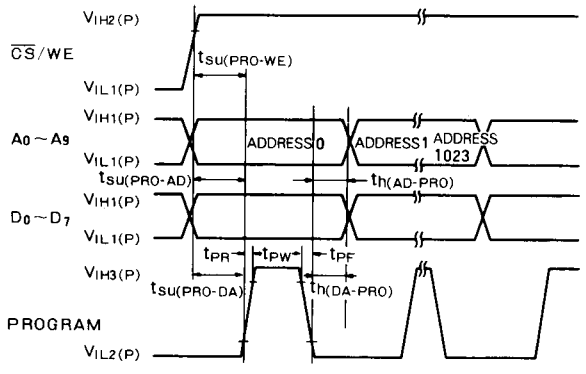
| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $t_{su(PRO-AD)}$ | Program setup time with respect to address | | 10 | | | μs |
| $t_{su(PRO-WE)}$ | Program setup time with respect to WE low-to-high | | 10 | | | μs |
| $t_{su(PRO-DA)}$ | Program setup time with respect to data | | 10 | | | μs |
| $t_{h(AD-PRO)}$ | Address hold time with respect to program | | 1 | | | μs |
| $t_{h(WE-PRO)}$ | WE hold time with respect to program | | 0.5 | | | μs |
| $t_{h(DA-PRO)}$ | Data hold time with respect to program | | 1 | | | μs |
| $t_{w(P)}$ | Program pulse width | | 0.1 | | 1 | ms |
| $t_{r(P)}$ | Program rise time | | 0.5 | | 2 | μs |
| $t_{f(P)}$ | Program fall time | | 0.5 | | 2 | μs |

**Switching Characteristics** ($T_a$=25℃, $V_{CC}$=5V±5%, $V_{DD}$=12V±5%, $V_{BB}$=−5V±5%, $V_{SS}$=0V, unless otherwise noted)

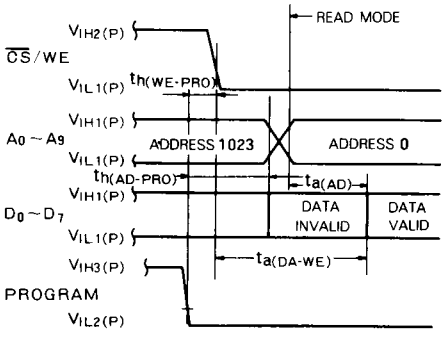
| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $t_{a(DA-WE)}$ | Access time with respect to WE high-to-low | | | | 10 | μs |
| $t_{dv(DA-\overline{CS})}$ | Data valid time with respect to $\overline{CS}$ low-to-high | | 0 | | 120 | ns |

### Timing Diagram

**Program Mode**




**From Program Mode to Read Mode**



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