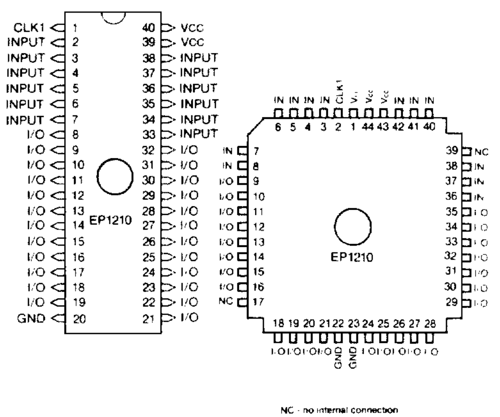
ALTERA EP1210 ERASABLE PROGRAMMABLE LOGIC DEVICE

FEATURES

- High Density (over 1200 gates) replacement for TTL and 74HC.
- Advanced CHMOS EPROM technology allows for erasability and reprogrammability.
- Low power: 15 mW typical standby power dissipation.
- Programmable Macrocell & I/O Architecture: up to 36 inputs or 24 outputs, 28 Macrocells including 4 buried state registers.
- Programmable latch feature allows latching of all inputs.
- Programmable clock system for input latches and output registers.
- Product term sharing and local bus architecture for optimized array performance.
- 100% generically testable — provides 100% programming yield.
- Programmable "Security Bit" allows total protection of proprietary designs.
- Advanced software support featuring Schematic Capture, Interactive Netlist, State Machine and Boolean Equation design entry methods.
- Package options include 40 pin DIP and 44 pin J-Leaded Chip Carrier.

CONNECTION DIAGRAM



(a) 40 Pin DIP (b) 44 Pin JLCC

GENERAL DESCRIPTION

The Altera EP1210 is an LSI logic circuit that can be programmed to provide logic replacement for conventional SSI and MSI logic circuits.

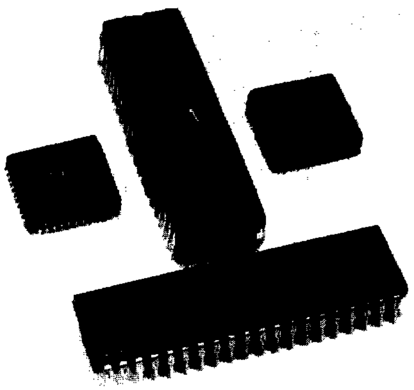
The EP1210 contains CMOS EPROM (floating-gate) elements that control the logical operation of the device. The device can typically provide equivalent performance to 1200 gates of SSI and MSI logic. The EPROM technology enables the logic designer to rapidly program the device and make design changes after erasing for just a few minutes. The same technology also permits 100% factory testing of all elements within the device.

The CMOS technology reduces power consumption to less than 10% of equivalent bipolar devices without sacrificing speed performance.

To implement general purpose logic the EP1210 contains the familiar sum-of-product PLA structure with a programmable AND and fixed OR array. The design uses a range of OR gate widths to accommodate logical functions without the overhead of unnecessary product-terms or the speed penalties of programmable OR structures.

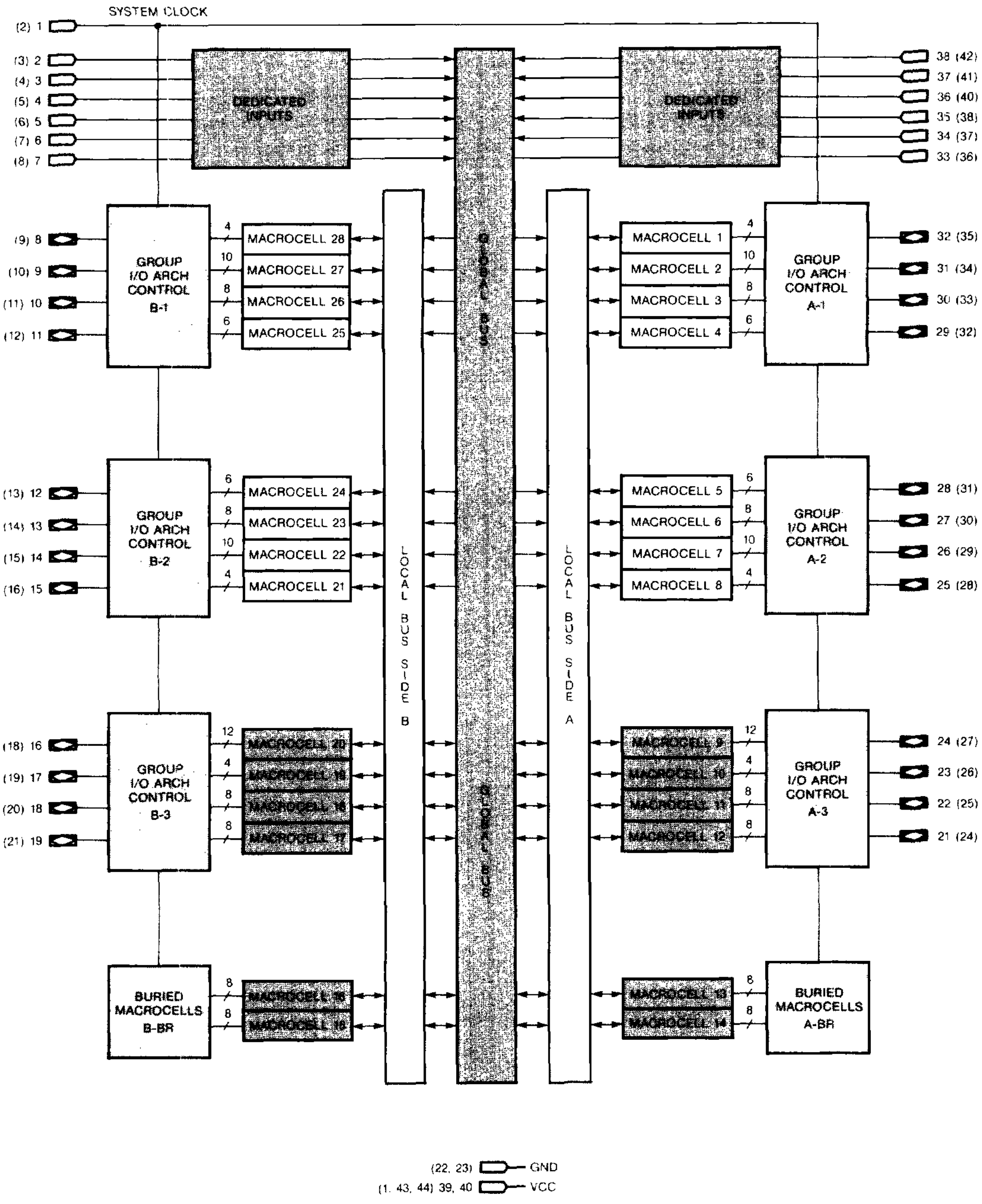
A segmented PLA design that provides local and global connectivity also optimizes the performance of the EP1210.

The EP1210 contains innovative architectural features that provide significant I/O flexibility and maximize performance within a conventional dual-in-line package or a J-leaded chip carrier package for increased footprint efficiency.



REV. 3.0

EP1210 BLOCK DIAGRAM



PIN NUMBERS IN ( ) PERTAIN TO 44 PIN JLCC.

FUNCTIONAL DESCRIPTION

The EP1210 is an LSI erasable programmable logic device (EPLD) which uses EPROM technology to configure connections within a programmable logic array. The device has a programmable I/O architecture that provides options to change inputs, outputs and logical function of the device.

The internal architecture is based on 28 Macrocells each of which contains a PLA and a programmable I/O block that can be programmed to create many different logic structures. This powerful I/O architecture can be configured to support both active-high, active-low, 3-state, open-drain and bi-directional data ports or act as an input, all on a 4-bit wide basis.

All inputs to the circuit may be latched, including the 12 dedicated input pins.

The Macrocells share a common programmable clock system that controls clocking of all registers and input latches. The device contains 8 modes of clock operation that allow logic transitions to take place on either rising or falling edges of the clock signals.

The primary logic array of the EP1210 is segmented into two symmetrical halves that communicate via global bus signals. The main arrays contain some 15104 programmable elements representing 236 product terms each containing 64 input signals.

Macrocells in each half of the circuit are grouped together for architecture programming. These banks of four Macrocells can be further programmed on an individual Macrocell basis to generate active high or active low outputs of the logic function from the PLA.

The circuit further contains four Macrocells whose outputs are only fed back into the array to create buried-state functions. The feedback path may be either the registered or combinatorial result of the PLA output. The use of buried state Macrocells provides maximum equivalent logic density without demanding higher pin-count packages which consume valuable board space.

I/O ARCHITECTURE

The Input/Output architecture of the EP1210 Macrocells can be programmed using both static and dynamic controls. The static controls remain fixed after the device is programmed whereas the dynamic controls may change state as a result of the signals applied to the device.

The static controls set the inversion logic, register by-pass and input feedback multiplexers. In the latter two cases these controls operate on four Macrocells as a bank. The buried-state registers have simpler controls which determine if the feedback is to be registered or combinatorial.

The dynamic controls consist of a programmable input latch-enable, as well as register clear and output-enable product terms. The latch-enable function is common throughout the EP1210 and is programmed by the clock control block but may also be driven by input signals applied to pin 1 (see clock modes in Table 1). The register clear and output-enable controls are logically controlled by single product terms (the logic AND of programmed variables in the array). These terms have control over banks of four Macrocells.

The output-enable control may be used to generate architecture types that include bi-directional, 3-state, open-drain or input only structures.

OUTPUT/FEEDBACK SELECTION

The EP1210 Input/Output Architecture allows each group of Macrocells to be programmed for combinatorial or registered operation, with individual control over output polarity. In addition, the designer may configure the feedback path for combinatorial, registered, input (pin), and latched input feedback. All Macrocell groups have Asynchronous Clear control from a dedicated product term. When the product term is asserted to a logical "1", the registers within the respective Macrocell group will immediately be loaded with a logical "0" independently of the clock. On power up, the EP1210 performs the Clear function automatically.

Figure 2 shows the basic output configurations for the EP1210. In a combinatorial mode, the output is controlled via the group dedicated Output Enable product term. The Invert Select EPROM bit controls output polarity. The Feedback Select Multiplexer enables registered feedback, pin or latched pin feedback, or no feedback.

In a registered mode, 4 to 16 product terms are ORed together and made available to the D-type flipflop. The Output Enable product term allows registered or no output. The Invert Select EPROM bit determines output polarity. The Feedback Select Multiplexer can be configured for registered feedback, pin or latched pin feedback, or no feedback.

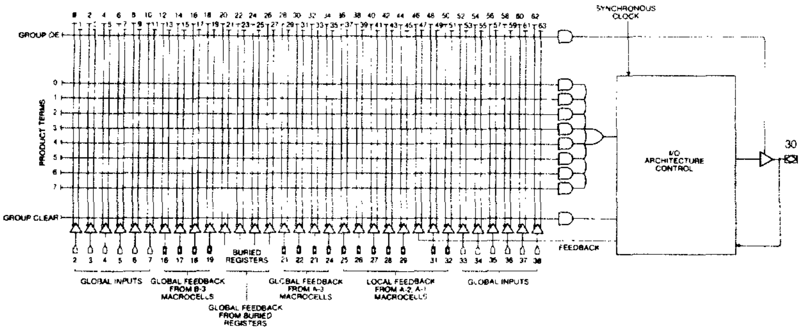
Any I/O group can be configured as a dedicated input group by selecting no output and pin feedback.

In the erased state, the EP1210 I/O is configured for active low combinatorial output and latched pin feedback.

SHARED PRODUCT TERMS

Macrocells 9, 10, 11, 12, 17, 18, 19 and 20 have the facility to share a total of 16 additional product terms. The sharing takes place between pairs of adjacent macrocells. This capability enables, for example, Macrocells 9 and 10 to expand to 16 and 8 effective product terms respectively and for Macrocells 11 and 12 both to expand to 12 effective product terms. This facility is primarily of use in state machine and counter applications where common product-terms are frequently required among output functions.

FIG. 1 LOGIC ARRAY MACROCELL (FOR OUTPUT TAKEN FROM "A" HALF ONLY)

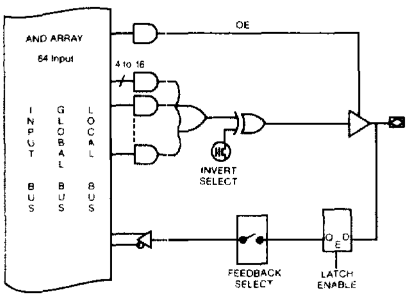


Note: [I/O pin symbol] = I/O Pin in which Logic Array input is from feedback path pin numbers pertain to 40 pin DIP.

FIG. 2 MACROCELL CONFIGURATIONS

A. I/O MACROCELLS

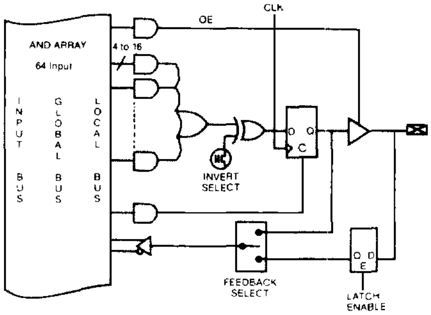
COMBINATORIAL



I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
Combinatorial/High	Pin, Latched Pin None
Combinatorial/Low	Pin, Latched Pin None
None	Pin, Latched Pin

REGISTERED

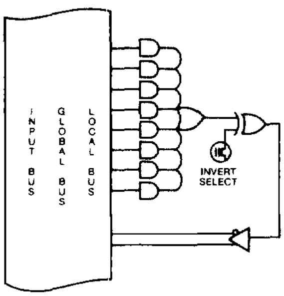


I/O SELECTION

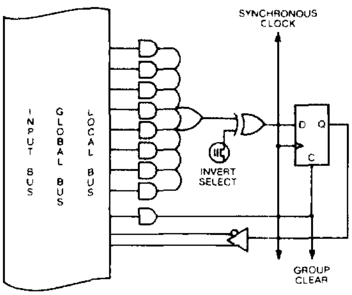
OUTPUT/POLARITY	FEEDBACK
Registered/High	Registered, Pin, Latched Pin, None
Registered/Low	Registered, Pin, Latched Pin, None
None	Registered, Pin, Latched Pin

B. BURIED MACROCELLS

NO OUTPUT, COMBINATORIAL FEEDBACK



NO OUTPUT, REGISTERED FEEDBACK



BUS STRUCTURE

The two identical halves of the EP1210 communicate via a series of buses. The local bus structure that is used for communication within each half of the chip contains 16 conductors that carry the TRUE and COMPLEMENT of 8 local Macrocells.

The global bus is comprised of 48 conductors that span the entire chip which carry the TRUE and COMPLEMENT of primary inputs (pins 2 through 7 and 33 through 38), signals from 4 Buried Registers, as well as the global outputs of 8 Macrocells in groups A-3 and B-3.

MACRO — BUS INTERFACE

The Macrocells within an EP1210 are interconnected to other Macrocells and inputs to the device via three internal data buses.

The product-terms span the entire bus structure that is adjacent to their Macrocell so that they may produce a logical AND of any of the variables (or their complements) that are present on the buses.

Macrocells all have the ability to return data to the local or global bus. Feedback data may originate from the output of the Macrocell or from the I/O pin. Feedback to the global bus communicates throughout the part. Macrocells that feedback to the local bus communicate to only half the EP1210. Connections to and from the signal buses are made with EPROM

FIG. 3 MACROCELL BUS STRUCTURE

At each intersecting point in the logic array there exists an EPROM-type programmable connection. Initially, all connections are complete. This means that both the true and complement of all inputs are connected to each product-term. Connections are opened during the programming process. Therefore any product term can be connected to the true or complement of any input. When both the true and complement connections of any input are left intact, a logical false results on the output of the AND gate. If both the true and complement connections of any input are programmed open, then a logical "don't care" results for that input. If all inputs for a product term are programmed open, then a logical true results on the output of the AND gate.

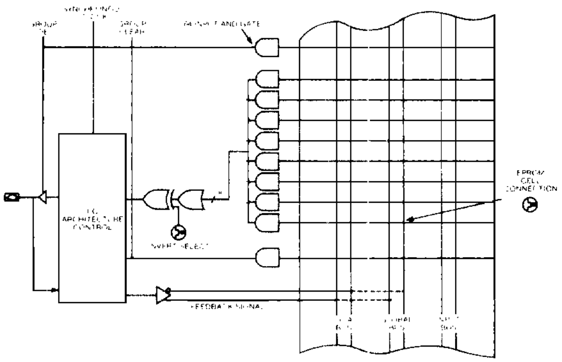
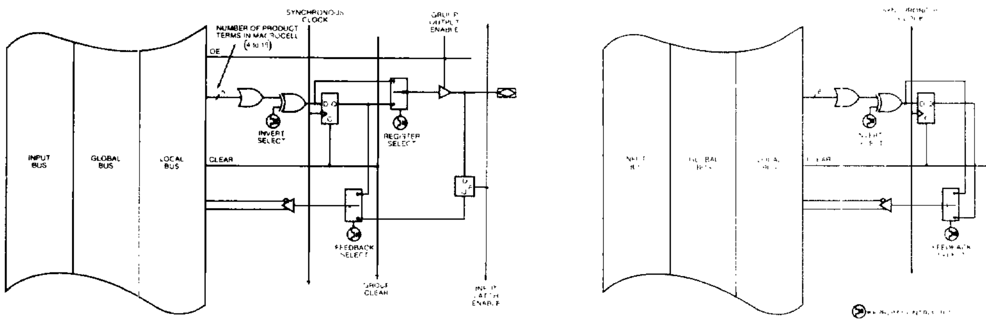


FIG. 4

A. I/O MACROCELL **B. BURIED MACROCELL**



switches that provide the reprogrammable logic capability of the circuit.

Macrocells in groups A-3 and B-3 and the buried registers all have global bus connections while Macrocells in groups A-1, A-2, and B-1, B-2 have local bus connections. Figure 3 illustrates the local and global bus connections. Advanced features of the ALTERA development system will, if desired, automatically select an appropriate Macrocell to meet both the logic requirements and the connection to an appropriate signal bus to achieve the interconnection to other Macrocells.

CLOCK MODE CONTROL

The EP1210 contains two internal clock data paths that drive the input latches (transparent 7475 type) and the output registers. These clocks may be programmed into one of eight operating modes. Input latches may be enabled on either the high or low level of CLK1 (pin1). Once latched, the input signal keeps its value until the next transition of the chosen clock. Output registers can be programmed to be positive or negative edge-triggered with respect to CLK1 or CLK2. Table 1 shows the operation of each programming mode.

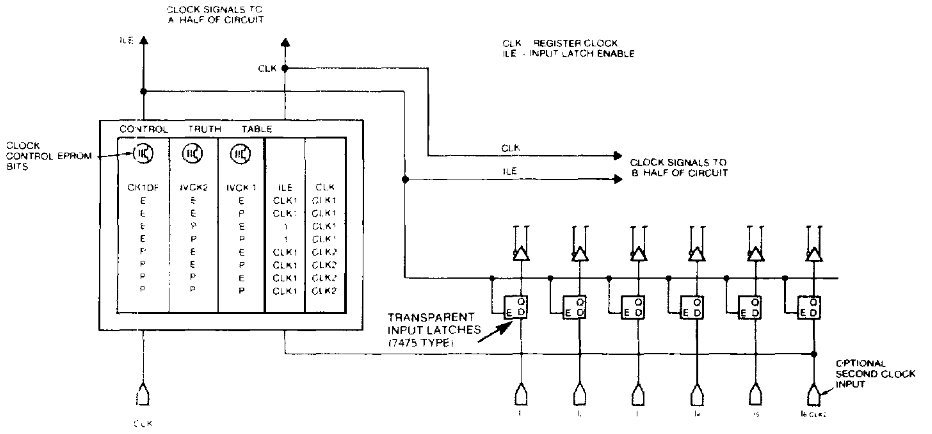
In the erased state, the EP1210 clocking operation is set for mode 0. This means inputs are latched on a high level of CLK1. The high to low transition of CLK1 causes the input latches to become disabled, allowing input values to propagate into the logic array without being latched. In addition, CLK1 drives the output registers which are negative edge-triggered.

Care is required when using any of the two-clock modes to ensure that timing hazards are not created.

TABLE 1 CLOCK PROGRAMMING

PROGRAMMED MODE	INPUT SIGNALS ARE PASSED (a) AND DATA IS LATCHED (b) WHEN:	OUTPUT REGISTERS CHANGE STATE WHEN:	CLOCK CONFIGURATION
0	CLK1 (PIN1) a b	CLK1 (PIN1)	1 CLOCK
1	CLK1 (PIN1) a b	CLK1 (PIN1)	1 CLOCK
2	INPUTS NOT LATCHED	CLK1 (PIN1)	1 CLOCK
3	INPUTS NOT LATCHED	CLK1 (PIN1)	1 CLOCK
4	CLK1 (PIN1) a b	CLK2 (PIN38)	2 CLOCKS
5	CLK1 (PIN1) a b	CLK2 (PIN38)	2 CLOCKS
6	CLK1 (PIN1) a b	CLK2 (PIN38)	2 CLOCKS
7	CLK1 (PIN1) a b	CLK2 (PIN38)	2 CLOCKS

FIG. 5 PROGRAMMABLE CLOCK CONTROL SYSTEM



ABSOLUTE MAXIMUM RATINGS

COMMERCIAL, INDUSTRIAL, MILITARY

Note: See Design Recommendations

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply voltage	With respect to GND note (3)	-2.0	7.0	V
V_{PP}	Programming supply voltage		-2.0	13.5	V
V_I	DC INPUT voltage		-2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		-150	+150	mA
I_{OUT}	DC OUTPUT current, per pin		-25	+25	mA
P_D	Power dissipation			380	mW
T_{STG}	Storage temperature	No bias	-65	+150	°C
T_{AMB}	Ambient temperature	Under bias, note (6)	-65	+135	°C
ESD	ElectroStatic Discharge Voltage		±900		V

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply Voltage	note (6)	4.75 (4.5)	5.25 (5.5)	V
V_I	INPUT voltage		0	V_{CC}	V
V_O	OUTPUT voltage		0	V_{CC}	V
T_A	Operating temperature	For Commercial	0	70	°C
T_A	Operating temperature	For Industrial	-40	85	°C
T_A	Operating temperature	For Military	-55	125	°C
T_R	INPUT rise time			500	ns
T_F	INPUT fall time			500	ns

DC OPERATING CHARACTERISTICS

(V_{CC} = 5V ± 5%, T_A = 0°C to 70°C for Commercial)
(V_{CC} = 5V ± 10%, T_A = -40°C to 85°C for Industrial)
(V_{CC} = 5V ± 10%, T_A = -55°C to 125°C for Military)
Note (1) and (6)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	HIGH level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	LOW level input voltage		-0.3		0.8	V
V_{OH}	HIGH level TTL output voltage	I_{OH} = -4mA DC	2.4			V
V_{OH}	HIGH level CMOS output voltage	I_{OH} = -2mA DC	3.84			V
V_{OL}	LOW level output voltage	I_{OL} = 4mA DC			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND note (6)	-10 (-20)		+10 (+20)	μA
I_{OZ}	3-state output off-state current	V_O = V_{CC} or GND note (6)	-10 (-20)		+10 (+20)	μA
I_{CC1}	V_{CC} supply current (standby)	V_I = V_{CC} or GND No load note (8)		3	6 (9)	mA
I_{CC2}	V_{CC} supply current (active)	V_I = V_{CC} or GND No load, f = 1.0 MHz note (7)		6	10 (13)	mA

CAPACITANCE

Note (4)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V f = 1.0 MHz		30	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V f = 1.0 MHz		40	pF
C_{CLK}	Clock Pin Capacitance	V_{IN} = 0V f = 1.0 MHz		30	pF

AC CHARACTERISTICS Note (5)

(V_{CC} = 5V ± 5%, T_A = 0° C to 70° C for Commercial)
(V_{CC} = 5V ± 10%, T_A = -40°C to 85°C for Industrial)
(V_{CC} = 5V ± 10%, T_A = -55°C to 125°C for Military)

			EP1210-1		EP1210-2		EP1210		
SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
t_{PD}	Input to non-registered output	C_1 = 30pF		50		65		90	ns
t_{PZX}	Input to output enable			50		65		90	ns
t_{PXZ}	Input to output disable	C_1 = 5pF note (2)		50		65		90	ns
t_{CLR}	Asynchronous output clear time	C_1 = 30pF		80		110		150	ns
t_{IO}	I/O input buffer delay			3		3		3	ns

SYNCHRONOUS CLOCK MODE

			EP1210-1		EP1210-2		EP1210		
SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
f_{MAX}	Maximum frequency	note (9)	28.5		23.2		17.5		MHz
t_{SU}	Input setup time		35		43		57		ns
t_H	Input hold time		0		0		0		ns
t_{CH}	Clock high time		17		21		28		ns
t_{CL}	Clock low time		17		21		28		ns
t_{CO1}	Clock to output delay			32		40		53	ns
t_{CNT}	Minimum clock period (register output feedback to register input - internal path)	note (7)		45		58		80	ns
f_{CNT}	Internal maximum frequency ($1/t_{CNT}$)	note (7)	22.2		17.2		12.5		MHz
t_{ILS}	Set up time for latching inputs		0		0		0		ns
t_{ILH}	Hold time for latching inputs		15		20		25		ns
t_{C1C2}	Minimum clock 1 to Clock 2 delay			40		50		65	ns
t_{P3}	Minimum period for a 2-clock system ($t_{C1C2} + t_{CO1}$)			72		90		118	ns
t_3	Maximum frequency ($1/t_{P3}$)		13.9		11		8.5		MHz

Notes:
1. Typical values are for T_A = 25°C, V_{CC} = 5V
2. Sample tested only for an output change of 500mV.
3. Minimum DC input is -0.3V. During transitions, the inputs may undershoot to -2.0V for periods less than 20ns.
4. Capacitance measured at 25°C. Sample tested only.
5. All AC values tested with TURBO-BIT™ programmed.
6. Figures in ( ) pertain to military and industrial temperature versions.
7. Measured with device programmed as a 26-Bit Counter.
8. EPLD automatically goes into standby mode if logic transitions do not occur when in non-turbo mode (approximately 100 ns after last transition).
9. The f_{MAX} values shown represent the highest frequency for pipelined data.

GRADE	AVAILABILITY	
Commercial (0°C to 70°C)	EP1210-2	EP1210
Industrial (-40°C to 85°C)	EP1210-2	EP1210
Military (-55°C to 125°C)	EP1210-2	EP1210

For devices other than shown please consult factory.

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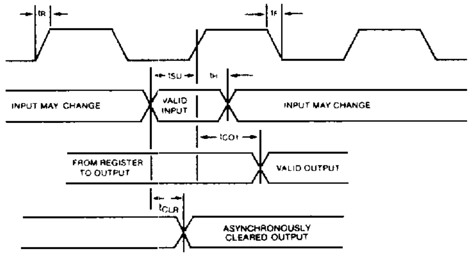
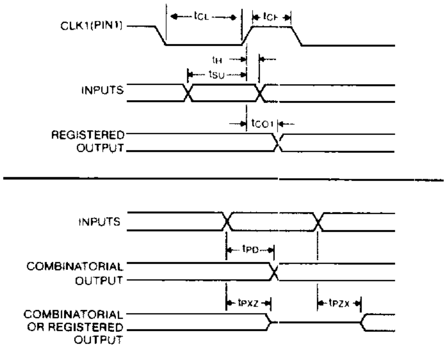
FIG. 6 SWITCHING WAVEFORMS
A.



Notes: t_R & t_F < 8ns
t_{CL} & t_{CH} measured at 0.3V and 2.7V
all other timings at 1.5V

FIG. 6 SWITCHING WAVEFORMS
B.

1-CLOCK SYSTEM: MODES 2 AND 3



INVERT CLK1 FOR MODE 2

FIG. 6 SWITCHING WAVEFORMS
C.

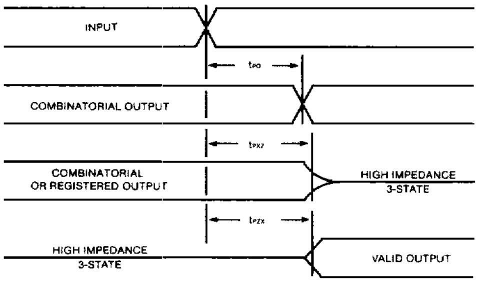
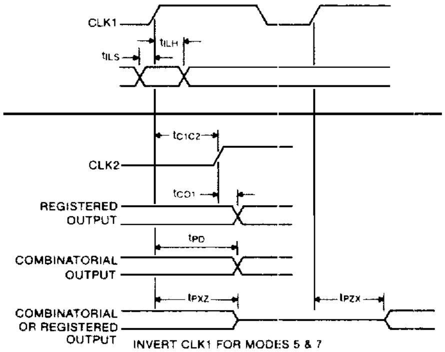


FIG. 6 SWITCHING WAVEFORMS
D.

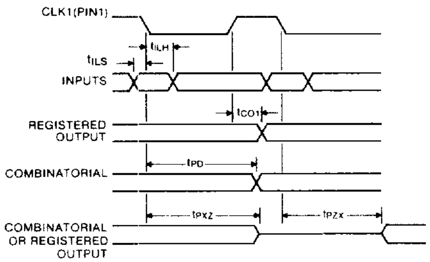
2-CLOCK SYSTEMS: MODES 4 THROUGH 7
CLK1 (PIN1) CONTROLS THE INPUT LATCH CLOCK
CLK2 (PIN38) CONTROLS THE D-FF CLOCK



INVERT CLK1 FOR MODES 5 & 7
INVERT CLK2 FOR MODES 4 & 5

FIG. 6 SWITCHING WAVEFORMS
E.

1-CLOCK SYSTEM: MODES 0 AND 1



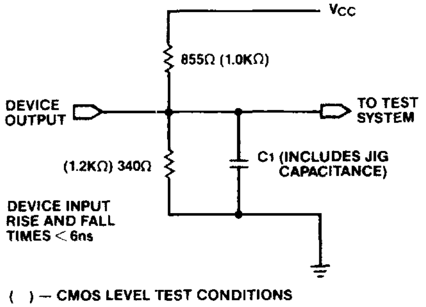
INVERT CLK1 FOR MODE 0

FUNCTIONAL TESTING

The EP1210 is fully functionally tested and guaranteed through complete testing of each programmable EPROM bit and all internal logic elements thus ensuring 100% programming yield.

As a result, traditional problems associated with fuse-programmed circuits are eliminated. The erasable nature of the EP1210 allows test program patterns to be used and then erased. This facility to use application-independent, general purpose tests is called generic testing and is unique among user-defined LSI logic devices.

FIG. 7 AC TEST CONDITIONS



Power supply transients can affect AC measurements, simultaneous transitions of multiple outputs should be avoided for accurate measurement. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.

DESIGN SECURITY

The EP1210 contains a programmable design security feature that controls the access to the data programmed into the device. If this programmable feature is used, a proprietary design implemented in the device cannot be copied or retrieved. This enables a high level of design control to be obtained since programmed data within EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset simply by erasing the device.

FIG. 8 ICC VS. FMAX

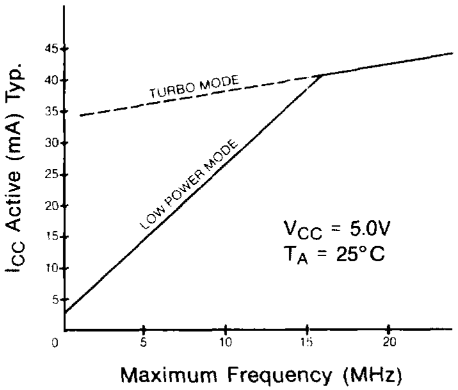
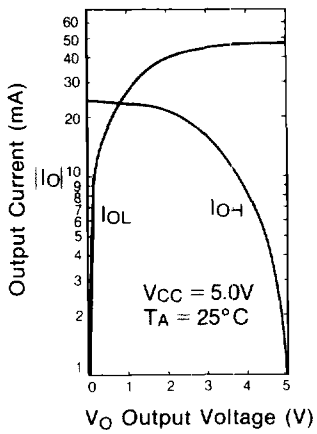


FIG. 9 OUTPUT DRIVE CURRENTS



2