EM27C512 512K (64K x 8) UVPROM

Features

- **Functional Compatible to AMD's AM27C512**
- **Fast Read Access Time – 45 ns**
- **Low-Power CMOS Operation**
  - **– 100 µA Max Standby**
  - **– 20 mA Max Active at 5 MHz**
- **JEDEC Standard Packages – 28-lead ceramic DIP**
- **5V ± 10% Supply**
- **High-Reliability CMOS Technology**
  - **– 2,000V ESD Protection**
  - **– 200 mA Latchup Immunity**
- **Rapid Programming Algorithm – 100 µs/Byte (Typical)**
- **CMOS and TTL Compatible Inputs and Outputs**
- **Integrated Product Identification Code**
- **Industrial, Extended Temperature Ranges and Military Screening**

1. Description

The EM27C512 is fabricated using high-density nonvolatile memory CMOS process and is assembled and tested in EM Semi approved assembly and test facilities. The device is offered in industrial, extended and a version screened to a military test flow.

The EM27C512 is a low-power, high-performance 524,288-bit UVPROM organized 64K by 8 bits. It requires only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 45 ns, eliminating the need for speed reducing WAIT states on high-performance microprocessor systems.

Atmel's scaled CMOS technology provides high-speed, lower active power consumption, and significantly faster programming. Power consumption is typically only 8 mA in Active Mode and less than 10 µA in Standby.

The EM27C512 is available in industry-standard JEDEC-approved ceramic DIP packages. All devices feature two-line control (CE_{NOT}, OE_{NOT}) to give designers the flexibility to prevent bus contention.

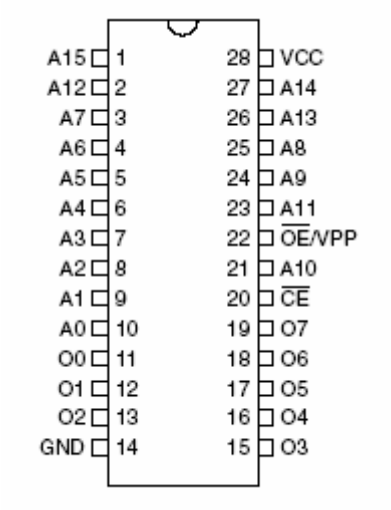
With 64K byte storage capability, the EM27C512 allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

EM27C512 has additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry-standard programming equipment to select the proper programming algorithms and voltages.

2. Pin Configurations

Pin Name	Function
A0 – A15	Addresses
O0 - O7	Outputs
CE_{NOT}	Chip Enable
OE_{NOT}/VPP	Output Enable/ Program Supply
NC	No Connect

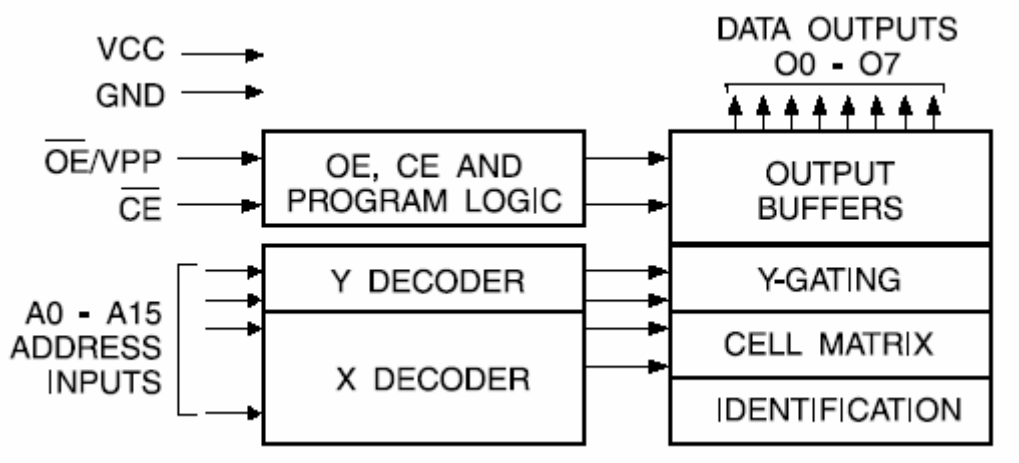
2.1 28-lead Ceramic DIP Top View



3. System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed datasheet limits, resulting in device non-conformance. At a minimum, a 0.1 µF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

4. Block Diagram



5. Absolute Maximum Ratings*

Temperature Under Bias..... -55°C to + 125°C
Storage Temperature ..... -65°C to + 150°C
Voltage on Any Pin with
Respect to Ground .....-2.0V to + 7.0V(1)
Voltage on A9 with
Respect to Ground .....-2.0V to + 14.0V(1)
V_{PP} Supply Voltage with
Respect to Ground .....-2.0V to + 14.0V(1)

* NOTICE:
Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
1. Minimum voltage is -0.6V DC which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V DC which may overshoot to +7.0 volts for pulses of less than 20 ns.

6. Operating Modes

Mode/Pin	CE_{NOT}	OE_{NOT}/V_{PP}	Ai	Outputs
Read	V_{IL}	V_{IL}	Ai	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X(1)	High Z
Standby	V_{IH}	X(1)	X	High Z
Rapid Program(2)	V_{IL}	V_{PP}	Ai	D_{IN}
PGM Inhibit	V_{IH}	V_{PP}	X(1)	High Z
Product Identification(4)	V_{IL}	V_{IL}	A9 =V_H(3) A0 = V_{IH} or V_{IL} A1 - A15 = V_{IL}	Identification Code

Notes:
1. X can be V_{IL} or V_{IH}.

2. Refer to Programming Characteristics.

3. V_H = 12.0 ± 0.5V.

4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

7. DC and AC Operating Conditions for Read Operation

		EM27C512	
		-45	**-70 / -90**
Operating Temp.(Case)	Industrial	-40°C - 85°C	-40°C - 85°C
	Extended	-45°C - 115°C	-45°C - 115°C
	Military	-55°C - 125°C	-55°C - 125°C
V_{CC} Supply		5V ± 10%	5V ± 10%

8. DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}	Ind.		±1	µA
			Ext. / Mil.		±5	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}	Ind.		±5	µA
			Ext. / Mil.		±10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1}(CMOS), CE_{NOT} = V_{CC} ±0.3V			100	µA
		I_{SB2}(TTL), CE_{NOT} = 2.0 to V_{CC}+0.5V			1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT}= 0 mA, CE_{NOT} = V_{IL}			20	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC}+ 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH}= -400 µA		2.4		V

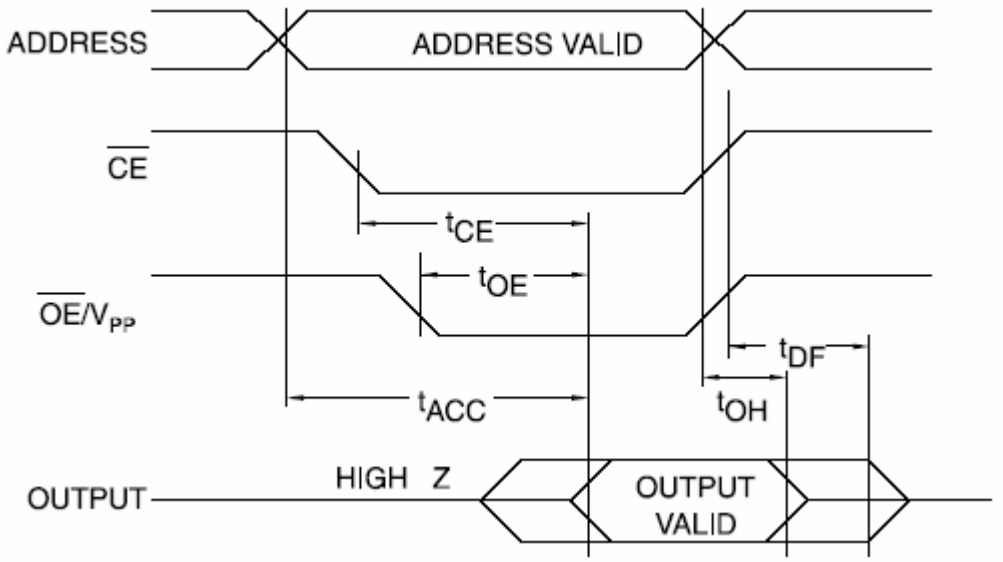
Note: 1. V_{CC} must be applied simultaneously with or before OE_{NOT}/V_{PP}, and removed simultaneously with or after OE_{NOT}/V_{PP}.

9. AC Characteristics for Read Operation

Symbol	Parameter	Condition	EM27C512				Units
			-45		-70 / -90		
			Min	Max	Min	Max	
t_{ACC}(1)	Address to Output Delay	CE_{NOT} = OE_{NOT}/V_{PP} = V_{IL}		45		70	ns
t_{CE}(1)	CE_{NOT} to Output Delay	OE_{NOT}/V_{PP} = V_{IL}		45		70	ns
t_{OE}(1)	OE_{NOT}/V_{PP} to Output Delay	CE_{NOT} = V_{IL}		20		30	ns
t_{DF}(1)	OE_{NOT}/V_{PP} or CE_{NOT} High to Output Float, Whichever Occurred First			20		25	ns
t_{OH}	Output Hold from Address, CE_{NOT} or OE_{NOT}/V_{PP}, Whichever Occurred First		7		7		ns

Note: 1. See AC Waveforms for Read Operation.

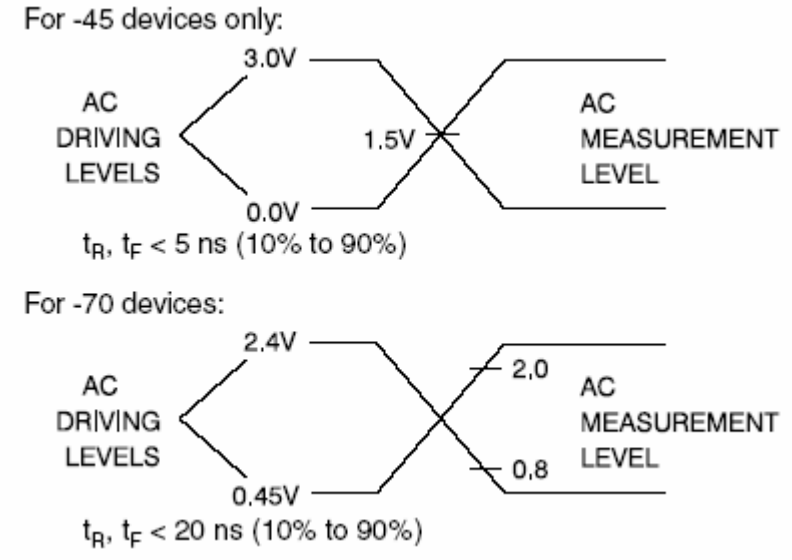
10. AC Waveforms for Read Operation(1)



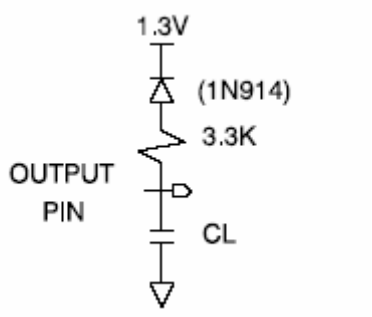
Notes:

1. Timing measurement reference level is 1.5V for -45 devices. Input AC drive levels are V_{IL} = 0.0V and V_{IH} = 3.0V. Timing measurement reference levels for all other speed grades are V_{OL} = 0.8V and V_{OH} = 2.0V. Input AC drive levels are V_{IL} = 0.45V and V_{IH} = 2.4V.
2. OE_{NOT}/V_{PP} may be delayed up to t_{CE} - t_{OE} after the falling edge of CE_{NOT} without impact on t_{CE}.
3. OE_{NOT}/V_{PP} may be delayed up to t_{ACC} - t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

11. Input Test Waveforms and Measurement Levels



12. Output Test Load



Note:

1. C_L = 100 pF including jig capacitance, except for the -45 devices, where C_L = 30 pF.

13. Pin Capacitance

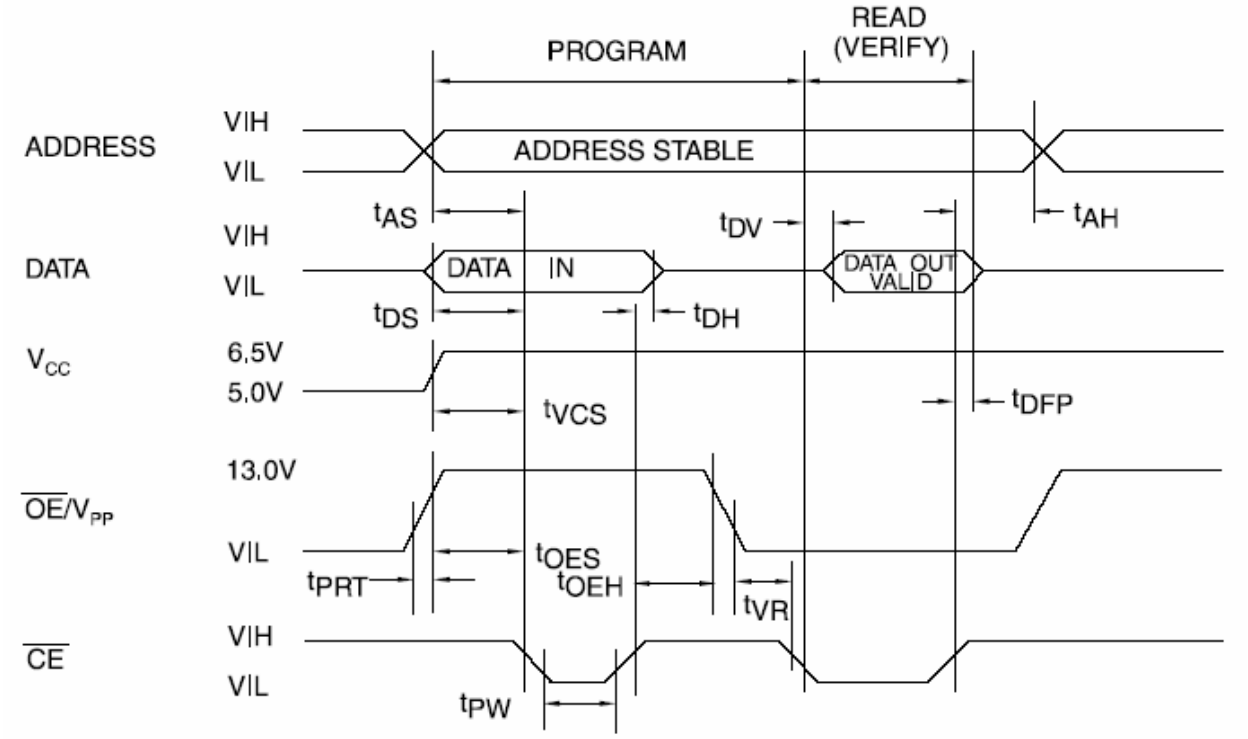
f = 1 MHz, T = 25°C (1)

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN}= 0V
C_{OUT}	8	12	pF	V_{OUT}= 0V

Note:

1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

14. Programming Waveforms(1)



Notes:

1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

15. DC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, OE_{NOT}/V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
I_{LI}	Input Load Current	$V_{IN}= V_{IL}, V_{IH}$		±10	µA
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			25	mA
I_{PP2}	OE_{NOT}/V_{PP}Current	$CE_{NOT} = V_{IL}$		25	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

16. AC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, OE_{NOT}/V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions(1)	Limits		Units
			Min	Max	
t_{AS}	Address Setup Tim		2		µs
t_{OES}	OE_{NOT}/V_{PP} Setup Time		2		µs
t_{OEH}	OE_{NOT}/V_{PP} Hold Time	Input Rise and Fall Times	2		µs
t_{DS}	Data Setup Time	(10% to 90%) 20 ns	2		µs
t_{AH}	Address Hold Time	Input Pulse Levels	0		µs
t_{DH}	Data Hold Time	0.45V to 2.4V	2		µs
t_{DFP}	CE_{NOT} High to Output Float Delay(2)	Input Timing Reference Level	0	130	ns
t_{VCS}	V_{CC} Setup Time	0.8V to 2.0V	2		µs
t_{PW}	CE_{NOT} Program Pulse Width(3)	Output Timing Reference Level	95	105	µs
t_{DV}	Data Valid from CE_{NOT}(2)	0.8V to 2.0V		1	µs
t_{VR}	OE_{NOT}/V_{PP} Recovery Time		2		µs
t_{PRT}	OE_{NOT}/V_{PP} Pulse Rise Time During Programming		50		ns

Notes:

1. V_{CC} must be applied simultaneously or before OE_{NOT}/V_{PP} and removed simultaneously or after OE_{NOT}/V_{PP}.

2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven – see timing diagram.

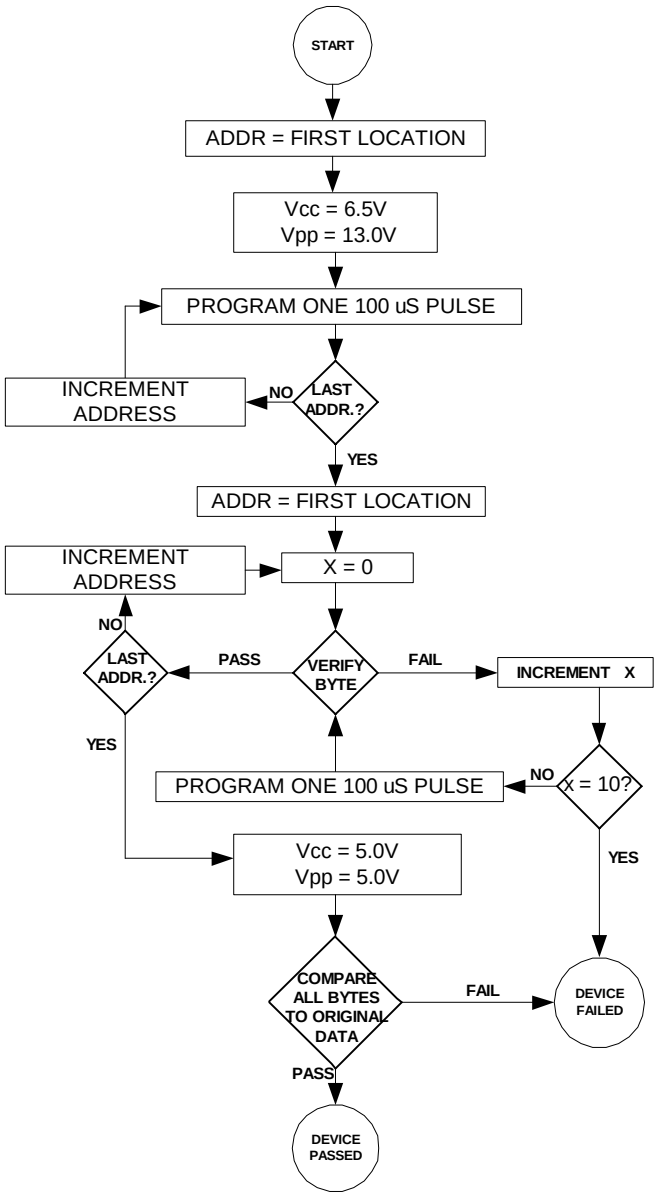
3. Program Pulse width tolerance is 100 µsec ± 5%.

17. EM27C512 Integrated Product Identification Code

Codes	Pins									Hex Data
	A0	O7	O6	O5	O4	O3	O2	O1	O0	
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	0	1	1	0	1	0D

18. Rapid Programming Algorithm

A 100 µs CE_{NOT} pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and OE_{NOT}/V_{PP} is raised to 13.0V. Each address is first programmed with one 100 µs CE_{NOT} pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. OE_{NOT}/V_{PP} is then lowered to V_{IL} and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



19. Ordering Information

EM27C512 – XX X X