Application Information

PLANAR REFRESH

The planar refresh feature of the 2105 allows all 1024 memory cells to be refreshed at one time. A positive transition of the refresh signal with Cenable (CE) low initiates an internally generated refresh pulse. (If the positive refresh transition occurs during CE high, the refresh pulse will be generated at the falling edge of Cenable.) The duration of the refresh pulse is established by the time t_{RH}.

The timing of the 2105 allows the refresh pulse to be contained within a normal cycle (read, write or read-modify-write) without an increase of cycle length. When the memory is inactive (not executing cycles), data may be retained by meeting the refresh requirements (i.e., at least one refresh pulse every 10μs).

During each refresh pulse, a typical current surge in the order of 100mA and 20ns duration is drawn from the V_{DD} supply. Thus refresh power is typically given by:

$$P_{REF} = V_{DD} \times 100mA \times \frac{.02\mu s}{t_{REF}} = \frac{24}{t_{REF}} \text{ mW}$$

At $t_{REF} = 10\mu s$, P_{REF} is approximately 2.4mW

Because of the presence of I_{DD} current spikes during refreshing and at leading and falling edges of CE, adequate bypassing of power supplies is necessary.

STANDBY POWER MODE

The 2105 is a dynamic RAM and goes into a power down or standby power mode when it is not being accessed. That is, when Cenable is at V_{IL} voltage and all address inputs are at V_{IL} voltage, the only currents flowing through the device are I_{DDS} and I_{BBS}. Power consumed during periodic (every 10μs) planar refresh is also part of standby power and is included in the I_{DDS} and I_{BBS}.

RETURN TO ZERO ADDRESS MODE

In normal operation all address lines must be returned to their low levels (V_{IL}) prior to the start of each memory cycle to ensure proper pre-conditioning internal to the device. To conserve additional power, addresses should be held at low levels in non-accessed devices, or in parts in which data is being retained.

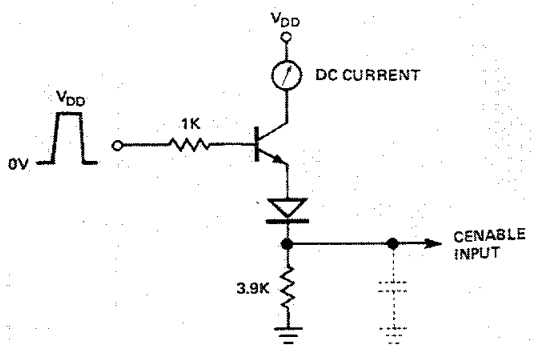
EFFECTIVE CAPACITANCE

The Cenable effective input capacitance was determined by measuring the amount of charge (Q) required to charge the Cenable input from ground (V_{IL}) to V_{IHC}.

$$C_{Eff} = \frac{Q}{V_{IHC} - V_{IL}}$$

The test circuit shown measures Q by reading the average charging current ΔI_{AV} when Cenable input is driven at a frequency f.

$$C_{Eff} = \frac{\Delta I_{AV}}{f\,(V_{IHC} - V_{IL})}$$, where ΔI_{AV} is the difference in the meter reading with the CE input disconnected and then connected.



An alternative way to measure effective capacitance is to observe the current spike with a current probe that results from the voltage ramp at Cenable input. By taking the area under the current spike waveform as a measure of the total charge transfer (including any non-capacitive current spikes), the effective capacitance can be calculated.

MEMORY SYSTEM INTERFACE

To simplify interfacing and minimize package count the 3210 (TTL compatible) and the 3211 (ECL compatible) will be introduced in the fall. Each 3210 and 3211 contain four address drivers and one clock driver designed specifically for the 2105.

Capacitance [1] $T_A = 25°C$, $V_{DD} = 12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{SS} = 0V$, unless otherwise specified.

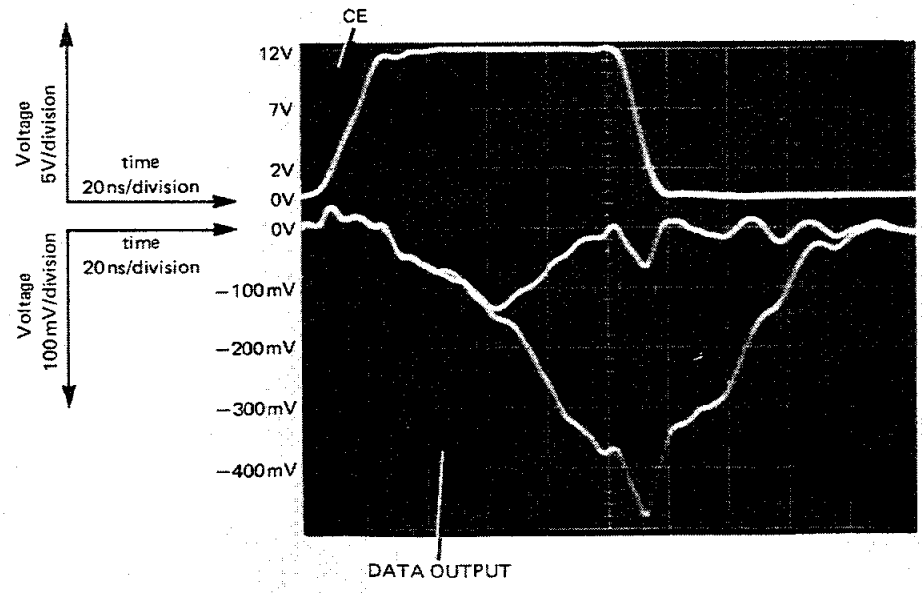
Symbol	Parameter	Plastic Pkg. Typ.	Plastic Pkg. Max.	Unit	Conditions
C_{IN}	Input Capacitance (Address, D_{IN}, WE, Ref)	4	6	pF	$V_{IN} = V_{SS}$
C_{OUT}	Data Out Capacitance	4	6	pF	$V_{IN} = V_{SS}$
C_{CE}	Effective Cenable Capacitance	65	85	pF	Note 2

f = 1MHz. All Unused Pins Are at V_{SS}.

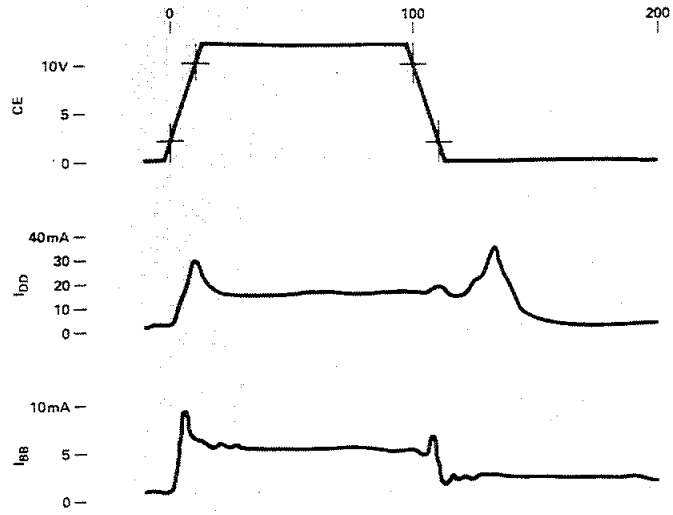
NOTES:
1. This parameter is periodically sampled and is not 100% tested. They are measured at worst case operating conditions.
2. Refer to page 7 for information on how effective capacitance was measured.

Typical Data Output Characteristics

The actual oscilloscope photo below shows the Cenable input and the resulting data outputs of two address locations during read of a typical device. One location with a one (high) stored and the other with a zero (low) stored. The output would normally be strobed at t_{CO} time. For a high output the condition of V_{OH1} between 0V and −110mV must be met. For a low output the condition of V_{OL1} more negative than −120mV must be met.

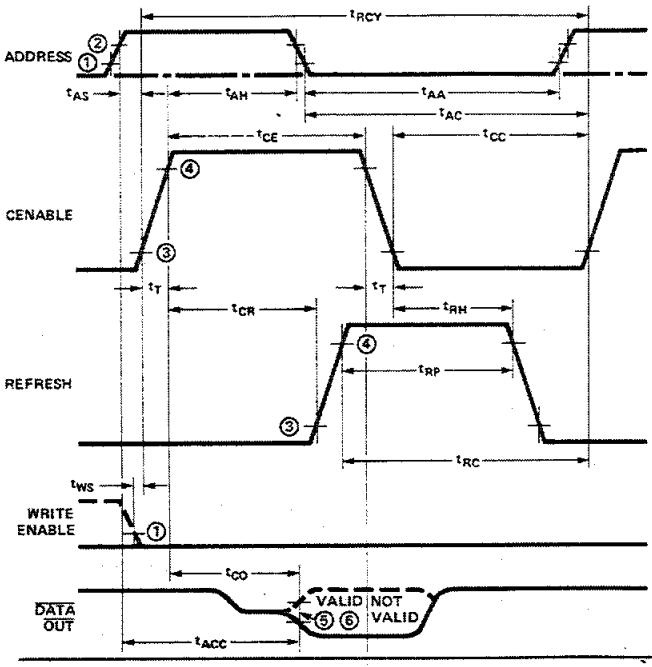


Typical Current Transients vs. Time

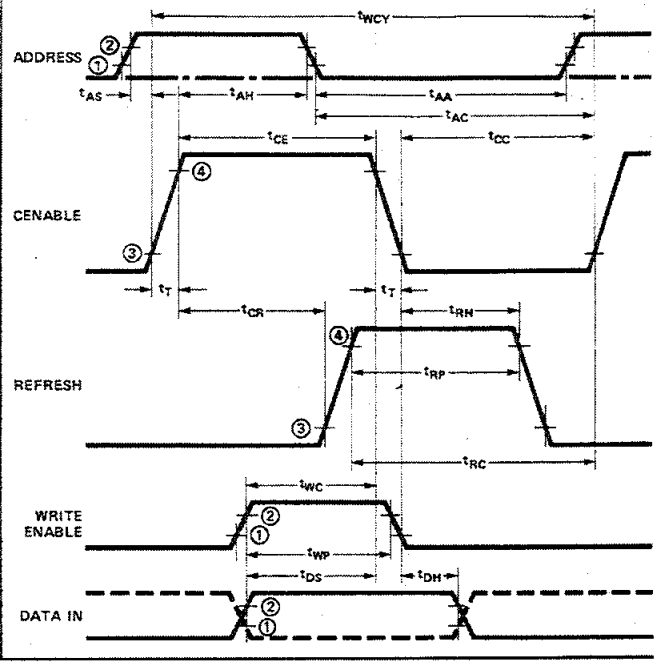


Waveforms

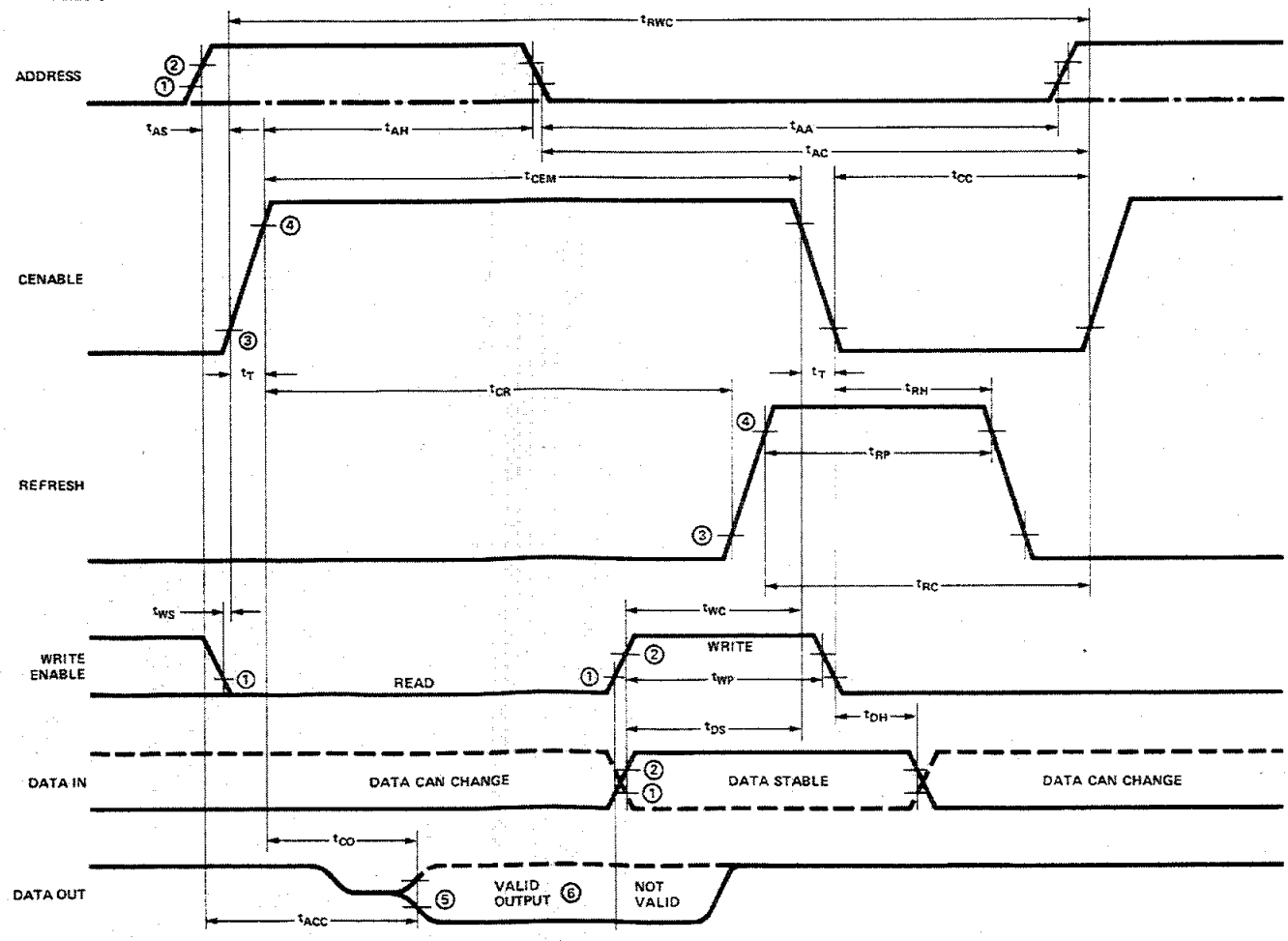
READ CYCLE



WRITE CYCLE



READ MODIFY WRITE CYCLE



NOTES:
① V_{SS} = + 1.5V
② V_{SS} = + 3.0V
③ V_{SS} = + 2.0V
④ V_{DD} = −2.0V
⑤ The parameter t_{CO} is defined at V_{OL1} or V_{OH1}, whichever occurs last. R_L = 100Ω, C_L = 50pF.
⑥ Data Out is valid during t_{CE} time or until Write Enable goes high.

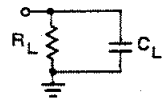
A.C. Characteristics $T_A = 0°C$ to $70°C$, $V_{DD} = 12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$,[1] $V_{SS} = 0V$, unless otherwise specified.[9]

READ, WRITE, and READ MODIFY WRITE CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{REF}	Time Between Planar Refresh Pulses	1	10	μs	
t_{AS}	Address to Cenable Set Up Time	10		ns	
t_{AH}	Address Hold Time	50		ns	
t_{AA}	Address Low Time	30		ns	
t_{AC}	Address to Cenable End	30		ns	
t_{CE}	Cenable On Time	90	500	ns	
t_{CC}	Cenable Off Time	90		ns	

READ CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RCY}[6]	Read Cycle	200		ns	$t_T = 10ns$
t_{WS}	Write Enable to Cenable Set Up Time	0		ns	
t_{CO}	Cenable Output Delay		75	ns	$C_{LOAD} = 50pF$, $R_{LOAD} = 100\Omega$
t_{ACC}[7]	Address to Output Access		95	ns	Refer to Note 4



WRITE CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{WCY}[6]	Write Cycle	200		ns	$t_T = 10ns$
t_{WP}	Write Enable Pulse Width	70		ns	
t_{WC}	Write Enable to Cenable End	70		ns	
t_{DS}[2]	Data Set Up Time	70		ns	
t_{DH}[3]	Data Hold Time	20		ns	

READ MODIFY WRITE CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RWC}[8]	Read Modify Write Cycle	265		ns	$t_T = 10ns$
t_{CEM}	Cenable On Time	155	500	ns	

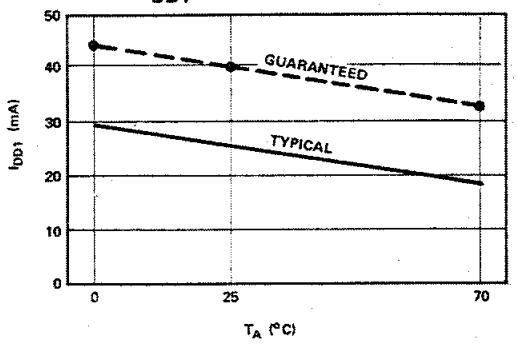
PLANAR REFRESH TIMING

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{CR}[5]	Cenable to Refresh Start	50		ns	
t_{RH}	Refresh Hold Time	50		ns	
t_{RP}	Refresh Pulse Width	50	500	ns	
t_{RC}	Refresh to Cenable Start	90		ns	
t_{REF}	Time Between Planar Refresh	1	10	μs	

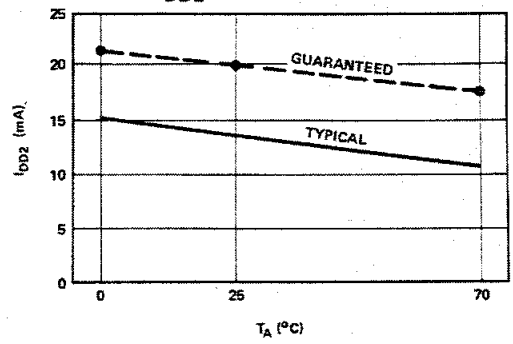
NOTES:
1. The V_{BB} supply also may be equal to $-5.2V \pm 5\%$.
2. The parameter t_{DS} is referenced to the falling edge of Cenable (④) or Write Enable (②), whichever occurs first.
3. The parameter t_{DH} is referenced to the falling edge of Cenable (③) or Write Enable (①), whichever occurs first.
4. The parameter t_{CO} is defined at V_{OL1} or V_{OH1}, whichever occurs last.
5. The parameter t_{CR} only applies when Cenable is going high (towards V_{DD}). For unselected devices (Cenable low) a refresh pulse width t_{RP} is all that is required.
6. The parameter t_{RCY} and t_{WCY} are defined as $t_T + t_{CE} + t_T + t_{CC}$.
7. The parameter t_{ACC} is defined as $t_{AS} + t_T + t_{CO}$, where $t_T = 10ns$.
8. The parameter t_{RWC} is defined as $t_{CO} + t_{WC} + 3t_T + t_{CC}$ + modify time or $t_T + t_{CEM} + t_T + t_{CC}$ + modify time.
9. The only requirement for the sequence of applying voltage to the device is that V_{DD} and V_{SS} should never be 0.3V more negative than V_{BB}.

Typical D.C. Characteristics

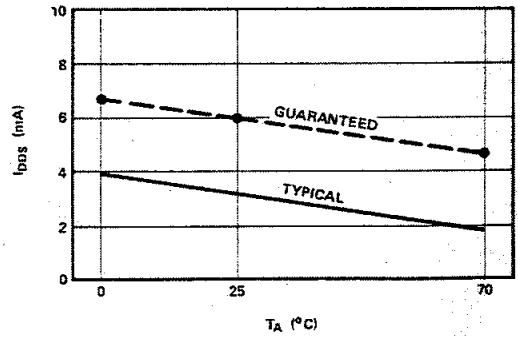
I_{DD1} VS. TEMPERATURE



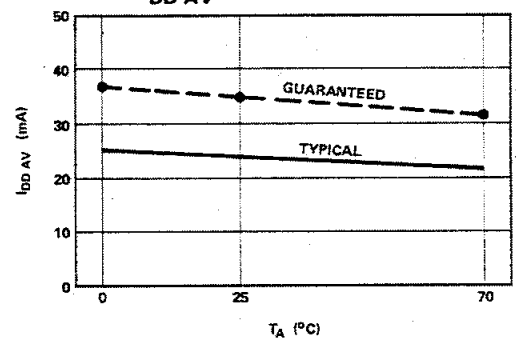
I_{DD2} VS. TEMPERATURE



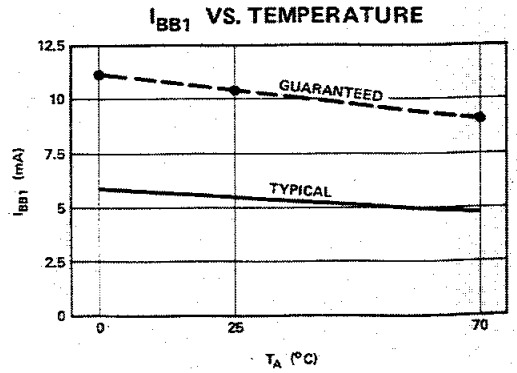
I_{DDS} VS. TEMPERATURE



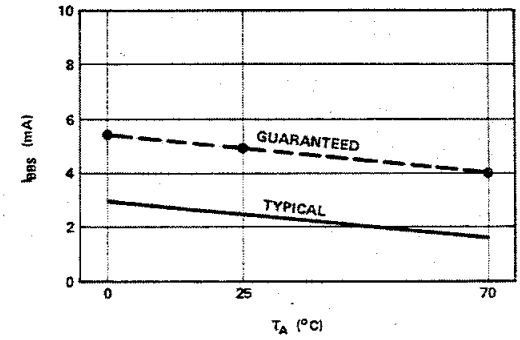
$I_{DD\ AV}$ VS. TEMPERATURE



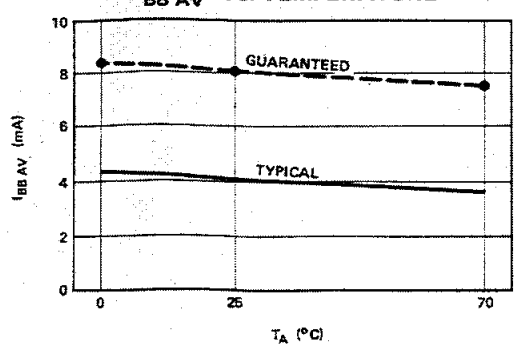
I_{BB1} VS. TEMPERATURE



I_{BBS} VS. TEMPERATURE



$I_{BB\ AV}$ VS. TEMPERATURE



Absolute Maximum Ratings*

Temperature Under Bias . . . . . 0°C to 70°C

Storage Temperature . . . . . −65°C to +150°C

All Input or Output Voltages with Respect to the most Negative Supply Voltage, V_{BB} . . . . . +25V to −0.3V

Supply Voltages V_{DD} and V_{SS} with Respect to V_{BB} . . . . . +20V to −0.3V

Power Dissipation 1.0W

**COMMENT:*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{BB} = −5V ± 5%[3], V_{SS} = 0V[4], unless otherwise specified.[2]

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[1]	Max.		
I_{LI}	Input Load Current (Address, D_{IN}, WE)			10	μA	V_{IN} = 0V to 6.5V
I_{LIC}	Input Load Current (CE, Ref)			10	μA	V_{IN} = 0V to V_{DD} + 0.5V
I_{LO}	Output Leakage Current			1	μA	V_O = 0V
I_{DD1}	V_{DD} Current During Cenable ON		25	40	mA	V_{CE} = 13.1V, V_{IN} = 0V to 4V, T_A = 25°C
I_{DD2}	V_{DD} Current During Cenable OFF, Address High		13	20	mA	V_{CE} = 0V, V_{IN} = 4V, T_A = 25°C
I_{DDS}	Average Standby V_{DD} Current During Cenable OFF		3.0	6.0	mA	V_{CE} = 0V, V_{IN} = 0V, T_A = 25°C t_{REF} = 10μs
$\lvert I_{BB1} \rvert$	V_{BB} Current During Cenable ON		5.5	10.5	mA	V_{CE} = 13.1V, V_{IN} = 0V to 4V, D_{OUT} = 0V, T_A = 25°C
$\lvert I_{BBS} \rvert$	Standby V_{BB} Current During Cenable OFF		2.5	5.0	mA	V_{CE} = 0V, V_{IN} = 0V to 4V, D_{OUT} = 0V, t_{REF} = 10μs, T_A = 25°C
$I_{DD\,AV}$	Average V_{DD} Supply Current		23	35	mA	t_{cyc} = 200ns, t_{REF} = 10μs, T_A = 25°C
$\lvert I_{BB\,AV} \rvert$	Average V_{BB} Supply Current		4	8	mA	t_{cyc} = 200ns, t_{REF} = 10μs, T_A = 25°C
V_{IL}	Input Low Level Voltage (All Inputs)	V_{SS} −1		V_{SS} +1	V	
V_{IH}	Input High Level Voltage (Address, D_{IN}, WE)	4.0		6.5	V	
V_{IHC}	Input High Level Voltage (CE, Ref)	V_{DD} −1		V_{DD} +0.5	V	
V_{OL1}	Output Low Voltage point 1			−120	mV	R_L = 100Ω at t_{CO}
V_{OH1}	Output High Voltage point 1	−110			mV	R_L = 100Ω at t_{CO}
V_{OL2}	Output Low Voltage point 2			−180	mV	R_L = 100Ω at t_{CO} + 20ns
V_{OH2}	Output High Voltage point 2	−20			mV	R_L = 100Ω at t_{CO} + 20ns

NOTES:
1. Typical values are for T_A=25°C and nominal supply voltages.
2. The only requirement for the sequence of applying voltage to the device is that V_{DD} and V_{SS} should never be 0.3V more negative than V_{BB}.
3. The V_{BB} supply also may be equal to −5.2V ± 5%.
4. The current I_{SS} is $I_{DD} - I_{BB}$.

1024 BIT HIGH SPEED DYNAMIC MOS RANDOM ACCESS MEMORY

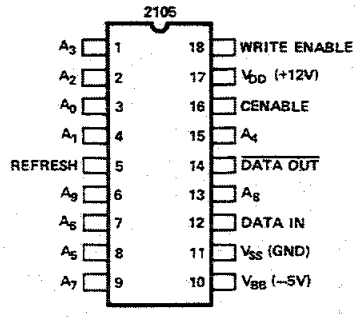
- **High Speed N-Channel— 95 ns Maximum Access Time**
- **Cycle Time—200 ns Maximum**
- **Planar Refresh**
- **Standby Power—100 μW/Bit**
- **Fully Decoded—On Chip Address Decode**
- **Low Level Address, Data, Write Enable Inputs**
- **Current Sinking Output**
- **OR-Tie Capability**
- **All Inputs Have Protection Against Static Charge**
- **Standard 18-Pin Dual In-Line Packages**

The Intel 2105 is a very high speed 1024 word by one bit dynamic random access memory element using normally off N-Channel MOS devices integrated on a monolithic array.

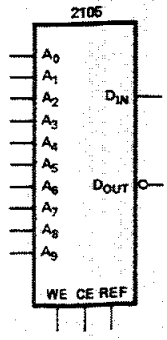
The 2105 is designed for memory applications where very high speed, low cost, and low power dissipation are important design objectives. The planar refresh mode of operation simplifies system design and allows all 1024 memory cells to be refreshed at once.

The Intel 2105 is fabricated with N-Channel silicon gate technology. This technology allows the design and production of high performance, easy to use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-Channel silicon gate technology.

PIN CONFIGURATION



LOGIC SYMBOL



PIN NAMES

D_{IN}	DATA INPUT	CE	CHIP ENABLE
A_0-A_9	ADDRESS INPUTS	REF	REFRESH INPUT
WE	WRITE ENABLE	$\overline{D_{OUT}}$	DATA OUTPUT

BLOCK DIAGRAM