NATIONAL

MOS RAMs

MM4261/MM5261 1024-bit fully decoded dynamic random access memory

general description

The MM4261/MM5261 fully decoded dynamic 1024 word x 1-bit word read/write Random Access Memory is a monolithic MOS integrated circuit using silicon gate low threshold technology to achieve bipolar compatibility on all I/O lines except the precharge and read/write lines. This provides an efficient approach to memory design using these systems oriented devices. The MM4261/MM5261 is used for main memory applications where large bit storage and improved operating performance are important. A TRI-STATE® output is utilized to allow wired "OR" capability and common I/O data busing in memory applications.

features

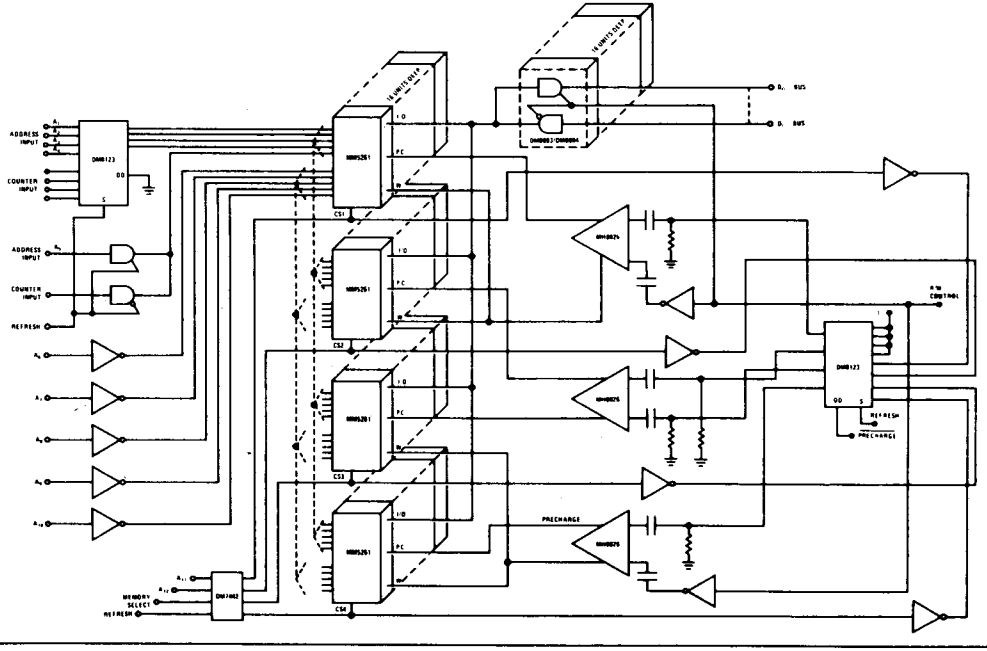
- Fast access time 300 typ
- Fast cycle time MM4261 600 ns read cycle min
  MM5261 500 ns read cycle min
  MM4261 750 ns write cycle min
  MM5261 625 ns write cycle min
- Low overhead circuit count Fully decoded
- Systems-oriented design
  Bipolar compatible (address lines, chip enable data I/O)
  Common data I/O line
  TRI-STATE output
- Refresh cycle 2.0 ms
- Easy memory expansion Chip enable
- Device protection All I/O lines have protection against static charge
- Low power dissipation 400 mW
- Small package size 18 pin dual-in-line package

applications

- High speed mainframe memory
- Mass memory storage

typical application

Main Memory Module Storing 4096 16-Bit Words



absolute maximum ratings (Note 3)

All Input or Output Voltages With Respect to Most Positive Supply Voltage V_{BB}	+0.3V to −22V
Power Dissipation	700 mW
Operating Temperature Range	
MM5261	0°C to +70°C
MM4261	−55°C to +125°C
Storage Temperature Range	−65°C to +160°C
Lead Temperature (Soldering, 10 seconds)	300°C

dc operating characteristics (MM4261) $T_A = -55°C$ to $+125°C$,

$V_{SS} = +5.0V \pm 5\%$, $V_{DD} = -12V \pm 5\%$, $(V_{BB} - V_{SS}) = 1.5V$ to $2.0V$ (Note 2), unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage (Address Input, Chip Enable and Data Input)					
Logic "1" (V_{IH})		$V_{SS} - 2.0$		$V_{SS} + 0.7$	V
Logic "0" (V_{IL})				$V_{SS} - 4.2$	V
Input Voltage (Precharge and Read/Write)					
Logic "1" (V_{IH})		$V_{SS} - 1.5$		$V_{SS} + 0.7$	V
Logic "0" (V_{IL})		$V_{SS} - 15$		$V_{SS} - 18$	V
Output Voltage Data Output					
Logic "1" (V_{OH})	$I_L = 200\mu A$ Source	2.4			V
Logic "0" (V_{OL})	$I_L = 1.6$ mA Sink			0.4	V
Standby Current (Note 1)	No Clocks, $\overline{CE} = V_{IH}$		6.0	12	mA
Average Supply Current (I_{SS}) (Note 1)	$t_{PW} = 300$, $t_{RC} = 600$ ns		20	34	mA
V_{BB} Supply Current				100	μA

ac operating characteristics (MM4261) $T_A = -55°C$ to $+125°C$,

$V_{SS} = +5.0V \pm 5\%$, $V_{DD} = -12V \pm 5\%$, $(V_{BB} - V_{SS}) = 1.5V$ to $2.0V$ (Note 2), unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Read Cycle (t_{RC})		600			ns
Write Cycle (t_{WC})		750			ns
Read/Write Cycle (t_{RWC})		$t_{ACC} + t_D + t_{WP} + t_{WRP} - t_{AP}$			
Address to $\overline{\text{Chip Enable}}$ (t_{AC})		0		50	ns
Address to Precharge (t_{AP})		0		50	ns
Precharge Width (t_{PW})		300		450	ns
Address Hold Time (t_{AH})		50			ns
Chip Enable Hold Time (t_{CH})		110			ns
Access Time (t_{ACC})			350	450	ns
Precharge Off Time (t_{PP})		300			ns
Precharge Leading Edge to R/$\overline{W}$ Leading Edge (t_{PWL})		225			ns
Read/$\overline{\text{Write}}$ Pulse Width (t_{WP})		300		450	ns
Read/$\overline{\text{Write}}$ Trailing Edge to Precharge Leading Edge (t_{WRP})		225			ns
Precharge Trailing to R/$\overline{W}$ Trailing (t_{PTW})		225			ns
Precharge to R/$\overline{W}$ Delay (t_{PWD})				500	ns
Refresh Interval (t_{REF})	(Note 6)			1.0	ms

capacitance characteristics (MM4261) (Note 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Address Capacitance (C_A)	$V_{IN} = V_{SS}$		5.0	7.0	pF
Chip Enable Capacitance (C_{CE})	$V_{IN} = V_{SS}$		5.0	9.0	pF
Precharge Capacitance (C_{PC})	$V_{IN} = V_{SS}$		25	45	pF
Read/Write Capacitance (C_{RW})	$V_{IN} = V_{SS}$		10	20	pF
Data Input/Output Capacitance ($C_{IN/OUT}$)	$V_{IN} = V_{SS}$		7.0	9.0	pF

f = 1 MHz, All Unused Inputs Are at AC Ground

dc operating characteristics (MM5261) $T_A = 0°C$ to $+70°C$,

$V_{SS} = +5.0V \pm 5\%$, $V_{DD} = -12V \pm 5\%$, $(V_{BB} - V_{SS}) = 1.5V$ to $2.0V$ (Note 2), unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage (Address Input, Chip Enable and Data Input)					
Logic "1" (V_{IH})		$V_{SS} - 2.0$		$V_{SS} + 0.7$	V
Logic "0" (V_{IL})				$V_{SS} - 4.2$	V
Input Voltage (Precharge and Read/Write)					
Logic "1" (V_{IH})		$V_{SS} - 1.5$		$V_{SS} + 0.7$	V
Logic "0" (V_{IL})		$V_{SS} - 15$		$V_{SS} - 18$	V
Output Voltage Data Output					
Logic "1" (V_{OH})	$I_L = 200\mu A$ Source	2.4			V
Logic "0" (V_{OL})	$I_L = 1.6$ mA Sink			0.4	V
Standby Current (Note 1)	No Clocks, $\overline{CE} = V_{IH}$		6.0	12	mA
Average Supply Current (I_{SS}) (Note 1)	$t_{PW} = 250$ ns, $t_{RC} = 500$ ns		20	34	mA
V_{BB} Supply Current				100	μA

ac operating characteristics (MM5261) $T_A = 0°C$ to $+70°C$,

$V_{SS} = +5.0V \pm 5\%$, $V_{DD} = -12V \pm 5\%$, $(V_{BB} - V_{SS}) = 1.5V$ to $2.0V$ (Note 2), unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Read Cycle (t_{RC})		500			ns
Write Cycle (t_{WC})		625			ns
Read/Write Cycle (t_{RWC})		$t_{ACC} + t_D + t_{WP} + t_{WRP} - t_{AP}$			
Address to $\overline{\text{Chip Enable}}$ (t_{AC})		0		50	ns
Address to Precharge (t_{AP})		0		50	ns
Precharge Width (t_{PW})		250		400	ns
Address Hold Time (t_{AH})		50			ns
Chip Enable Hold Time (t_{CH})		110			ns
Access Time (t_{ACC})			300	400	ns
Precharge Off Time (t_{PP})		250			ns
Precharge Leading Edge to R/$\overline{W}$ Leading Edge (t_{PWL})		175			ns
Read/$\overline{\text{Write}}$ Pulse Width (t_{WP})		250		400	ns
Read/$\overline{\text{Write}}$ Trailing Edge to Precharge Leading Edge (t_{WRP})		200			ns
Precharge Trailing to R/$\overline{W}$ Trailing (t_{PTW})		175			ns
Precharge to R/$\overline{W}$ Delay (t_{PWD})				500	ns
Refresh Interval (t_{REF})	(Note 6)			2.0	ms

capacitance characteristics (MM5261) (Note 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Address Capacitance (C_A)	$V_{IN} = V_{SS}$		5.0	7.0	pF
Chip Enable Capacitance (C_{CE})	$V_{IN} = V_{SS}$		5.0	9.0	pF
Precharge Capacitance (C_{PC})	$V_{IN} = V_{SS}$	f = 1 MHz, All Unused Inputs Are at AC Ground	25	45	pF
Read/Write Capacitance (C_{RW})	$V_{IN} = V_{SS}$		10	20	pF
Data Input/Output Capacitance ($C_{IN/OUT}$)	$V_{IN} = V_{SS}$		7.0	9.0	pF

Note 1: $V_{SS} = 5.0V$, $V_{DD} = -12V$, $T_A = 25°C$.

Note 2: Under power turn on conditions care must be taken to insure that V_{BB} is always the most positive potential in the system or large transient currents could result causing permanent damage.

Note 3: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

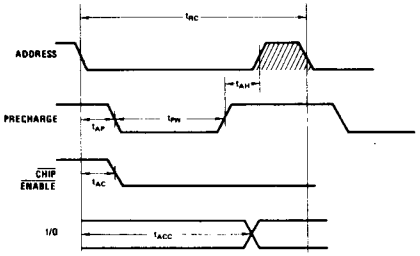
Note 4: Capacitance is guaranteed by periodic testing.

Note 5: Positive true logic notation is used:
Logic "1" = most positive voltage level
Logic "0" = most negative voltage level

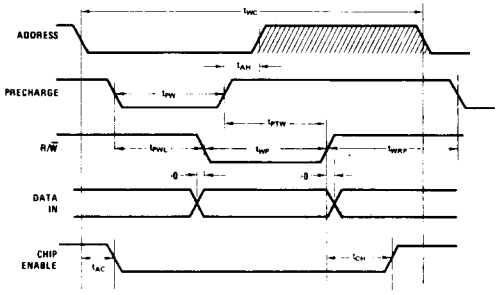
Note 6: Each of the 32 rows addressed by Address inputs A_0 through A_4 must be refreshed within the maximum interval, t_{REF}, by performing a write cycle. The row will be refreshed with $\overline{\text{Chip Enable}}$ ($\overline{CE}$) at V_{IH} or V_{IL}. Note, if $\overline{CE} = V_{IL}$ the memory cell defined by Address inputs A_0 through A_9 will be altered in accordance with information present on I/O line.

switching time waveforms

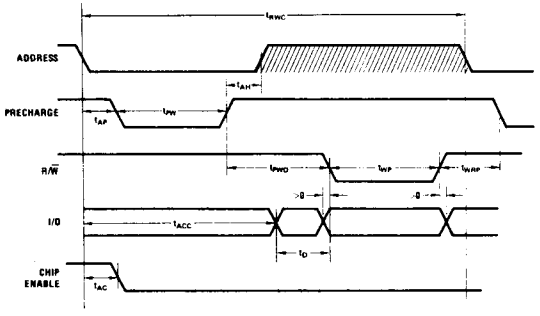
Read Cycle



Write Cycle



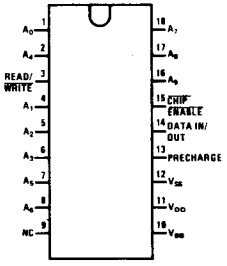
Read/Write Cycle



NOTE 1: ALL TIMING MEASUREMENTS MADE WITH 10% TO 90% t_R AND $t_F \leq 20$ ns FROM 50% POINTS.
NOTE 2: ACCESS TIME MEASURED WITH OUTPUT LOADED WITH DM8093 AND 15 pF.

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number MM4261D or MM5261D
See Package 4

Order Number MM5261N
See Package 16