# 8155H/8156H/8155H-2/8156H-2
# 2048-BIT STATIC HMOS RAM WITH I/O PORTS AND TIMER

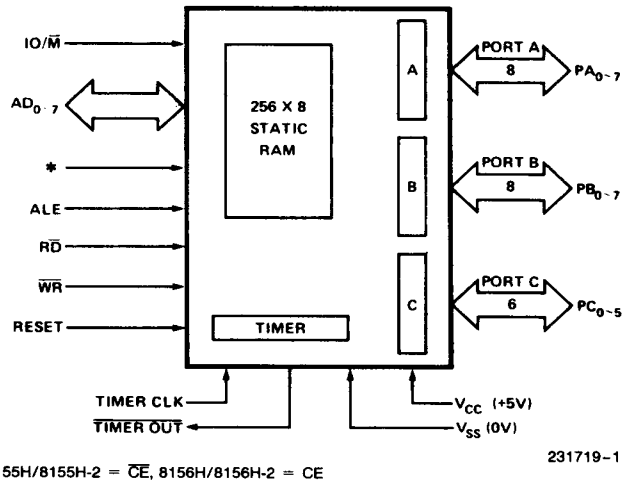
- **Single +5V Power Supply with 10% Voltage Margins**
- **30% Lower Power Consumption than the 8155 and 8156**
- **256 Word x 8 Bits**
- **Completely Static Operation**
- **Internal Address Latch**
- **2 Programmable 8-Bit I/O Ports**
- **1 Programmable 6-Bit I/O Port**
- **Programmable 14-Bit Binary Counter/ Timer**
- **Compatible with 8085AH and 8088 CPU**
- **Multiplexed Address and Data Bus**
- **Available in EXPRESS**
  - **— Standard Temperature Range**
  - **— Extended Temperature Range**

1

The Intel 8155H and 8156H are RAM and I/O chips implemented in N-Channel, depletion load, silicon gate technology (HMOS), to be used in the 8085AH and 8088 microprocessor systems. The RAM portion is designed with 2048 static cells organized as 256 x 8. They have a maximum access time of 400 ns to permit use with no wait states in 8085AH CPU. The 8155H-2 and 8156H-2 have maximum access times of 330 ns for use with the 8085H-2 and the 5 MHz 8088 CPU.

The I/O portion consists of three general purpose I/O ports. One of the three ports can be programmed to be status pins, thus allowing the other two ports to operate in handshake mode.

A 14-bit programmable counter/timer is also included on chip to provide either a square wave or terminal count pulse for the CPU system depending on timer mode.




*8155H/8155H-2 = $\overline{CE}$, 8156H/8156H-2 = CE

**Figure 1. Block Diagram**

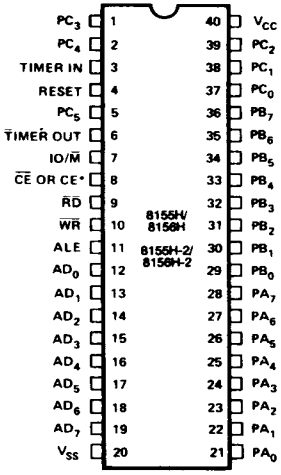



**Figure 2. Pin Configuration**

**December 1986**
**Order Number: 231719-001**

**Table 1. Pin Description**

| Symbol | Type | Name and Function |
|---|---|---|
| RESET | I | **RESET:** Pulse provided by the 8085AH to initialize the system (connect to 8085AH RESET OUT). Input high on this line resets the chip and initializes the three I/O ports to input mode. The width of RESET pulse should typically be two 8085AH clock cycle times. |
| $AD_{0-7}$ | I/O | **ADDRESS/DATA:** 3-state Address/Data lines that interface with the CPU lower 8-bit Address/Data Bus. The 8-bit address is latched into the address latch inside the 8155H/56H on the falling edge of ALE. The address can be either for the memory section or the I/O section depending on the IO/$\overline{M}$ input. The 8-bit data is either written into the chip or read from the chip, depending on the $\overline{WR}$ or $\overline{RD}$ input signal. |
| CE or $\overline{CE}$ | I | **CHIP ENABLE:** On the 8155H, this pin is $\overline{CE}$ and is ACTIVE LOW. On the 8156H, this pin is CE and is ACTIVE HIGH. |
| $\overline{RD}$ | I | **READ CONTROL:** Input low on this line with the Chip Enable active enables and $AD_{0-7}$ buffers. If IO/$\overline{M}$ pin is low, the RAM content will be read out to the AD bus. Otherwise the content of the selected I/O port or command/status registers will be read to the AD bus. |
| $\overline{WR}$ | I | **WRITE CONTROL:** Input low on this line with the Chip Enable active causes the data on the Address/Data bus to be written to the RAM or I/O ports and command/status register, depending on IO/$\overline{M}$. |
| ALE | I | **ADDRESS LATCH ENABLE:** This control signal latches both the address on the $AD_{0-7}$ lines and the state of the Chip Enable and IO/$\overline{M}$ into the chip at the falling edge of ALE. |
| IO/$\overline{M}$ | I | **I/O MEMORY:** Selects memory if low and I/O and command/status registers if high. |
| $PA_{0-7}$ (8) | I/O | **PORT A:** These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register. |
| $PB_{0-7}$ (8) | I/O | **PORT B:** These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register. |
| $PC_{0-5}$ (6) | I/O | **PORT C:** These 6 pins can function as either input port, output port, or as control signals for PA and PB. Programming is done through the command register. When $PC_{0-5}$ are used as control signals, they will provide the following:<br>$PC_0$—A INTR (Port A Interrupt)<br>$PC_1$—ABF (Port A Buffer Full)<br>$PC_2$—$\overline{A\ STB}$ (Port A Strobe)<br>$PC_3$—B INTR (Port B Interrupt)<br>$PC_4$—B BF (Port B Buffer Full)<br>$PC_5$—$\overline{B\ STB}$ (Port B Strobe) |
| TIMER IN | I | **TIMER INPUT:** Input to the timer-counter. |
| $\overline{TIMER\ OUT}$ | O | **TIMER OUTPUT:** This output can be either a square wave or a pulse, depending on the timer mode. |
| $V_{CC}$ | | **VOLTAGE:** +5V supply. |
| $V_{SS}$ | | **GROUND:** Ground reference. |

## FUNCTIONAL DESCRIPTION

The 8155H/8156H contains the following:

- 2K Bit Static RAM organized as 256 x 8
- Two 8-bit I/O ports (PA & PB) and one 6-bit I/O port (PC)
- 14-bit timer-counter

The IO/$\overline{M}$ (IO/Memory Select) pin selects either the five registers (Command, Status, $PA_{0-7}$, $PB_{0-7}$, $PC_{0-5}$) or the memory (RAM) portion.

The 8-bit address on the Address/Data lines, Chip Enable input CE or $\overline{CE}$, and IO/$\overline{M}$ are all latched on-chip at the falling edge of ALE.

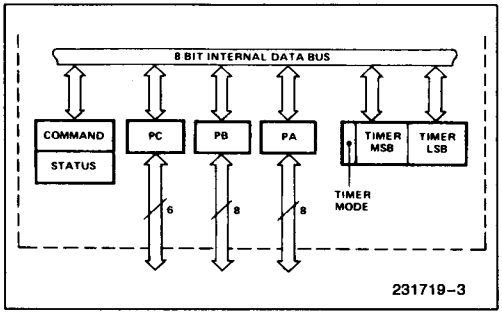
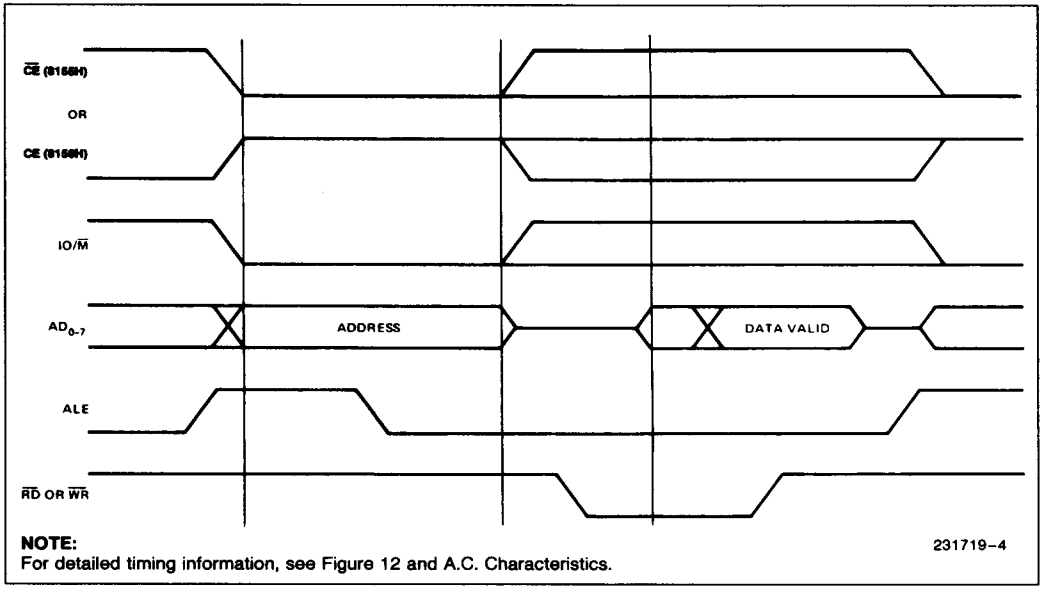



**Figure 3. 8155H/8156H Internal Registers**




**NOTE:**
For detailed timing information, see Figure 12 and A.C. Characteristics.

**Figure 4. 8155H/8156H On-Board Memory Read/Write Cycle**

## PROGRAMMING OF THE COMMAND REGISTER

The command register consists of eight latches. Four bits (0–3) define the mode of the ports, two bits (4–5) enable or disable the interrupt from port C when it acts as control port, and the last two bits (6–7) are for the timer.

The command register contents can be altered at any time by using the I/O address XXXXX000 during a WRITE operation with the Chip Enable active and IO/$\overline{M}$ = 1. The meaning of each bit of the command byte is defined in Figure 5. The contents of the command register may never be read.

## READING THE STATUS REGISTER

The status register consists of seven latches, one for each bit; six (0–5) for the status of the ports and one (6) for the status of the timer.

The status of the timer and the I/O section can be polled by reading the Status Register (Address XXXXX000). Status word format is shown in Figure 6. Note that you may never write to the status register since the command register shares the same I/O address and the command register is selected when a write to that address is issued.

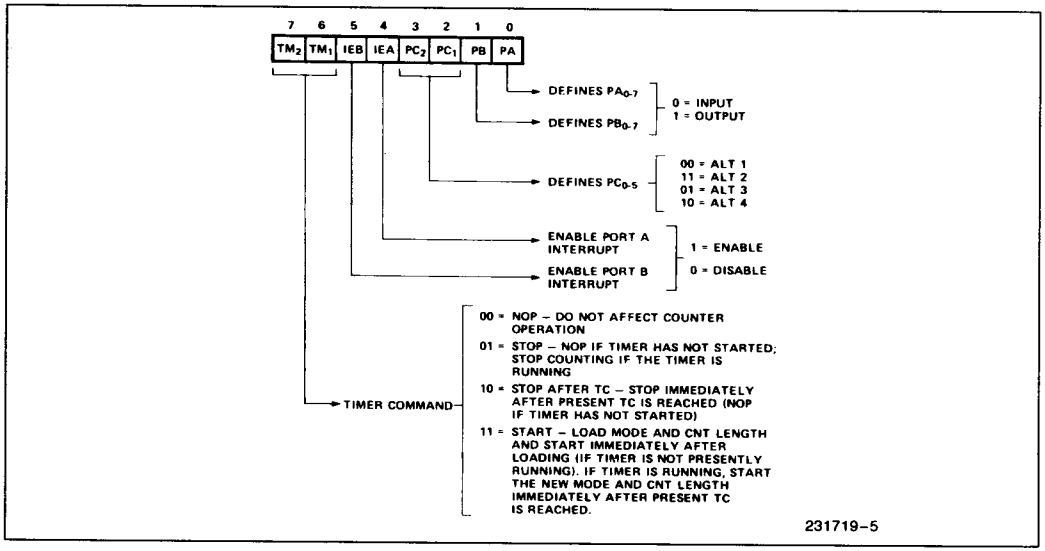



**Figure 5. Command Register Bit Assignment**

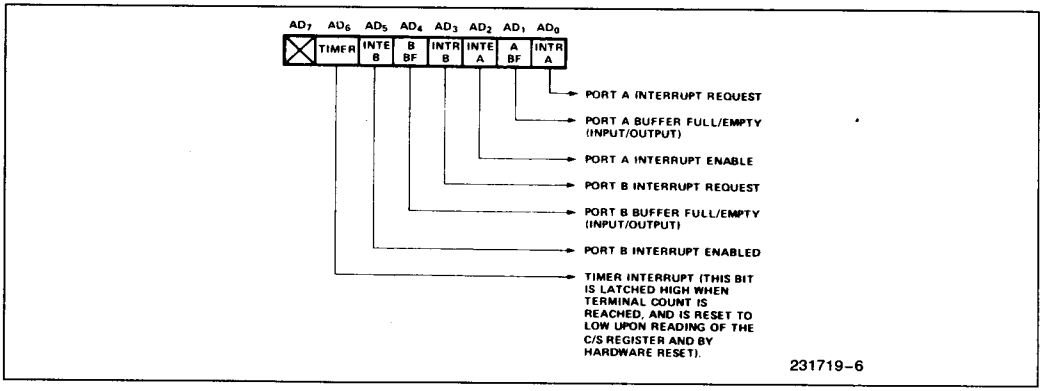



**Figure 6. Status Register Bit Assignment**

## INPUT/OUTPUT SECTION

The I/O section of the 8155H/8156H consists of five registers: (see Figure 7.)

- **Command/Status Register (C/S)**—Both registers are assigned the address XXXXX000. The C/S address serves the dual purpose.
  When the C/S registers are selected during WRITE operation, a command is written into the command register. The contents of this register are *not* accessible through the pins.
  When the C/S (XXXXX000) is selected during a READ operation, the status information of the I/O ports and the timer becomes available on the $AD_{0-7}$ lines.
- **PA Register**—This register can be programmed to be either input or output ports depending on the status of the contents of the C/S Register. Also depending on the command, this port can operate in either the basic mode or the strobed mode (see timing diagram). The I/O pins assigned in relation to this register are $PA_{0-7}$. The address of this register is XXXXX001.
- **PB Register**—This register functions the same as PA Register. The I/O pins assigned are $PB_{0-7}$. The address of this register is XXXXX010.
- **PC Register**—This register has the address XXXXX011 and contains only 6 bits. The 6 bits can be programmed to be either input ports, output ports or as control signals for PA and PB by properly programming the $AD_2$ and $AD_3$ bits of the C/S register.
  When $PC_{0-5}$ is used as a control port, 3 bits are assigned for Port A and 3 for Port B. The first bit is an interrupt that the 8155H sends out. The second is an output signal indicating whether the buffer is full or empty, and the third is an input pin to accept a strobe for the strobed input mode. (See Table 2.)

When the 'C' port is programmed to either ALT3 or ALT4, the control signals for PA and PB are initialized as follows:

| Control | Input Mode | Output Mode |
|---|---|---|
| BF | Low | Low |
| INTR | Low | High |
| STB | Input Control | Input Control |

| I/O Address† | | | | | | | | Selection |
|---|---|---|---|---|---|---|---|---|
| A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | |
| X | X | X | X | X | 0 | 0 | 0 | Interval Command/Status Register |
| X | X | X | X | X | 0 | 0 | 1 | General Purpose I/O Port A |
| X | X | X | X | X | 0 | 1 | 0 | General Purpose I/O Port B |
| X | X | X | X | X | 0 | 1 | 1 | Port C—General Purpose I/O or Control |
| X | X | X | X | X | 1 | 0 | 0 | Low-Order 8 bits of Timer Count |
| X | X | X | X | X | 1 | 0 | 1 | High 6 bits of Timer Count and 2 bits of Timer Mode |

X: Don't Care.
†: I/O Address must be qualified by CE = 1 (8156H) or $\overline{CE}$ = 0 (8155H) and IO/$\overline{M}$ = 1 in order to select the appropriate register.

**Figure 7. I/O Port and Timer Addressing Scheme**

Figure 8 shows how I/O PORTS A and B are structured within the 8155H and 8156H:

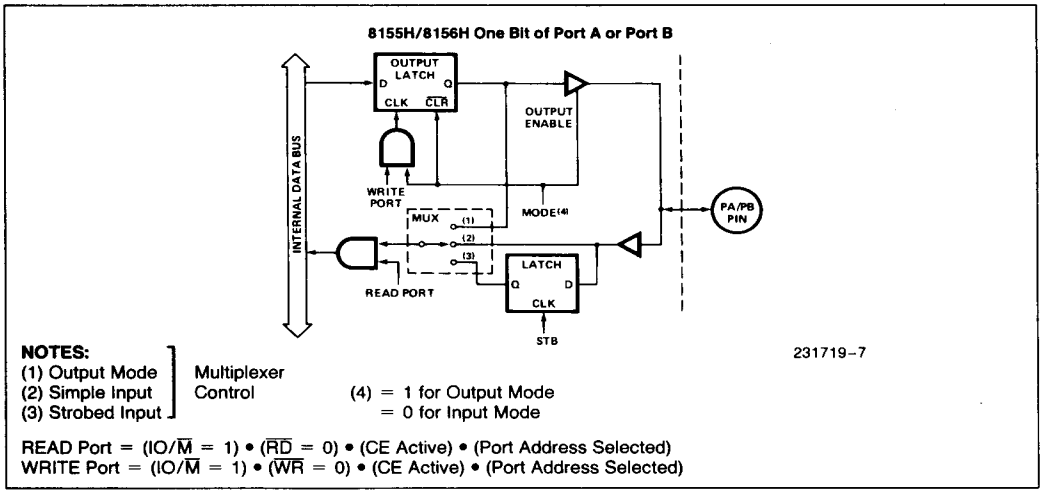



**Figure 8. 8155H/8156H Port Functions**

**Table 2. Port Control Assignment**

| Pin | ALT 1 | ALT 2 | ALT 3 | ALT 4 |
|---|---|---|---|---|
| PC0 | Input Port | Output Port | A INTR (Port A Interrupt) | A INTR (Port A Interrupt) |
| PC1 | Input Port | Output Port | A BF (Port A Buffer Full) | A BF (Port A Buffer Full) |
| PC2 | Input Port | Output Port | A $\overline{STB}$ (Port A Strobe) | A $\overline{STB}$ (Port A Strobe) |
| PC3 | Input Port | Output Port | Output Port | B INTR (Port B Interrupt) |
| PC4 | Input Port | Output Port | Output Port | B BF (Port B Buffer Full) |
| PC5 | Input Port | Output Port | Output Port | B $\overline{STB}$ (Port B Strobe) |

Note in the diagram that when the I/O ports are programmed to be output ports, the contents of the output ports can still be read by a READ operation when appropriately addressed.

The outputs of the 8155H/8156H are "glitch-free" meaning that you can write a "1" to a bit position that was previously "1" and the level at the output pin will not change.

Note also that the output latch is cleared when the port enters the input mode. The output latch cannot be loaded by writing to the port if the port is in the input mode. The result is that each time a port mode is changed from input to output, the output pin will go low. When the 8155H/56H is RESET, the output latches are all cleared and all 3 ports enter the input mode.

When in the ALT 1 or ALT 2 modes, the bits of PORT C are structured like the diagram above in the simple input or output mode, respectively.

Reading from an input port with nothing connected to the pins will provide unpredictable results.

Figure 9 shows how the 8155H/8156H I/O ports might be configured in a typical MCS®-85 system.

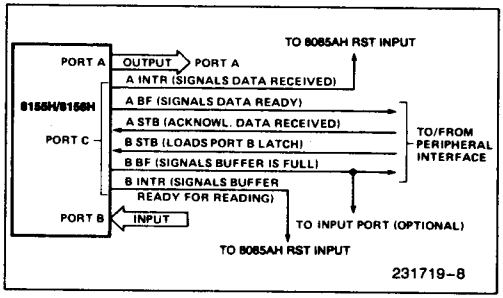



**Figure 9. Example: Command Register = 00111001**

## TIMER SECTION

The time is a 14-bit down-counter that counts the TIMER IN pulses and provides either a square wave or pulse when terminal count (TC) is reached.

The timer has the I/O address XXXXX100 for the low order byte of the register and the I/O address XXXXX101 for the high order byte of the register. (See Figure 7.)

To program the timer, the COUNT LENGTH REG is loaded first, one byte at a time, by selecting the timer addresses. Bits 0–13 of the high order count register will specify the length of the next count and bits 14–15 of the high order register will specify the timer output mode (see Figure 10). The value loaded into the count length register can have any value from 2H through 3FFFH in Bits 0–13.

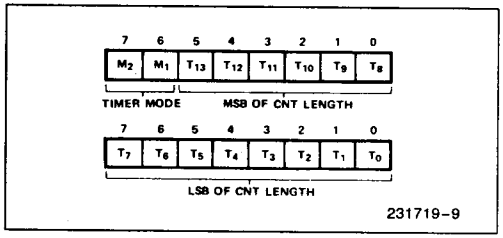



**Figure 10. Timer Format**

There are four modes to choose from: M2 and M1 define the timer mode, as shown in Figure 11.

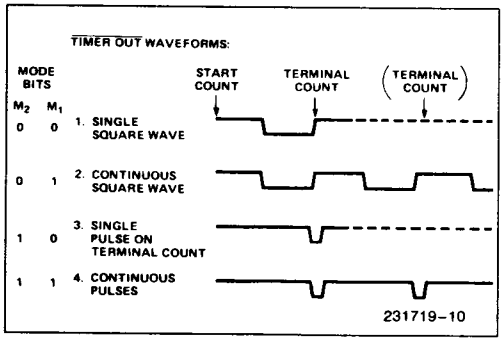


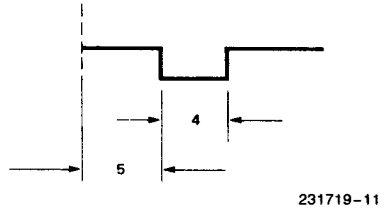

**Figure 11. Timer Modes**

Bits 6–7 ($TM_2$ and $TM_1$) of command register contents are used to start and stop the counter. There are four commands to choose from:

| $TM_2$ | $TM_1$ | |
|---|---|---|
| 0 | 0 | NOP—Do not affect counter operation. |
| 0 | 1 | STOP—NOP if timer has not started; stop counting if the timer is running. |
| 1 | 0 | STOP AFTER TC—Stop immediately after present TC is reached (NOP if timer has not started) |
| 1 | 1 | START—Load mode and CNT length and start immediately after loading (if timer is not presently running). If timer is running, start the new mode and CNT length immediately after present TC is reached. |

Note that while the counter is counting, you may load a new count and mode into the count length registers. Before the new count and mode will be used by the counter, you **must** issue a START command to the counter. This applies even though you may only want to change the count and use the previous mode.

In case of an odd-numbered count, the first half-cycle of the squarewave output, which is high, is one count longer than the second (low) half-cycle, as shown in Figure 12.




**NOTE:**
5 and 4 refer to the number of clocks in that time period.

**Figure 12. Asymmetrical Square-Wave Output Resulting from Count of 9**

The counter in the 8155H is not initialized to any particular mode or count when hardware RESET occurs, but RESET does *stop* the counting. Therefore, counting cannot begin following RESET until a START command is issued via the C/S register.

Please note that the timer circuit on the 8155H/8156H chip is designed to be a square-wave timer, not an event counter. To achieve this, it counts down by twos twice in completing one cycle. Thus, its registers do not contain values directly representing the number of TIMER IN pulses received. You cannot load an initial value of 1 into the count register and cause the timer to operate, as its terminal count value is 10 (binary) or 2 (decimal). (For the detection of single pulses, it is suggested that one of the hardware interrupt pins on the 8085AH be used.) After the timer has started counting down, the values residing in the count registers can be used to calculate the actual number of TIMER IN pulses required to complete the timer cycle if desired. To obtain the remaining count, perform the following operations in order:

1. Stop the count
2. Read in the 16-bit value from the count length registers
3. Reset the upper two mode bits
4. Reset the carry and rotate right one position all 16 bits through carry
5. If carry is set, add ½ of the full original count (½ full count—1 if full count is odd).

**NOTE:**
If you started with an odd count and you read the count length register before the third count pulse occurs, you will not be able to discern whether one or two counts has occurred. Regardless of this, the 8155H/56H always counts out the right number of pulses in generating the $\overline{\text{TIMER OUT}}$ waveforms.

## 8085AH MINIMUM SYSTEM CONFIGURATION

Figure 13a shows a minimum system using three chips, containing:

- 256 Bytes RAM
- 2K Bytes EPROM
- 38 I/O Pins
- 1 Interval Timer
- 4 Interrupt Levels

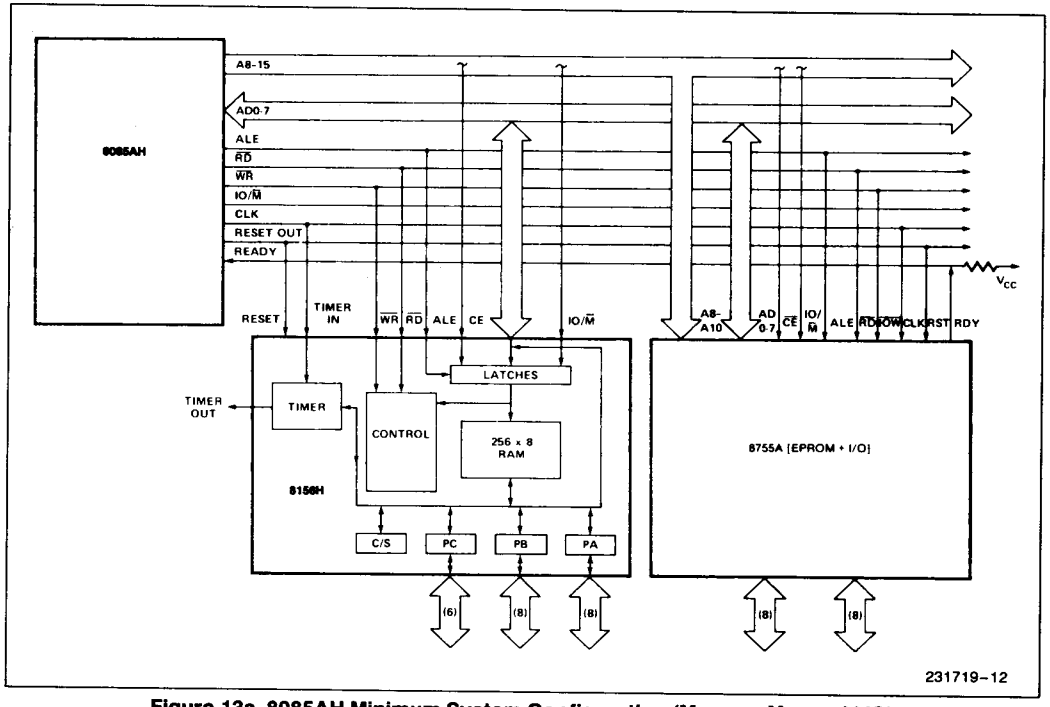



**Figure 13a. 8085AH Minimum System Configuration (Memory Mapped I/O)**

## 8088 FIVE CHIP SYSTEM

Figure 13b shows a five chip system containing:

- 1.25K Bytes RAM
- 2K Bytes EPROM
- 38 I/O Pins
- 1 Interval Timer
- 2 Interrupt Levels

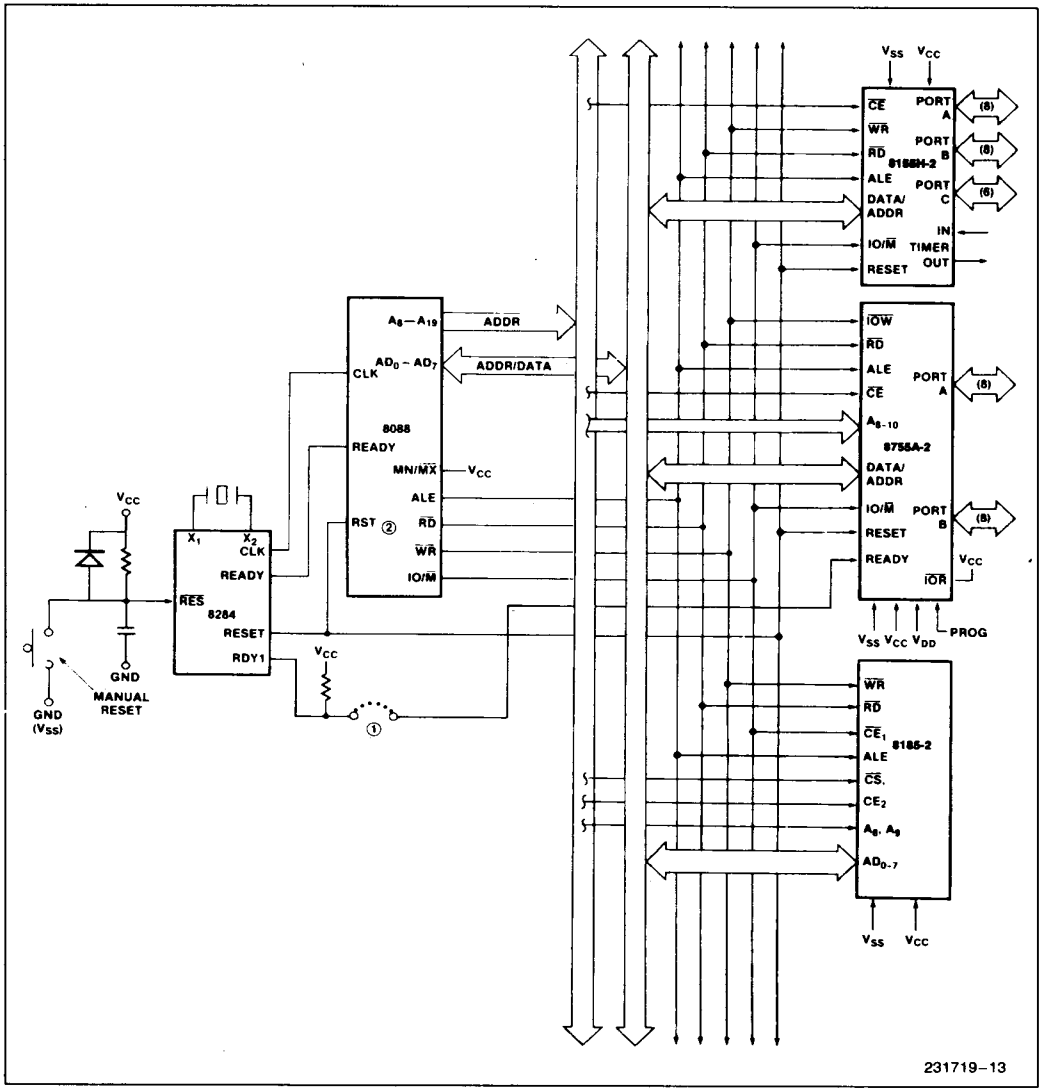



**Figure 13b. 8088 Five Chip System Configuration**

## ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....0°C to +70°C
Storage Temperature .....−65°C to +150°C
Voltage on Any Pin with Respect to Ground.....−0.5V to +7V
Power Dissipation.....1.5W

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

## D.C. CHARACTERISTICS $T_A$ = 0°C to 70°C, $V_{CC}$ = 5V ±10%

| Symbol | Parameter | Min | Max | Units | Test Conditions |
|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | −0.5 | 0.8 | V | |
| $V_{IH}$ | Input High Voltage | 2.0 | $V_{CC}$+0.5 | V | |
| $V_{OL}$ | Output Low Voltage | | 0.45 | V | $I_{OL}$ = 2 mA |
| $V_{OH}$ | Output High Voltage | 2.4 | | V | $I_{OH}$ = −400 μA |
| $I_{IL}$ | Input Leakage | | ±10 | μA | 0V ≤ $V_{IN}$ ≤ $V_{CC}$ |
| $I_{LO}$ | Output Leakage Current | | ±10 | μA | 0.45V ≤ $V_{OUT}$ ≤ $V_{CC}$ |
| $I_{CC}$ | $V_{CC}$ Supply Current | | 125 | mA | |
| $I_{IL}$ (CE) | Chip Enable Leakage<br>8155H<br>8156H | | <br>+100<br>−100 | <br>μA<br>μA | 0V ≤ $V_{IN}$ ≤ $V_{CC}$ |

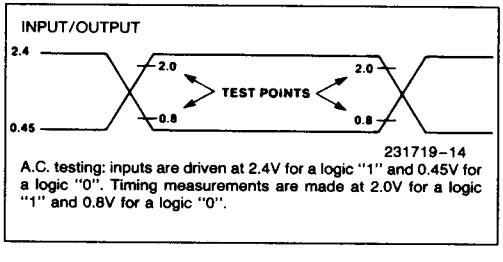
## A.C. CHARACTERISTICS $T_A$ = 0°C to 70°C, $V_{CC}$ = 5V ±10%

| Symbol | Parameter | 8155H/8156H | | 8155H-2/8156H-2 | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $t_{AL}$ | Address to Latch Setup Time | 50 | | 30 | | ns |
| $t_{LA}$ | Address Hold Time after Latch | 80 | | 30 | | ns |
| $t_{LC}$ | Latch to READ/WRITE Control | 100 | | 40 | | ns |
| $t_{RD}$ | Valid Data Out Delay from READ Control | | 170 | | 140 | ns |
| $t_{LD}$ | Latch to Data Out Valid | | 350 | | 270 | ns |
| $t_{AD}$ | Address Stable to Data Out Valid | | 400 | | 330 | ns |
| $t_{LL}$ | Latch Enable Width | 100 | | 70 | | ns |
| $t_{RDF}$ | Data Bus Float after READ | 0 | 100 | 0 | 80 | ns |
| $t_{CL}$ | READ/WRITE Control to Latch Enable | 20 | | 10 | | ns |
| $t_{CLL}$ | WRITE Control to Latch Enable for C/S Register | 125 | | 125 | | ns |
| $t_{CC}$ | READ/WRITE Control Width | 250 | | 200 | | ns |
| $t_{DW}$ | Data In to WRITE Setup Time | 150 | | 100 | | ns |
| $t_{WD}$ | Data In Hold Time after WRITE | 25 | | 25 | | ns |
| $t_{RV}$ | Recovery Time between Controls | 300 | | 200 | | ns |
| $t_{WP}$ | WRITE to Port Output | | 400 | | 300 | ns |

## A.C. CHARACTERISTICS $T_A$ = 0°C to 70°C, $V_{CC}$ = 5V ±10% (Continued)

| Symbol | Parameter | 8155H/8156H | | 8155H-2/8156H-2 | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $t_{PR}$ | Port Input Setup Time | 70 | | 50 | | ns |
| $t_{RP}$ | Port Input Hold Time | 50 | | 10 | | ns |
| $t_{SBF}$ | Strobe to Buffer Full | | 400 | | 300 | ns |
| $t_{SS}$ | Strobe Width | 200 | | 150 | | ns |
| $t_{RBE}$ | READ to Buffer Empty | | 400 | | 300 | ns |
| $t_{SI}$ | Strobe to INTR On | | 400 | | 300 | ns |
| $t_{RDI}$ | READ to INTR Off | | 400 | | 300 | ns |
| $t_{PSS}$ | Port Setup Time to Strobe | 50 | | 0 | | ns |
| $t_{PHS}$ | Port Hold Time After Strobe | 120 | | 100 | | ns |
| $t_{SBE}$ | Strobe to Buffer Empty | | 400 | | 300 | ns |
| $t_{WBF}$ | WRITE to Buffer Full | | 400 | | 300 | ns |
| $t_{WI}$ | WRITE to INTR Off | | 400 | | 300 | ns |
| $t_{TL}$ | TIMER-IN to $\overline{\text{TIMER-OUT}}$ Low | | 400 | | 300 | ns |
| $t_{TH}$ | TIMER-IN to $\overline{\text{TIMER-OUT}}$ High | | 400 | | 300 | ns |
| $t_{RDE}$ | Data Bus Enable from READ Control | 10 | | 10 | | ns |
| $t_1$ | TIMER-IN Low Time | 80 | | 40 | | ns |
| $t_2$ | TIMER-IN High Time | 120 | | 70 | | ns |
| $t_{WT}$ | WRITE to TIMER-IN (for writes which start counting) | 360 | | 200 | | ns |

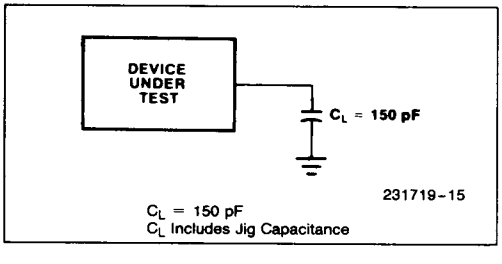
### A.C. TESTING INPUT, OUTPUT WAVEFORM




231719-14

A.C. testing: inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

### A.C. TESTING LOAD CIRCUIT

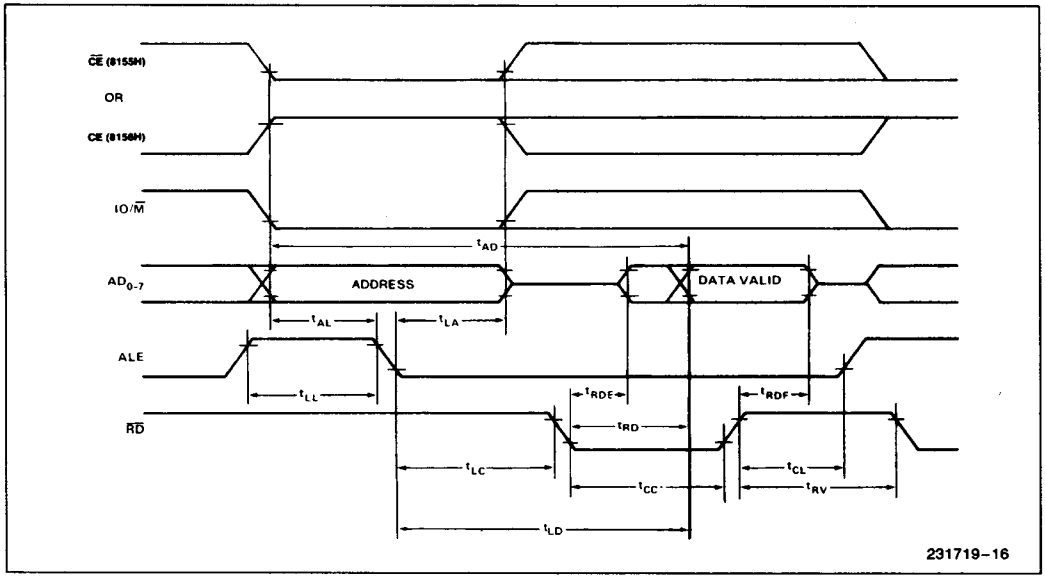



231719-15

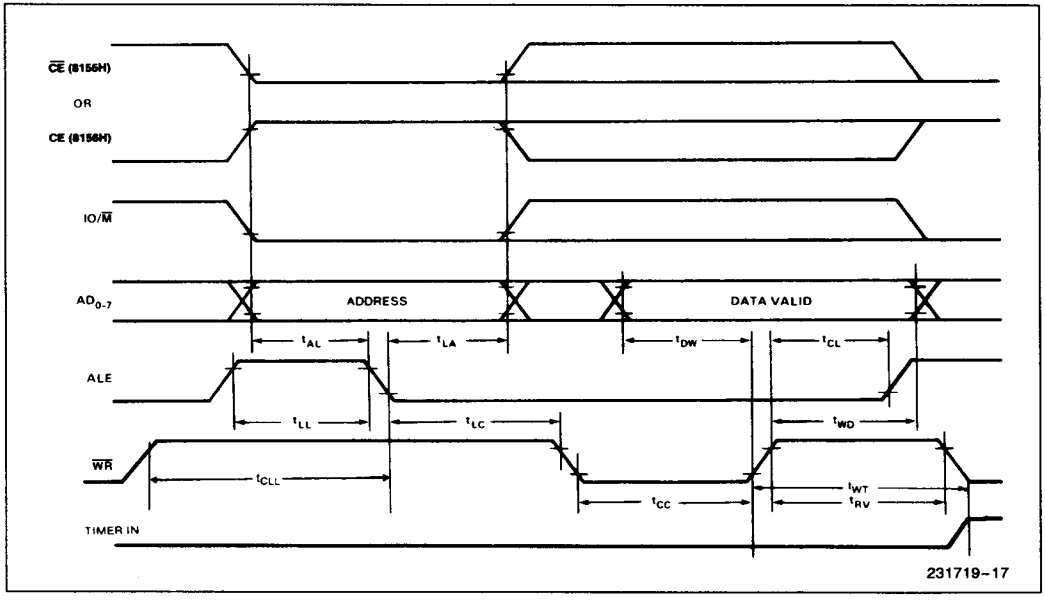
$C_L$ = 150 pF
$C_L$ Includes Jig Capacitance

## WAVEFORMS

### READ

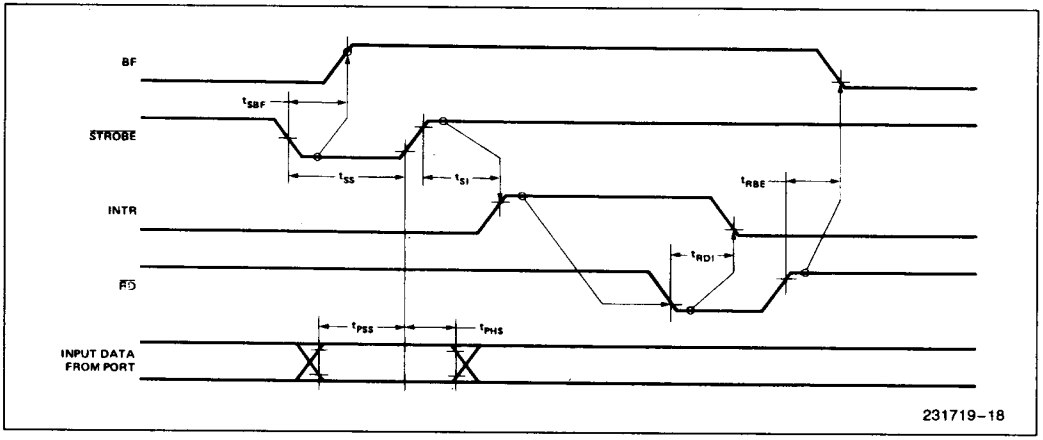



### WRITE

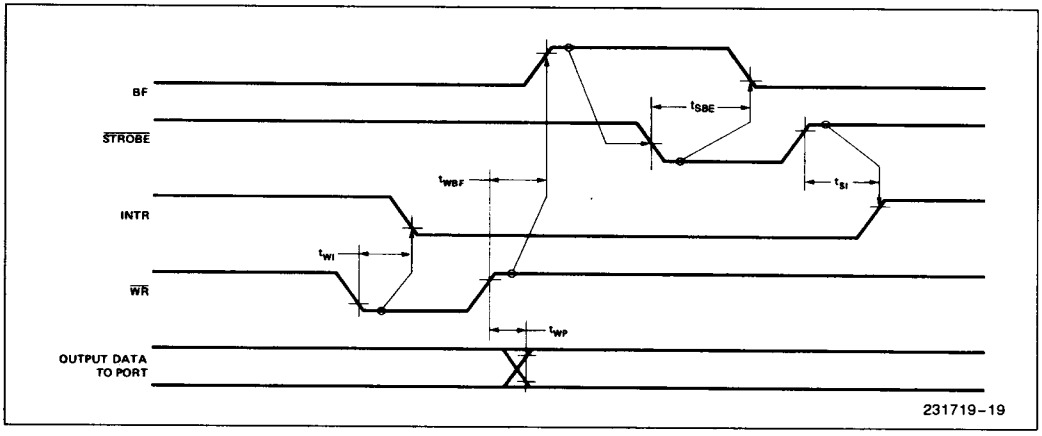


## WAVEFORMS (Continued)

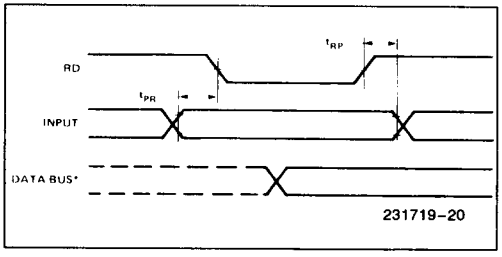
### STROBED INPUT



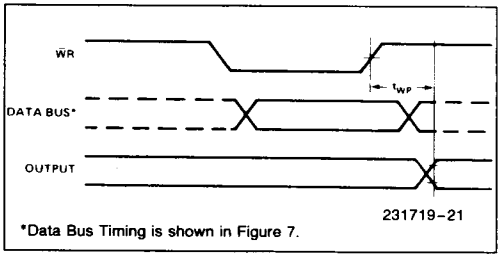

### STROBED OUTPUT




### BASIC INPUT



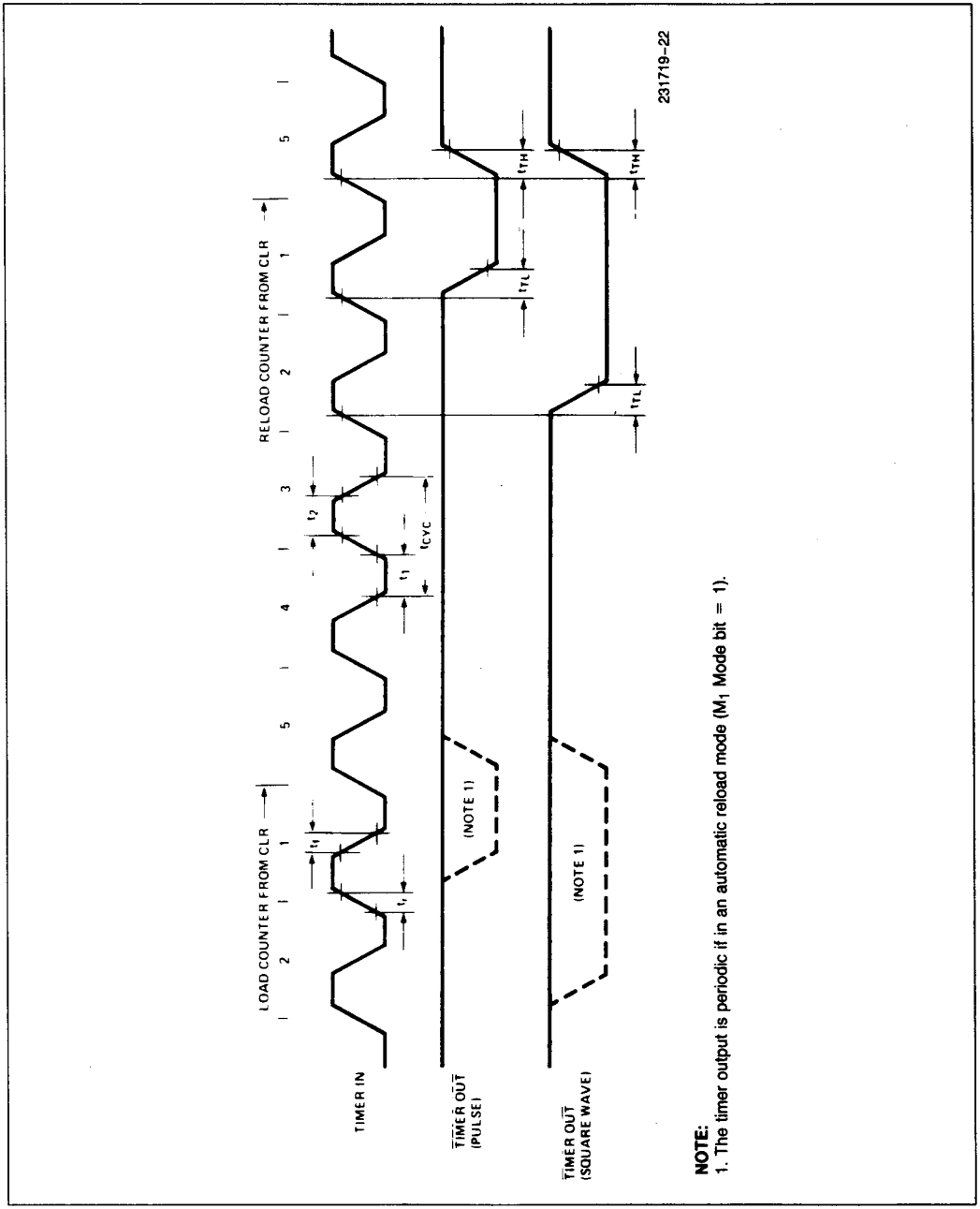

### BASIC OUTPUT




*Data Bus Timing is shown in Figure 7.

## WAVEFORMS (Continued)

### TIMER OUTPUT COUNTDOWN FROM 5 TO 1




**NOTE:**
1. The timer output is periodic if in an automatic reload mode ($M_1$ Mode bit = 1).