

## CMOS 16K-BIT STATIC RAM

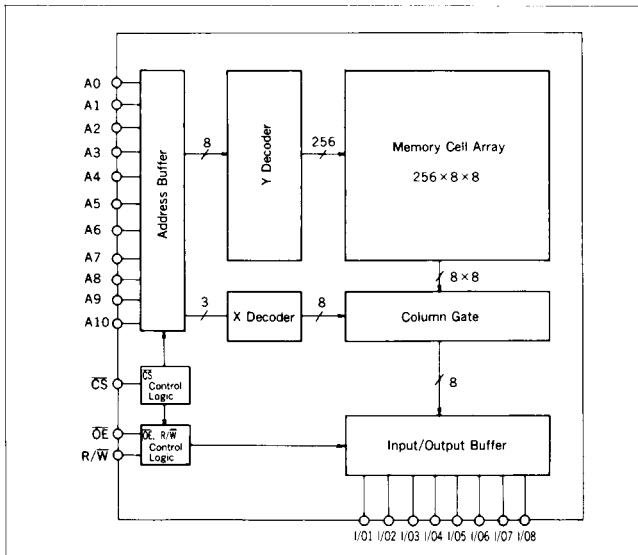
## DESCRIPTION

The SRM2016<sub>10/12</sub> is a 2,048 words x 8 bits asynchronous, static, random access memory on a monolithic CMOS chip. Its very low standby power requirement makes it ideal for applications requiring non-volatile storage with back-up batteries. The asynchronous and static nature of the memory requires no external clock or refreshing circuit. Both the input and output ports are TTL compatible and the three-state output allows easy expansion of memory capacity.

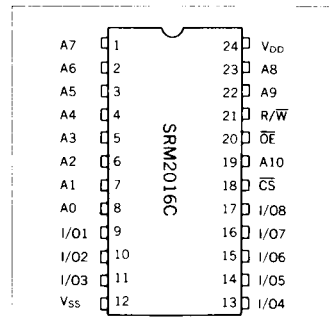
## FEATURES

- Access time ..... SRM2016<sub>10</sub> 100ns (Max)  
SRM2016<sub>12</sub> 120ns (Max)
- Low supply current .... Standby : 1 $\mu$ A (Typ)  
Operation: SRM2016<sub>10</sub> 30mA (Typ)  
SRM2016<sub>12</sub> 25mA (Typ)
- Completely static operation
- Single power supply .. 5V  $\pm$  10%
- TTL compatible inputs and outputs
- 3-state output with wired-OR capability
- Non-volatile storage with back-up batteries
- Package ..... SRM2016C<sub>10/12</sub> 24-pin DIP (plastic)  
SRM2016M<sub>10/12</sub> 24-pin SOP (plastic)  
SRM2016N<sub>10/12</sub> 24-pin Skinny DIP (plastic)

## BLOCK DIAGRAM



## PIN CONFIGURATION



## PIN DESCRIPTION

A0 to A10	Address Input
R/ $\bar{W}$	Read/Write
$\bar{O}E$	Output Enable
$\bar{C}S$	Chip Select
I/O1 to 8	Data Input/Output
V <sub>DD</sub>	Power Supply (+5V)
V <sub>SS</sub>	Power Supply (0V)

### ■ ABSOLUTE MAXIMUM RATINGS

(V<sub>SS</sub> = 0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V <sub>DD</sub>	-0.5 to 7.0	V
Input voltage*	V <sub>I</sub>	-0.5 to 7.0	V
Input/output voltage*	V <sub>I/O</sub>	-0.5 to V <sub>DD</sub> +0.3	V
Power dissipation	P <sub>D</sub>	1.0	W
Operating temperature	T <sub>opr</sub>	0 to 70	°C
Storage temperature	T <sub>stg</sub>	-65 to 150	°C
Soldering temp. & time	T <sub>sol</sub>	260°C, 10s (at lead)	—

\*V<sub>I</sub>, V<sub>I/O</sub> = -1.0V when pulse width is 50 ns

### ■ RECOMMENDED OPERATING CONDITIONS

(T<sub>a</sub> = 0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V <sub>DD</sub>		4.5	5.0	5.5	V
	V <sub>SS</sub>		0	0	0	V
Input voltage	V <sub>IH</sub>		2.2	3.5	V <sub>DD</sub> +0.3	V
	V <sub>IL</sub>		-0.3*	—	0.8	V

\*V<sub>IL</sub>(Min) = -1.0V when pulse width is 50ns

### ■ ELECTRICAL CHARACTERISTICS

#### ● DC Electrical Characteristics

(V<sub>DD</sub> = 5V ± 10%, V<sub>SS</sub> = 0V, T<sub>a</sub> = 0 to 70°C)

Parameter	Symbol	Conditions	SRM2016 <sub>10</sub>			SRM2016 <sub>12</sub>			Unit
			Min	Typ*	Max	Min	Typ*	Max	
Input leakage current	I <sub>LI</sub>	V <sub>DD</sub> = 5.5V, V <sub>I</sub> = 0 to V <sub>DD</sub>	-1	—	1	-1	—	1	μA
Output leakage current	I <sub>LO</sub>	CS = V <sub>IH</sub> , or OE = V <sub>IH</sub> , V <sub>I/O</sub> = 0 to V <sub>DD</sub>	-1	—	1	-1	—	1	μA
Operating supply current	I <sub>DD0</sub>	CS = V <sub>IL</sub> , I <sub>I/O</sub> = 0mA	—	30	60	—	25	50	mA
	I <sub>DD01</sub>	V <sub>IH</sub> = 3.5V, V <sub>IL</sub> = 0.6V, I <sub>I/O</sub> = 0mA	—	16	—	—	16	—	mA
Average operating current	I <sub>DDA</sub>	Min. cycle, duty = 100%, I <sub>I/O</sub> = 0mA	—	30	60	—	25	50	mA
Standby supply current	I <sub>DDS</sub>	CS = V <sub>IH</sub>	—	1.5	3.0	—	1.5	3.0	mA
	I <sub>DDS1</sub>	CS = V <sub>DD</sub> - 0.2V	—	1	50	—	1	50	μA
Output voltage	V <sub>OL</sub>	I <sub>OL</sub> = 4.0mA	—	—	0.4	—	—	0.4	V
	V <sub>OH</sub>	I <sub>OH</sub> = -1.0mA	2.4	—	—	2.4	—	—	V

\* Typical values are for reference, with V<sub>DD</sub> = 5V and T<sub>a</sub> = 25°C assumed

#### ● Terminal Capacitance

(f = 1MHz, T<sub>a</sub> = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C <sub>I</sub>	V <sub>I</sub> = 0V	—	4	6	pF
I/O capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> = 0V	—	6	8	pF

#### ● AC Electrical Characteristics

##### ○ Read Cycle

(V<sub>DD</sub> = 5V ± 10%, V<sub>SS</sub> = 0V, T<sub>a</sub> = 0 to 70°C)

Parameter	Symbol	Conditions	SRM2016 <sub>10</sub>		SRM2016 <sub>12</sub>		Unit
			Min	Max	Min	Max	
Read cycle time	t <sub>RC</sub>		100	—	120	—	ns
Address access time	t <sub>ACC</sub>	*1	—	100	—	120	ns
CS access time	t <sub>ACS</sub>		—	100	—	120	ns
CS output setup time	t <sub>CLZ</sub>	*2	10	—	10	—	ns
OE access time	t <sub>OE</sub>	*1	—	55	—	60	ns
OE output setup time	t <sub>OLZ</sub>		5	—	10	—	ns
CS output floating	t <sub>CHZ</sub>	*2	0	40	0	40	ns
OE output floating	t <sub>OHZ</sub>		0	40	0	40	ns
Output hold time	t <sub>OH</sub>	*1	10	—	10	—	ns

○ Write Cycle

( $V_{DD}=5V \pm 10\%$ ,  $V_{SS}=0V$ ,  $T_a=0$  to  $70^\circ C$ )

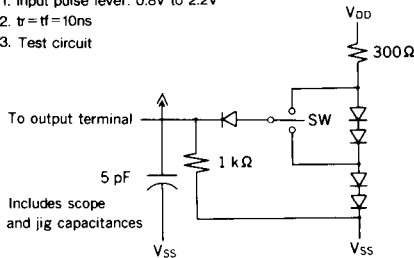
Parameter	Symbol	Conditions	SRM201610		SRM201612		Unit
			Min	Max	Min	Max	
Write cycle time	$t_{WC}$	*1	100	—	120	—	ns
Chip select time (CS)	$t_{CW}$		80	—	85	—	ns
Address enable time	$t_{AW}$		80	—	85	—	ns
Address setup time	$t_{AS}$		0	—	0	—	ns
Write pulse width	$t_{WP}$		65	—	70	—	ns
$\overline{OE}$ output floating	$t_{OHZ}$	*2	0	40	0	40	ns
R/ $\overline{W}$ output floating	$t_{WHZ}$	*3	0	45	0	50	ns
Input data setup time	$t_{DW}$	*1	45	—	50	—	ns
Address hold time	$t_{WR}$		5	—	5	—	ns
Input data hold time	$t_{DH}$		0	—	0	—	ns
R/ $\overline{W}$ output setup time	$t_{OW}$	*3	5	—	10	—	ns

\*1 Test conditions.

1. Input pulse level: 0.8V to 2.2V
2.  $t_r = t_f = 10ns$
3. Input/output timing reference level: 1.5V
4. Output load:  $I_{TL} + C_L = 100pF$

\*3 Test conditions.

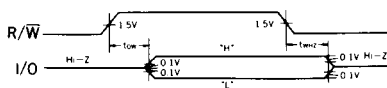
1. Input pulse level: 0.8V to 2.2V
2.  $t_r = t_f = 10ns$
3. Test circuit



○ SW is set to the  $V_{DD}$  side when measuring Hi-z-high and high-Hi-z of  $t_{OW}$  or  $t_{WHZ}$ .

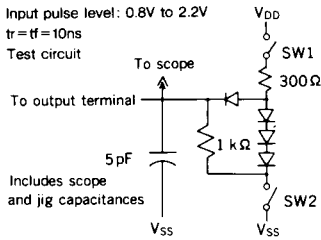
○ SW is set to the  $V_{SS}$  side when measuring Hi-z-low and low-Hi-z of  $t_{OW}$  or  $t_{WHZ}$ .

Output turn-on turn-off times



\*2 Test conditions.

1. Input pulse level: 0.8V to 2.2V
2.  $t_r = t_f = 10ns$
3. Test circuit

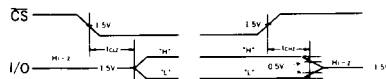
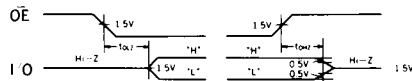


○ Both SW1 and SW2 are closed when measuring  $t_{OHZ}$  or  $t_{WHZ}$ .

○ SW1 is open and SW2 is closed when measuring Hi-z-high of  $t_{OZ}$  or  $t_{WZ}$ .

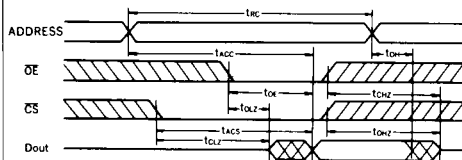
○ SW1 is closed and SW2 is open when measuring Hi-z-low of  $t_{OZ}$  or  $t_{WZ}$ .

Output turn-on turn-off times

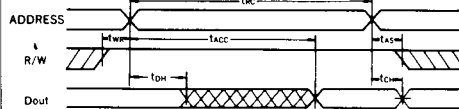


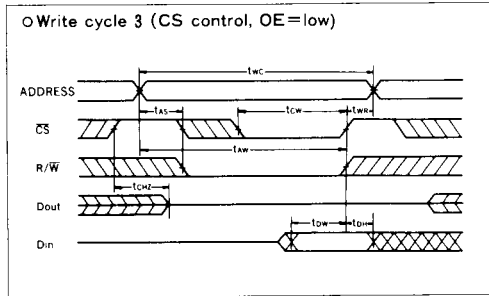
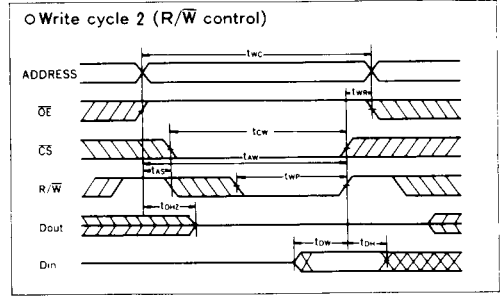
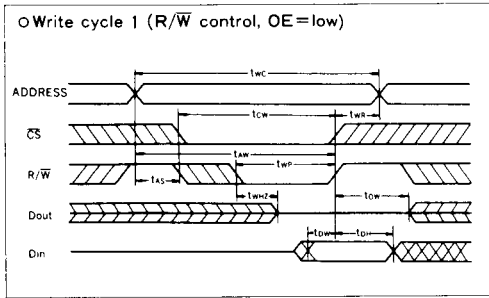
● Timing Chart

○ Read cycle 1 ( $\overline{OE}$ ,  $\overline{CS}$  control, R/ $\overline{W}$ =high)



○ Read cycle 2 (R/ $\overline{W}$  control,  $\overline{OE}$ =low,  $\overline{CS}$ =low)





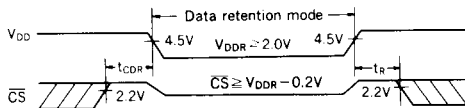
DATA RETENTION CHARACTERISTICS WITH LOW VOLTAGE POWER SUPPLY

( $T_a = 0$  to  $70^\circ\text{C}$ )

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	$V_{DDR}$	$\overline{CS} \geq V_{DDR} - 0.2\text{V}$	2.0	—	5.5	V
Data retention current	$I_{DDR}$	$V_{DD} = 3.0\text{V}$ , $\overline{CS} \geq 2.8\text{V}$	—	—	25	$\mu\text{A}$
Chip select data hold time	$t_{CDR}$	Refer to the figure below.	0	—	—	ns
Operation recovery time	$t_R$		$t_{RC}^*$	—	—	ns

\*  $t_{RC}$  : read cycle time

Data retention timing



Note: When retaining data in standby mode, supply voltage can be lowered within a certain range. Read or write cycle cannot be performed while the supply voltage is low.

FUNCTIONS

Truth Table

$\overline{CS}$	OE	R/W	A0 to A10	DATA I/O	Mode	$I_{DD}$
H	—	—	—	Hi-Z	Unselected	$I_{DDS}$ , $I_{DDSI}$
L	L	H	Stable	Output data	Read	$I_{DDO}$
L	H	L	Stable	Input data	Write	$I_{DDO}$
L	L	L	Stable	Input data	Write	$I_{DDO}$

X: "H" or "L" —: "H", "L" or "Hi"

Reading Data

Data can be read out if an address is set while  $\overline{CS}$  and  $\overline{OE}$  are held low, and  $\overline{R/W}$  is held high.

### ● Writing Data

There are the following three ways of writing data into the memory.

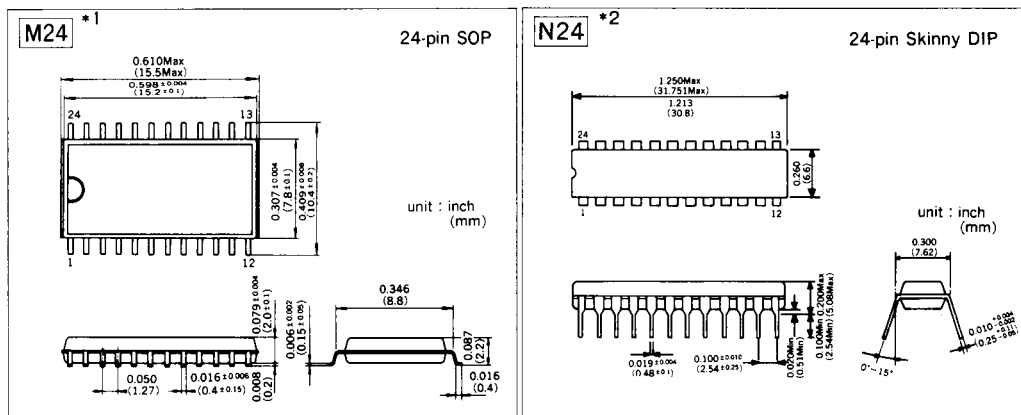
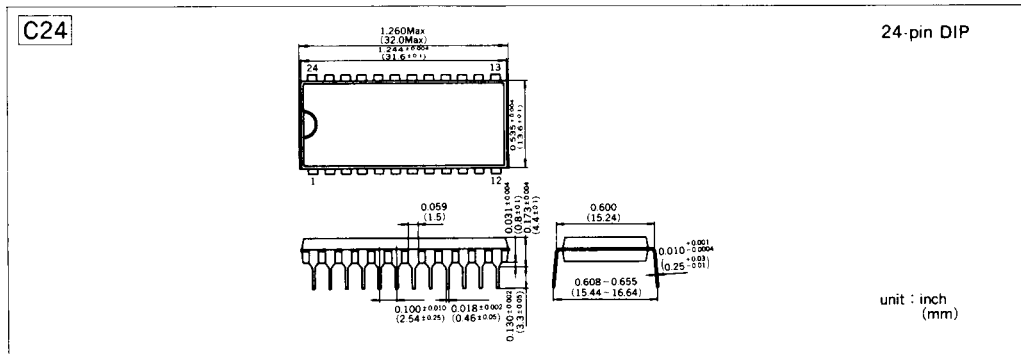
- (1) Hold  $\overline{CS}$  low, set the address, and apply a low pulse to  $R/\overline{W}$ .
- (2) Hold  $R/\overline{W}$  low, set the address, and apply a low pulse to  $\overline{CS}$ .
- (3) Set the address, then apply low pulses to both  $\overline{CS}$  and  $R/\overline{W}$ .

In each case, data from the DATA I/O terminal is fetched into the SRM201610/12 at the last transition of a section in which both  $\overline{CS}$  and  $R/\overline{W}$  are low. Because the DATA I/O terminal is in high-impedance state when  $\overline{CS}$  or  $\overline{OE}$  is high, or  $R/\overline{W}$  is low, contention of the data driver on the bus and memory output is avoided.

### ● Standby Mode

When  $\overline{CS}$  is high, SRM201610/12 is in the stand-by mode and only retains the data. At this time the DATA I/O terminal is in high-impedance state, and input of an address,  $R/\overline{W}$  signal, or data is prohibited. When  $\overline{CS}$  is above  $V_{DD}-0.2V$ , current flowing within the SRM201610/12 chip is only that in the high-resistance portion of the memory cells and leakage current.

### ■ PACKAGE DIMENSIONS



\* 1 Represents model SRM2016M10/12 that has the same electrical characteristics as model SRM2016C10/12.

\* 2 Represents model SRM2016N10/12 that has the same electrical characteristics as model SRM2016C10/12.

### CHARACTERISTICS CURVES

