

## Document Title

128Kx8 bit Low Power CMOS Static RAM

## Revision History

<u>Revision No.</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>
0.0	Initial draft	July 15, 2002	Preliminary
0.1	Revised - Deleted 32-TSOP1-0820R Package Type. - Added Commercial product.	December 4, 2002	Preliminary
0.2	Revised - Added Lead Free 32-SOP-525 Product	May 13, 2003	Preliminary
0.3	Revised - Added Lead Free 32-TSOP1-0820F Product	June 21, 2003	Preliminary
1.0	Finalized - Changed Icc from 10mA to 5mA - Changed Icc2 from 35mA to 25mA - Changed Isb from 3mA to 0.4mA - Changed IDR(industrial) from 15μA to 10μA - Changed IDR(Automotive) from 25μA to 20μA	September 16, 2003	Final

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## PRODUCT LIST

Commercial Products(0~70°C)		Industrial Products(-40~85°C)		Automotive Products(-40~125°C)	
Part Name	Function	Part Name	Function	Part Name	Function
K6X1008C2D-DB55	32-DIP, 55ns, LL	K6X1008C2D-DF55	32-DIP, 55ns, LL	K6X1008C2D-GQ55	32-SOP, 55ns, L
K6X1008C2D-DB70	32-DIP, 70ns, LL	K6X1008C2D-DF70	32-DIP, 70ns, LL	K6X1008C2D-GQ70	32-SOP, 70ns, L
K6X1008C2D-GB55	32-SOP, 55ns, LL	K6X1008C2D-GF55	32-SOP, 55ns, LL	K6X1008C2D-TQ55	32-TSOP-F, 55ns, L
K6X1008C2D-GB70	32-SOP, 70ns, LL	K6X1008C2D-GF70	32-SOP, 70ns, LL	K6X1008C2D-TQ70	32-TSOP-F, 70ns, L
K6X1008C2D-BB55 <sup>1)</sup>	32-SOP, 55ns, LL	K6X1008C2D-BF55 <sup>1)</sup>	32-SOP, 55ns, LL		
K6X1008C2D-BB70 <sup>1)</sup>	32-SOP, 70ns, LL	K6X1008C2D-BF70 <sup>1)</sup>	32-SOP, 70ns, LL		
K6X1008C2D-TB55	32-TSOP-F, 55ns, LL	K6X1008C2D-TF55	32-TSOP-F, 55ns, LL		
K6X1008C2D-TB70	32-TSOP-F, 70ns, LL	K6X1008C2D-TF70	32-TSOP-F, 70ns, LL		
K6X1008C2D-PB55 <sup>1)</sup>	32-TSOP-F, 55ns, LL	K6X1008C2D-PF55 <sup>1)</sup>	32-TSOP-F, 55ns, LL		
K6X1008C2D-PB70 <sup>1)</sup>	32-TSOP-F, 70ns, LL	K6X1008C2D-PF70 <sup>1)</sup>	32-TSOP-F, 70ns, LL		

1. Lead Free Product

## FUNCTIONAL DESCRIPTION

$\overline{CS}_1$	$CS_2$	$\overline{OE}$	$\overline{WE}$	I/O	Mode	Power
H	X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	Deselected	Standby
X <sup>1)</sup>	L	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	Deselected	Standby
L	H	H	H	High-Z	Output Disabled	Active
L	H	L	H	Dout	Read	Active
L	H	X <sup>1)</sup>	L	Din	Write	Active

1. X means don't care (Must be in high or low states)

## ABSOLUTE MAXIMUM RATINGS<sup>1)</sup>

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-0.5 to V <sub>CC</sub> +0.5V(Max. 7.0V)	V	-
Voltage on Vcc supply relative to Vss	V <sub>CC</sub>	-0.3 to 7.0	V	-
Power Dissipation	P <sub>D</sub>	1.0	W	-
Storage temperature	T <sub>STG</sub>	-65 to 150	°C	-
Operating Temperature	T <sub>A</sub>	0 to 70	°C	K6X1008C2D-B
		-40 to 85	°C	K6X1008C2D-F
		-40 to 125	°C	K6X1008C2D-Q

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS<sup>1)</sup>

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
Ground	V <sub>SS</sub>	0	0	0	V
Input high voltage	V <sub>IH</sub>	2.2	-	V <sub>CC</sub> +0.5 <sup>2)</sup>	V
Input low voltage	V <sub>IL</sub>	-0.5 <sup>3)</sup>	-	0.8	V

Note:

- Commercial Product: T<sub>A</sub>=0 to 70°C, Otherwise specified  
Industrial Product: T<sub>A</sub>=-40 to 85°C, Otherwise specified  
Automotive Product: T<sub>A</sub>=-40 to 125°C, Otherwise specified
- Overshoot: V<sub>CC</sub>+3.0V in case of pulse width≤30ns.
- Undershoot: -3.0V in case of pulse width≤30ns.
- Overshoot and undershoot are sampled, not 100% tested.

## CAPACITANCE<sup>1)</sup> (f=1MHz, T<sub>A</sub>=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	8	pF
Input/Output capacitance	C <sub>IO</sub>	V <sub>IO</sub> =0V	-	10	pF

- Capacitance is sampled, not 100% tested

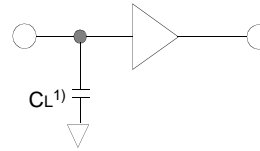
## DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA	
Output leakage current	I <sub>LO</sub>	$\overline{CS}_1=V_{IH}$ or $CS_2=V_{IL}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ , V <sub>IO</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA	
Operating power supply current	I <sub>CC</sub>	I <sub>IO</sub> =0mA, $\overline{CS}_1=V_{IL}$ , CS <sub>2</sub> =V <sub>IH</sub> , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , Read	-	-	5	mA	
Average operating current	I <sub>CC1</sub>	Cycle time=1μs, 100%duty, I <sub>IO</sub> =0mA, $\overline{CS}_1\leq 0.2V$ , CS <sub>2</sub> ≥V <sub>CC</sub> -0.2V, V <sub>IN</sub> ≤0.2V or V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V	-	-	7	mA	
	I <sub>CC2</sub>	Cycle time=Min, 100% duty, I <sub>IO</sub> =0mA, $\overline{CS}_1=V_{IL}$ , CS <sub>2</sub> =V <sub>IH</sub> , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>	-	-	25	mA	
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> =2.1mA	-	-	0.4	V	
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> =-1.0mA	2.4	-	-	V	
Standby Current(TTL)	I <sub>SB</sub>	$\overline{CS}_1=V_{IH}$ , CS <sub>2</sub> =V <sub>IL</sub> , Other inputs=V <sub>IH</sub> or V <sub>IL</sub>	-	-	0.4	mA	
Standby Current(CMOS)	I <sub>SB1</sub>	$\overline{CS}_1\geq V_{CC}-0.2V$ , CS <sub>2</sub> ≥V <sub>CC</sub> -0.2V or CS <sub>2</sub> ≤0.2V, Other inputs=0~V <sub>CC</sub>	K6X1008C2D-B	-	-	10	μA
			K6X1008C2D-F	-	-	15	μA
			K6X1008C2D-Q	-	-	25	μA

## AC OPERATING CONDITIONS

### TEST CONDITIONS (Test Load and Input/Output Reference)

Input pulse level: 0.8 to 2.4V  
 Input rising and falling time: 5ns  
 Input and output reference voltage: 1.5V  
 Output load(see right):  $C_L=100\text{pF}+1\text{TTL}$   
 $C_L=50\text{pF}+1\text{TTL}$



1. Including scope and jig capacitance

## AC CHARACTERISTICS

( $V_{CC}=4.5\sim 5.5\text{V}$ , Commercial product:  $T_A=0$  to  $70^\circ\text{C}$ , Industrial product:  $T_A=-40$  to  $85^\circ\text{C}$ , Automotive product:  $T_A=-40\sim 125^\circ\text{C}$ )

Parameter List		Symbol	Speed Bins				Units
			55ns		70ns		
			Min	Max	Min	Max	
Read	Read Cycle Time	trc	55	-	70	-	ns
	Address Access Time	tAA	-	55	-	70	ns
	Chip Select to Output	tCO	-	55	-	70	ns
	Output Enable to Valid Output	tOE	-	25	-	35	ns
	Chip Select to Low-Z Output	tLZ	10	-	10	-	ns
	Output Enable to Low-Z Output	tOLZ	5	-	5	-	ns
	Chip Disable to High-Z Output	tHZ	0	20	0	25	ns
	Output Disable to High-Z Output	tOHZ	0	20	0	25	ns
	Output Hold from Address Change	tOH	10	-	10	-	ns
Write	Write Cycle Time	tWC	55	-	70	-	ns
	Chip Select to End of Write	tCW	45	-	60	-	ns
	Address Set-up Time	tAS	0	-	0	-	ns
	Address Valid to End of Write	tAW	45	-	60	-	ns
	Write Pulse Width	tWP	40	-	50	-	ns
	Write Recovery Time	tWR	0	-	0	-	ns
	Write to Output High-Z	tWHZ	0	20	0	25	ns
	Data to Write Time Overlap	tDW	20	-	25	-	ns
	Data Hold from Write Time	tDH	0	-	0	-	ns
	End Write to Output Low-Z	tOW	5	-	5	-	ns

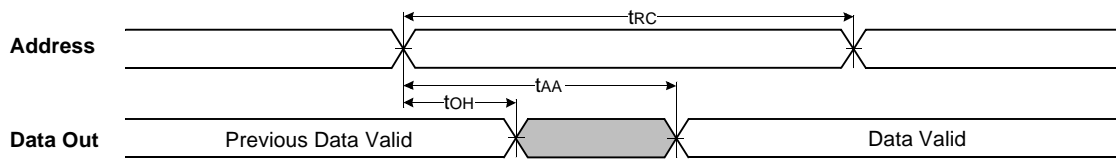
## DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ	Max	Unit	
Vcc for data retention	VDR	$\overline{CS}_1 \geq V_{CC}-0.2\text{V}^{(1)}$	2.0	-	5.5	V	
Data retention current	IDR	$V_{CC}=3.0\text{V}$ , $\overline{CS}_1 \geq V_{CC}-0.2\text{V}^{(1)}$	K6X1008C2D-B	-	-	10	$\mu\text{A}$
			K6X1008C2D-F	-	-	10	$\mu\text{A}$
			K6X1008C2D-Q	-	-	20	$\mu\text{A}$
Data retention set-up time	tSDR	See data retention waveform	0	-	-	ms	
Recovery time	trDR		5	-	-		

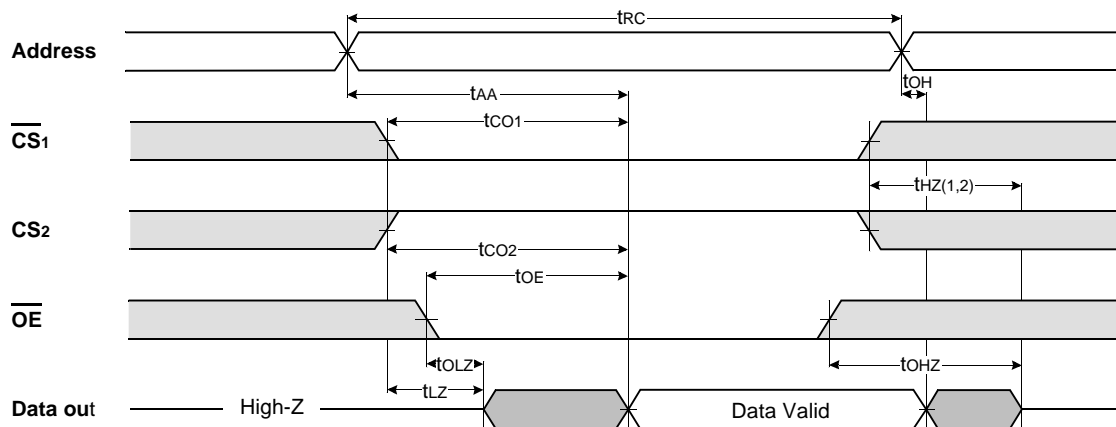
1.  $\overline{CS}_1 \geq V_{CC}-0.2\text{V}$ ,  $\overline{CS}_2 \geq V_{CC}-0.2\text{V}$ , or  $\overline{CS}_2 \leq 0.2\text{V}$

## TIMING DIAGRAMS

**TIMING WAVEFORM OF READ CYCLE(1)** (Address Controlled,  $\overline{CS1}=\overline{OE}=V_{IL}$ ,  $CS2=\overline{WE}=V_{IH}$ )



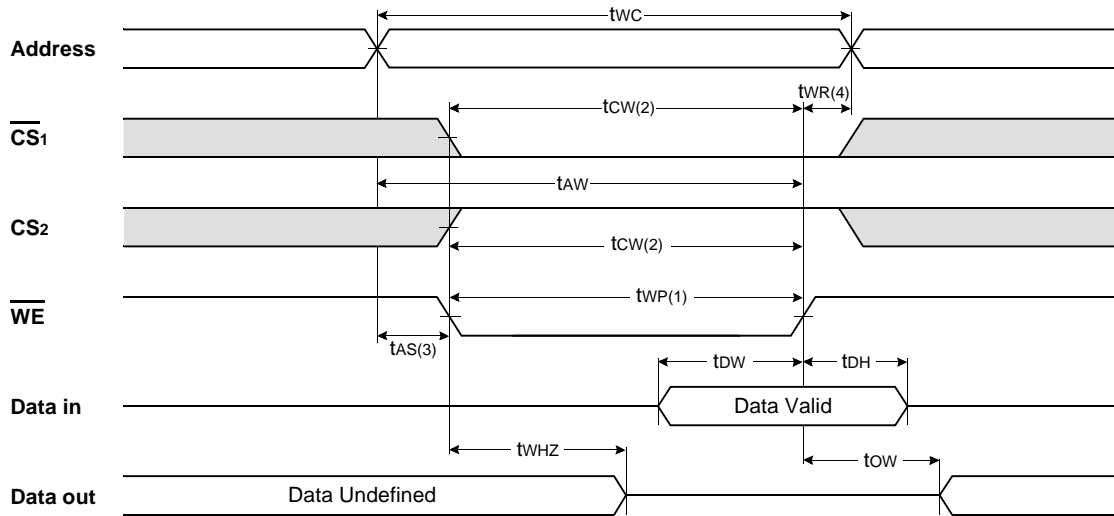
**TIMING WAVEFORM OF READ CYCLE(2)** ( $\overline{WE}=V_{IH}$ )



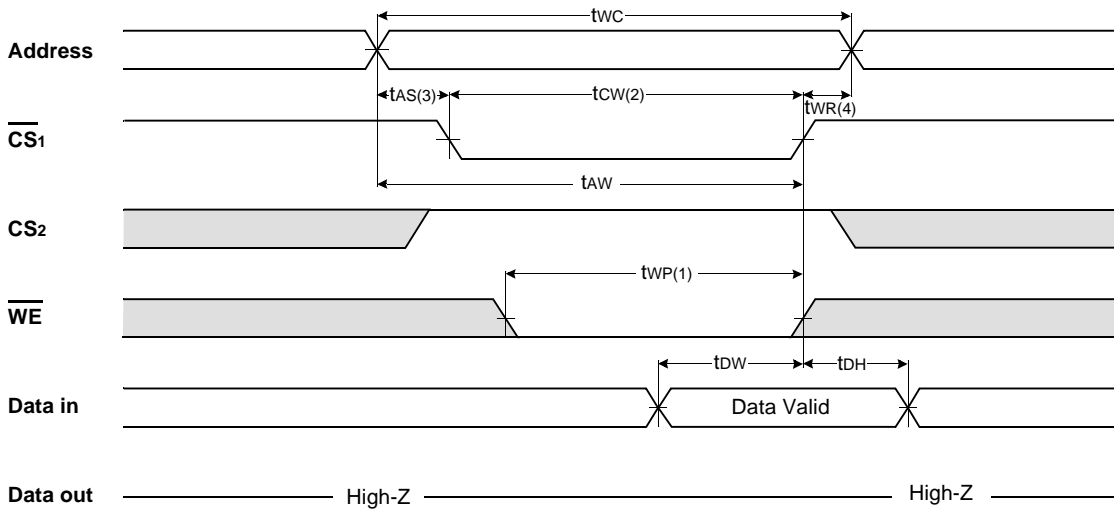
**NOTES (READ CYCLE)**

1.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition,  $t_{HZ}(\text{Max.})$  is less than  $t_{LZ}(\text{Min.})$  both for a given device and from device to device interconnection.

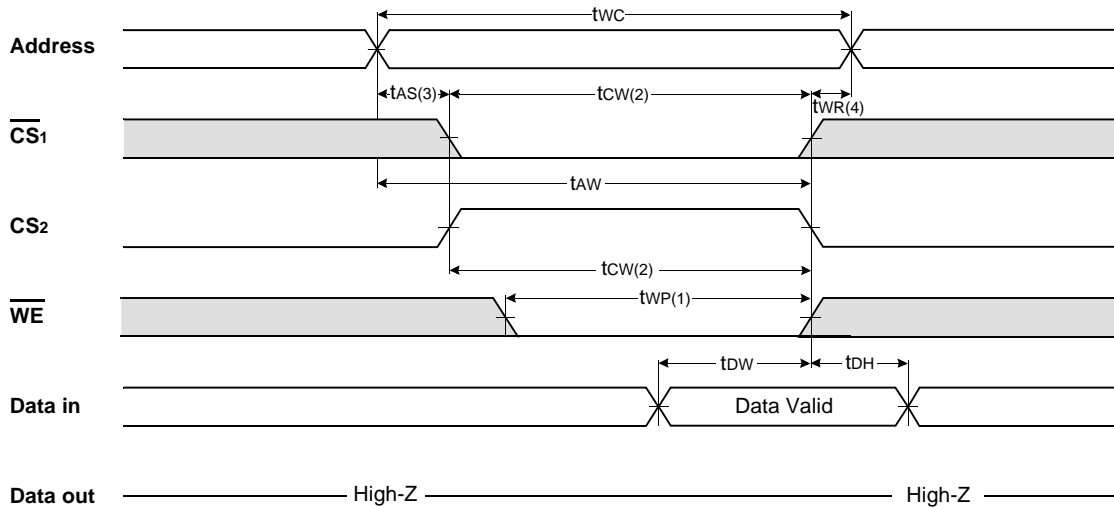
TIMING WAVEFORM OF WRITE CYCLE(1) ( $\overline{WE}$  Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ( $\overline{CS1}$  Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS<sub>2</sub> Controlled)

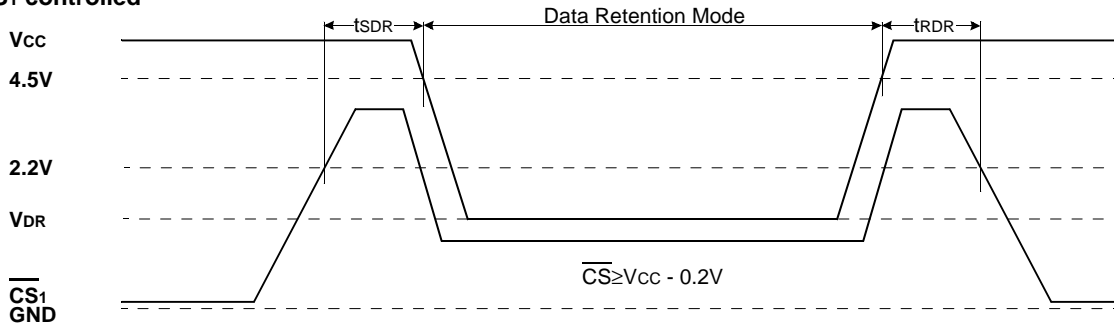


NOTES (WRITE CYCLE)

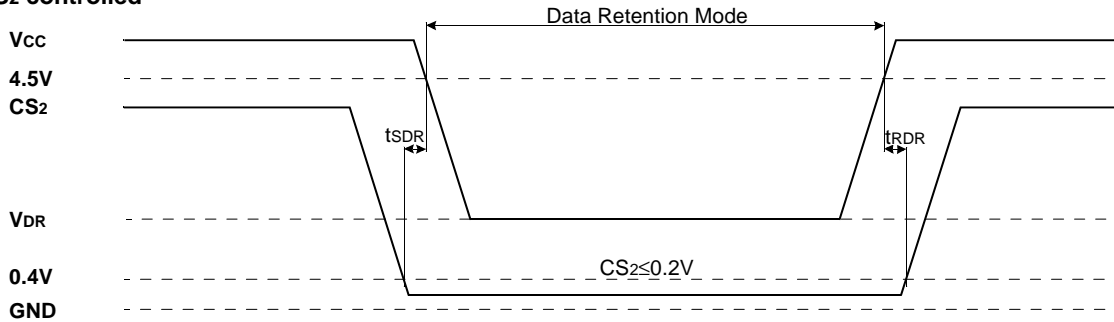
1. A write occurs during the overlap of a low  $\overline{CS}_1$ , a high  $CS_2$  and a low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CS}_1$  goes low,  $CS_2$  going high and  $\overline{WE}$  going low: A write ends at the earliest transition among  $\overline{CS}_1$  going high,  $CS_2$  going low and  $\overline{WE}$  going high,  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from the  $\overline{CS}_1$  going low or  $CS_2$  going high to the end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR}$  applied in case a write ends as  $\overline{CS}_1$  or  $\overline{WE}$  going high  $t_{WR2}$  applied in case a write ends as  $CS_2$  going to low.

DATA RETENTION WAVE FORM

$\overline{CS}_1$  controlled



$CS_2$  controlled







## PACKAGE DIMENSIONS

Units: millimeters(inches)

### 32 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0820F)

