AMIC

A27L6308

Preliminary ***64K X 8 LOW VOLTAGE OTP CMOS EPROM***

Document Title

64K X 8 LOW VOLTAGE OTP CMOS EPROM

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue	July 14, 1998	

Preliminary

64K X 8 LOW VOLTAGE OTP CMOS EPROM

Features

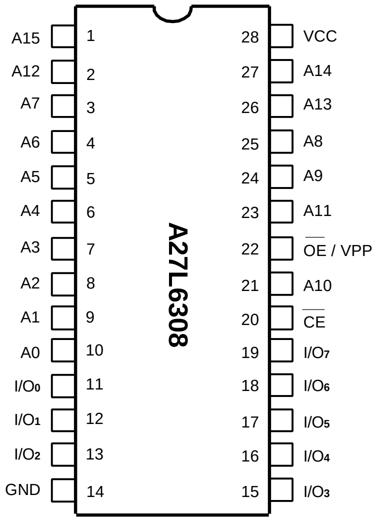
- 65,536 X 8 bit organization
- Programming voltage: 12.75V
- VCC power supply range: 3.0V to 3.6V
- Access time: 120 ns (max.)
- Current: Operating: 15mA (max.)
  Standby: 50µA (max.)
- All inputs and outputs are directly TTL-compatible
- Available in 28-pin DIP and 32-PLCC packages

General Description

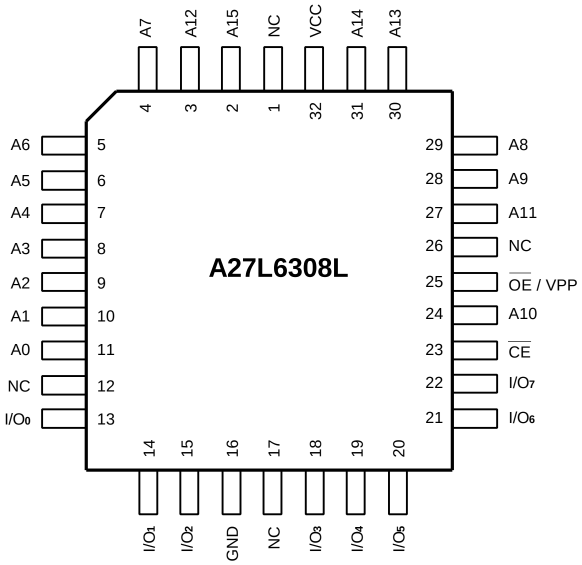
The A27L6308 chip is a low-voltage 524,288 bit one-time programmable read only memory (OTP EPROM) organized as 64K by 8 bits. The A27L6308 requires only 3.3V power supply in normal read mode operation and any input signals are TTL levels. The A27L6308 is available in industry standard 28 pin dual-in-line and 32 lead PLCC packages.

Pin Configurations

■ **DIP**


A27L6308
A15 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
I/O_0 11
I/O_1 12
I/O_2 13
GND 14
28 VCC
27 A14
26 A13
25 A8
24 A9
23 A11
22 $\overline{OE}$ / VPP
21 A10
20 $\overline{CE}$
19 I/O_7
18 I/O_6
17 I/O_5
16 I/O_4
15 I/O_3

■ **PLCC**


A27L6308L
A7 4
A12 3
A15 2
NC 1
VCC 32
A14 31
A13 30
A6 5
A5 6
A4 7
A3 8
A2 9
A1 10
A0 11
NC 12
I/O_0 13
29 A8
28 A9
27 A11
26 NC
25 $\overline{OE}$ / VPP
24 A10
23 $\overline{CE}$
22 I/O_7
21 I/O_6
14 I/O_1
15 I/O_2
16 GND
17 NC
18 I/O_3
19 I/O_4
20 I/O_5

Pin Configurations

Pin Name	Function
A0-A15	Address Inputs
I/O_7-I/O_0	Data Inputs / Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$ / VPP	Output Enable / Program Power Supply
VCC	Power Supply
GND	Ground
NC	No Internal Connection

Operating Modes and Truth Table

Mode	$\overline{CE}$	$\overline{OE}$ / VPP	A0	A1	A9	VCC	I/O_7-I/O_0
Read	V_{IL}	V_{IL}	X	X	X	VCC	Data Out
Output Disable	V_{IL}	V_{IH}	X	X	X	VCC	Hi-Z
Standby	V_{IH}	X	X	X	X	VCC	Hi-Z
Program	V_{IL}	12.75V	X	X	X	6.25V	Data In
Program Verify	V_{IL}	V_{IL}	X	X	X	6.25V	Data Out
Program Inhibit	V_{IH}	12.75V	X	X	X	6.25V	Hi-Z
Manufacturer Code(3)	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{ID}	VCC	37H
Device Code(3)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{ID}	VCC	3DH
Continuation Code(3)	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{ID}	VCC	7FH

Notes:

1. X = Either V_{IH} or V_{IL}.
2. V_{ID} = 12V ± 0.5V.
3. A2 ~ A8 = A10 ~ A15 = V_{IL} (For auto identification)

Functional Description

Read Mode

The A27L6308 has two control functions, both of which must be logically active in order to obtain data at the outputs. $\overline{CE}$ is the power control and should be used for device selection. $\overline{OE}$ is the output control and should be used to data to the output pins, which is independent of device selection. Assuming that addresses are stable, address access time (t_{AA}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the output after a delay (t_{OE}) from the falling edge of $\overline{OE}$, as long as $\overline{CE}$ has been low and the addresses have been stable for at least t_{AA} - t_{OE}.

Standby Mode

The A27L6308 has a standby mode which reduces the active current from 15mA to 50µA. The A27L6308 is placed in the standby mode by applying a CMOS high signal to $\overline{CE}$. When in the standby mode, the output are in a high impedance state, independent of the $\overline{OE}$.

Auto Identify Mode

The auto identify mode allows the reading out of a binary code from a EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm.

To activate the mode, the programming equipment must apply 12.0V ± 0.5V on address line A9 of the A27L6308. Three identification code can be read from data output pin by toggling A0 and A1. The other addresses must be held at V_{IL} during this mode. Byte 0 (with A0 at V_{IL}, A1 at V_{IL}) represents the manufacturer code which is 37H. Byte 1 and Byte 2 represent the device code and continuation code, which is 3DH and 7FH respectively. All identifiers for these codes will possess odd parity, with MSB (IO_7) defined the parity bit.

Absolute Maximum Ratings*

Ambient Operating Temperature (T_A) . . . . -10°C to +85°C
Storage Temperature Plastic Package (T_{STG}) . . . . -55°C to 125°C
Applied Input Voltage (V_I):
  All Pins Except A9, VPP and VCC . . . . -0.6V to VCC + 0.6V
  A9, VPP . . . . -0.6V to 13.5V
  VCC . . . . -0.6V to 7.0V
Output Voltage (V_O) . . . . -0.6V to 7.0V (Note 1)

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. During voltage transitions, the input may undershoot GND to -2.0V for periods less than 20 ns. Maximum DC voltage on input and I/O may overshoot to VCC + 2.0V for periods less than 20 ns.
2. When transitions, A9 and VPP may undershoot GND to -2.0V for periods less than 20 ns. Maximum DC input voltage on A9 and VPP is +13.5V which may overshoot to 14.0V for period less than 20 ns.

Read Mode DC Electrical Characteristics (Ta = 0°C to 70°C, VCC = 3.3V ± 10%, VPP = VCC)

Symbol	Parameter	Min.	Max.	Unit	Conditions
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -100μA
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 1.6mA
V_{IH}	Input High Voltage	2.0	VCC + 0.5	V	
V_{IL}	Input Low Voltage	-0.5	0.6	V	
I_{LI}	Input Leakage Current	-1	+1	μA	VCC = max. Vin = 0V to VCC
I_{LO}	Output Leakage Current	-1	+1	μA	VCC = max. Vout = 0V to VCC
I_{CC}	VCC Read Operating Current		15	mA	VCC = max. $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IL} Iout = 0mA
I_{SB}	VCC Standby Current (TTL)		1	mA	VCC = max. $\overline{CE}$ = V_{IH}
I_{SB1}	VCC Standby Current (CMOS)		50	μA	VCC = max. $\overline{CE}$ = VCC - 0.2V
I_{PP}	VPP Current During Read		10	μA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, VPP = VCC
I_{ID}	A9 Auto Select Current		100	μA	A9 = V_{ID}, VCC = max.

Capacitance (T_A = 25°C, f = 1.0MHz)

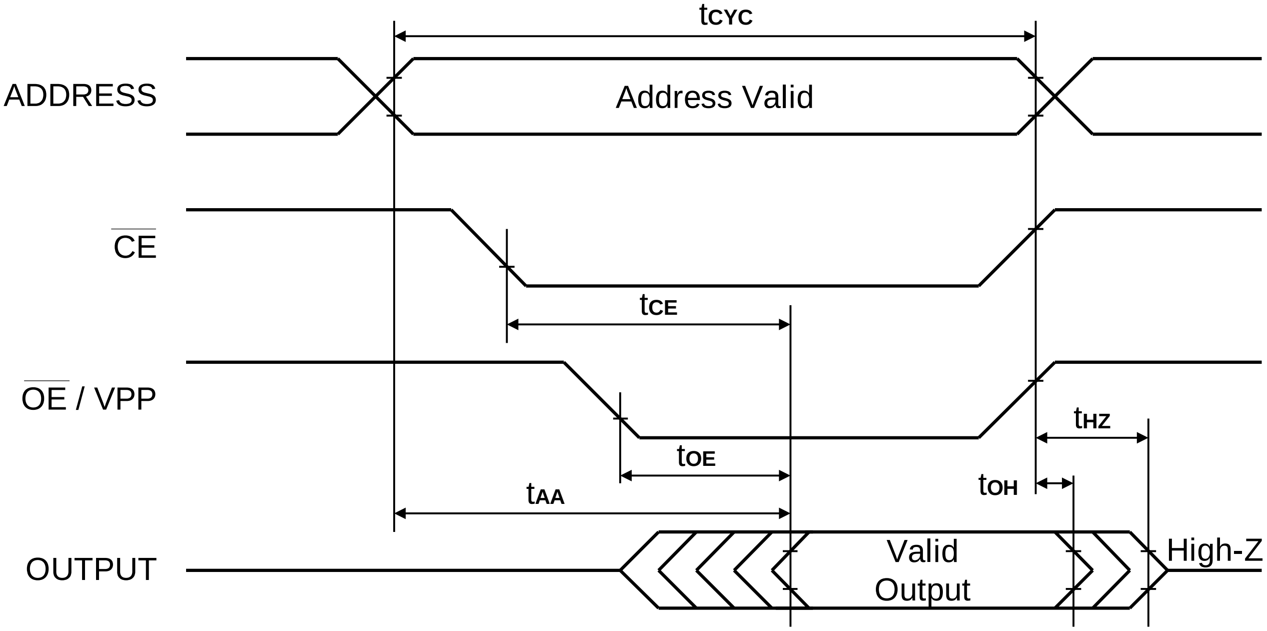
Symbol	Parameter	Min.	Max.	Unit	Conditions
C_{IN}	Input Capacitance		8	pF	V_{IN} = 0V
C_{Out}	Output Capacitance		8	pF	V_{Out} = 0V

* These parameters are sampled and not 100% tested.

Read Mode AC Characteristics (Ta = 0°C to 70°C, VCC = 3.3V ± 10%, VPP = VCC)

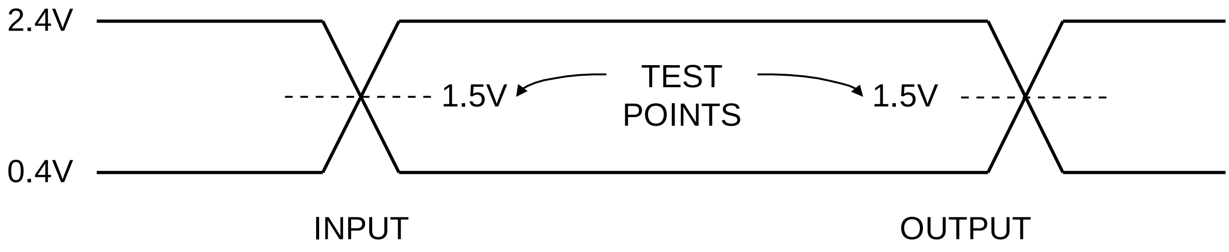
Symbol	Parameter	120ns		Unit
		Min.	Max.	
t_{CYC}	Cycle Time	120		ns
t_{AA}	Address Access Time		120	ns
t_{CE}	Chip Enable Access Time		120	ns
t_{OE}	Output Enable Access Time		50	ns
t_{OH}	Output Hold after Address, $\overline{CE}$ or $\overline{OE}$, whichever Occurred First	0		ns
t_{HZ}	Output High Z Delay		30	ns

Read Mode Switching Waveforms

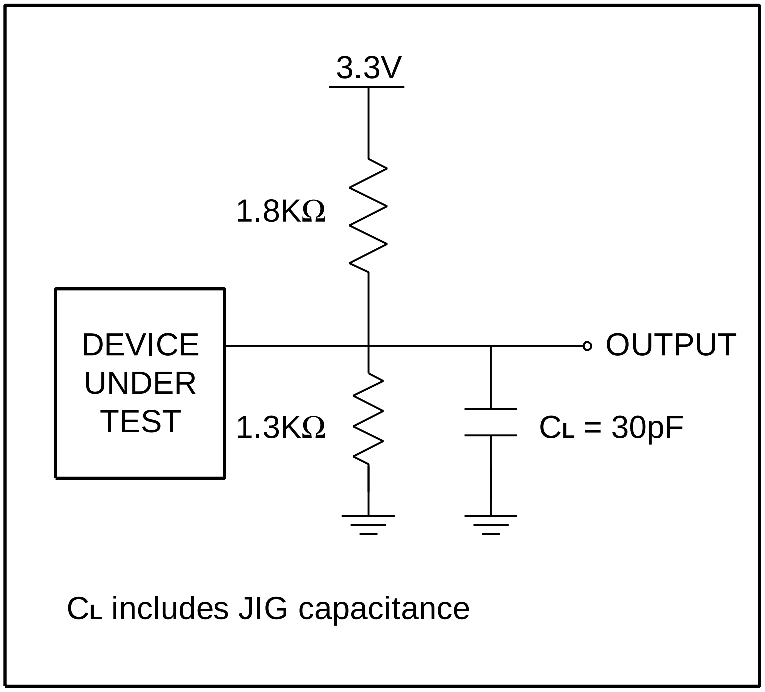

tCYC
ADDRESS
Address Valid
CE
tCE
OE / VPP
tOE
tAA
tHZ
tOH
OUTPUT
Valid Output
High-Z

AC Measurement Conditions

for 120 ns ① Input Rise and Fall Times ≤ 5 ns
Input Pulse Voltage: 0.4V to 2.4Volt
Input and Output Timing Ref. Voltage: 0.8V to 1.5Volt


2.4V
0.4V
1.5V
TEST POINTS
1.5V
INPUT
OUTPUT

AC Testing Load Circuit


3.3V
1.8KΩ
DEVICE UNDER TEST
OUTPUT
1.3KΩ
C_L = 30pF
C_L includes JIG capacitance

Programming and Program Verify

The programming flowchart is shown in Page 10.

The A27L6308 is shipped with all bits being set to "1". Programming causes relevant bits to be changed to "0". The programming mode is started by setting VCC to 6.25V, $\overline{OE}$/VPP to +12.75V and $\overline{CE}$ is at V_{IL}. Data to be programmed can be directly input in the 8 bit format through the data bus.

The write programming algorithm reduces programming time by using 100µs pulse followed by a byte verification to determine whether the byte has been successfully programmed. If the data does not pass the verification, an additional pulse programming is applied for a maximum of 25 pulses. On completion of 1 byte programming and, The verified address is incremented. After the final address is completed, all bytes are verified again with VCC = 5.0 Volt.

Program Inhibit

This mode is used to program one of multiple A27L6308 whose VCC, address bus and data bus are connected in parallel. When programming is performed, other A27L6308 can be inhibited from being programmed by setting their $\overline{CE}$ pins to V_{IH} and $\overline{OE}$/VPP pins to +12.75V.

Programming Mode DC Characteristics (Ta = 0°C to 70°C, VCC = 6.25V ± 0.25V, VPP = 12.75V ± 0.25V)

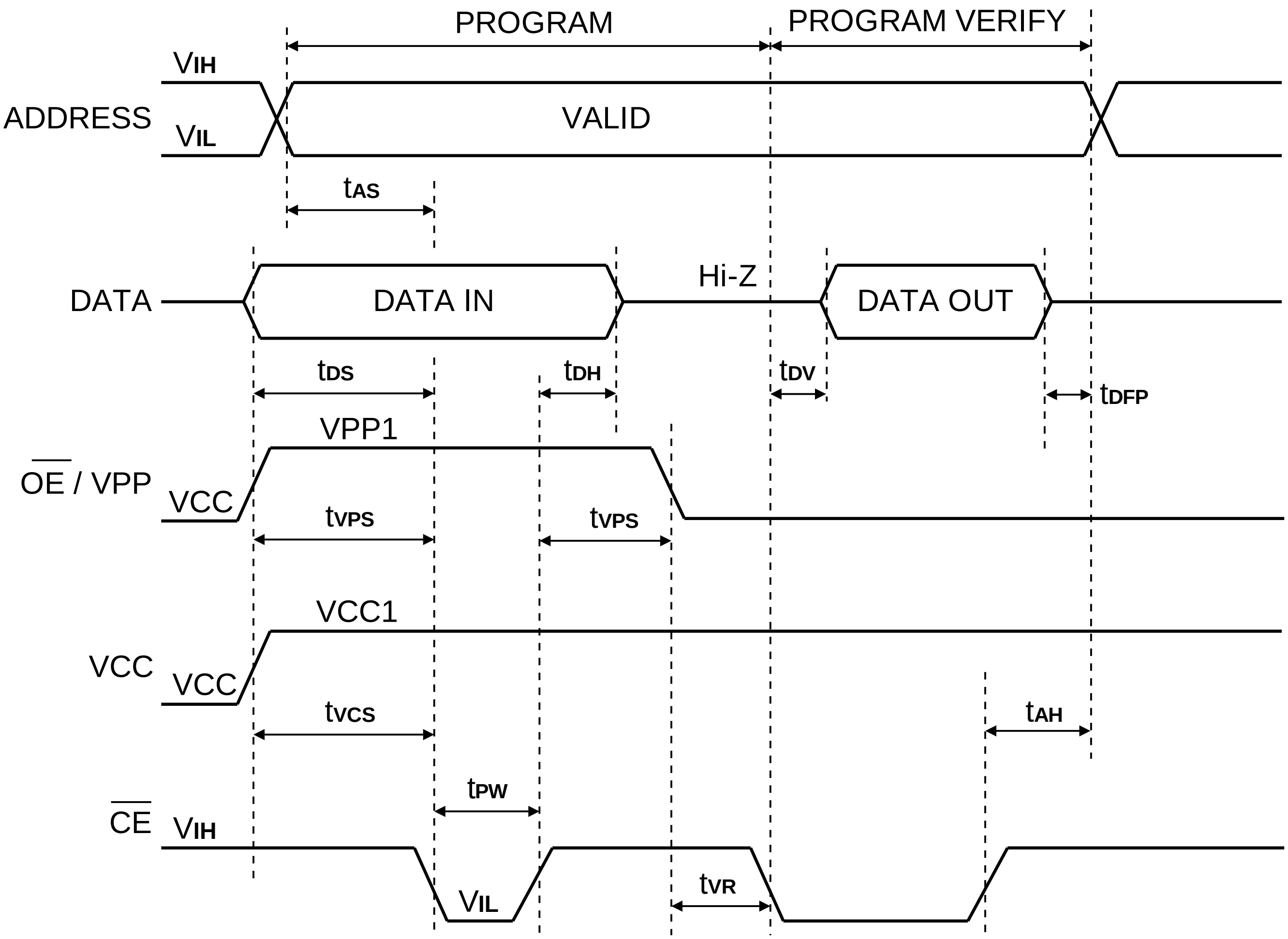
Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{IH}	Input High Voltage	2.0	VCC + 0.5	V	
V_{IL}	Input Low Voltage	-0.5	0.6	V	
I_{LI}	Input Leakage Current	-1	+1	µA	VCC = max. Vin = 0V to VCC
I_{CC}	VCC Current During Program		50	mA	
I_{PP}	VPP Current During Program		50	mA	$\overline{CE}$ = V_{IL}
V_{ID}	A9 Auto Select Voltage	11.5	12.5	V	A9 = V_{ID}
VCC1	Programming Supply Voltage	6.0	6.5	V	
VPP1	Programming Voltage	12.5	13	V	

Note: VCC must be applied simultaneously or before VPP and removed simultaneously or after VPP.

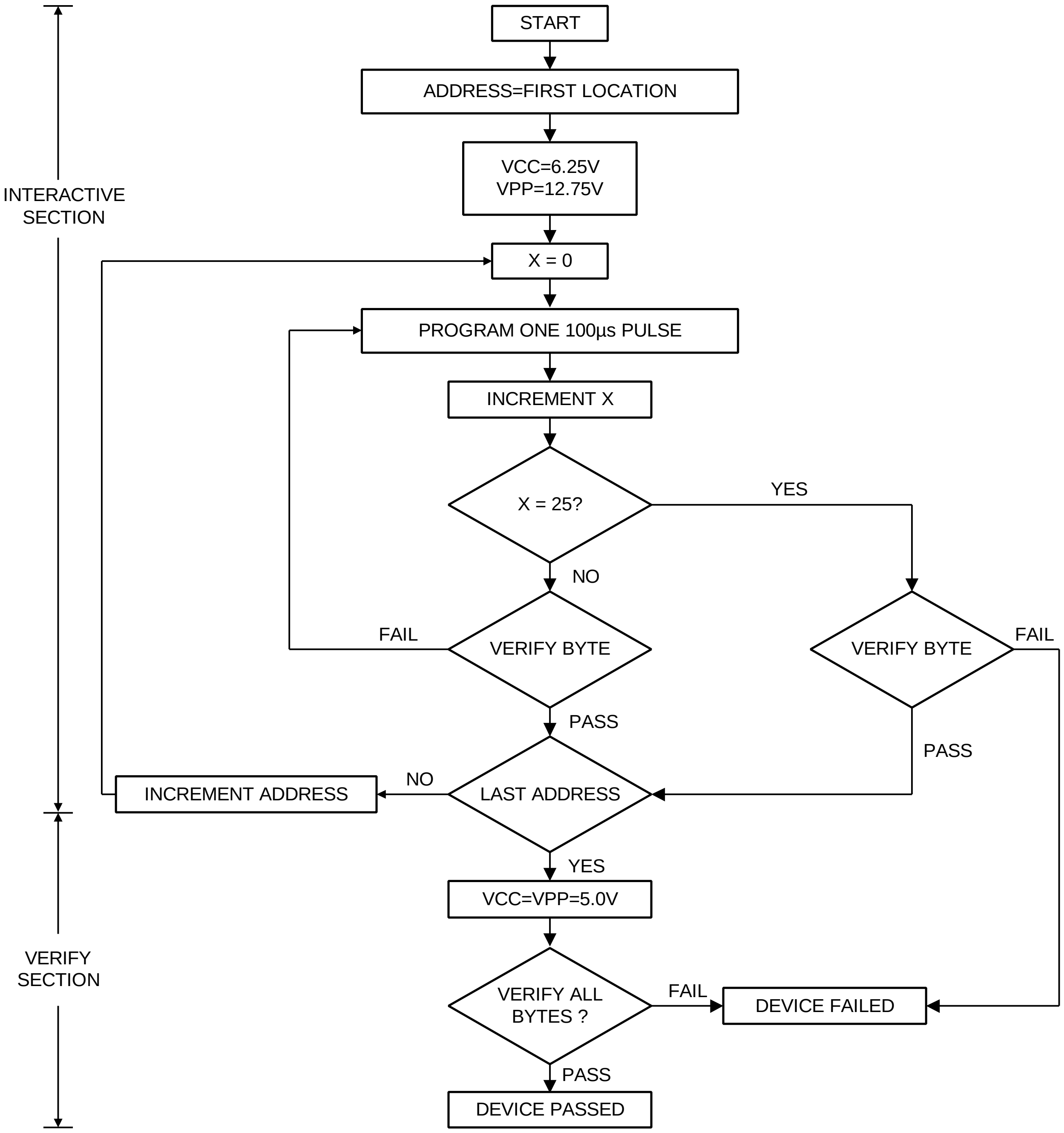
Programming Mode AC Characteristics (Ta = 0°C to 70°C, VCC= 6.25V ± 0.25V, VPP = 12.75V ± 0.25V)

Symbol	Parameter	Min.	Max.	Unit
t_{AS}	Address Valid to Program Low	2		µs
t_{DS}	Input Valid to Program Low	2		µs
t_{VPS}	VPP Set up Time	2		µs
t_{VCS}	VCC Set up Time	2		µs
t_{PW}	Program Pulse Width	95	105	µs
t_{DH}	Data Hold Time	2		µs
t_{VR}	$\overline{OE}$ / VPP Recovery Time	2		µs
t_{DV}	Data Valid from $\overline{CE}$		100	ns
t_{DFP}	Chip Enable to Output Float Delay		130	ns
t_{AH}	Address Hold Time	0		ns

Programming and Verify Mode AC Waveforms


PROGRAM
PROGRAM VERIFY
ADDRESS
VIH
VIL
VALID
tAS
DATA
DATA IN
Hi-Z
DATA OUT
tDS
tDH
tDV
tDFP
VPP1
OE / VPP
VCC
tVPS
tVPS
VCC1
VCC
VCC
tVCS
tAH
tPW
CE
VIH
VIL
tVR

Programming Flowchart


INTERACTIVE SECTION
VERIFY SECTION
START
ADDRESS=FIRST LOCATION
VCC=6.25V
VPP=12.75V
X = 0
PROGRAM ONE 100µs PULSE
INCREMENT X
X = 25?
YES
NO
VERIFY BYTE
FAIL
PASS
VERIFY BYTE
FAIL
PASS
LAST ADDRESS
NO
INCREMENT ADDRESS
YES
VCC=VPP=5.0V
VERIFY ALL BYTES ?
FAIL
DEVICE FAILED
PASS
DEVICE PASSED

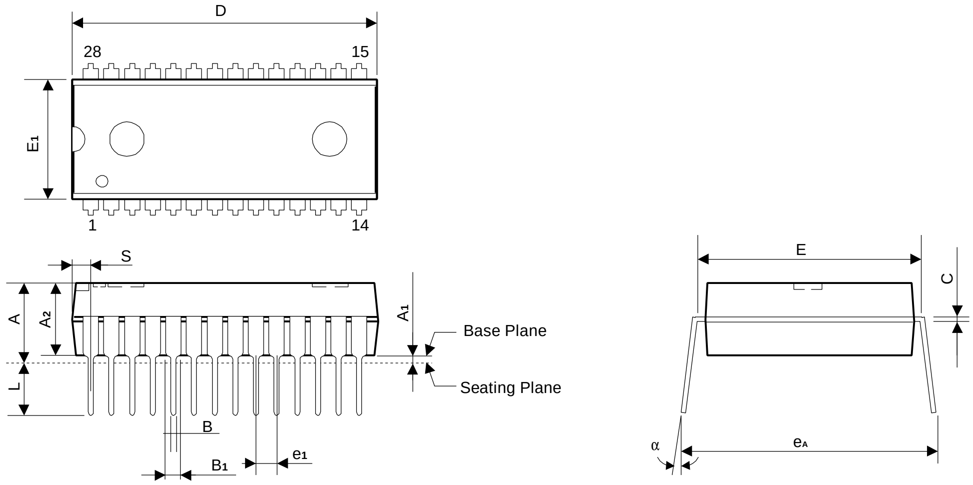
Ordering Information

Part No.	Access Time (ns)	Operating Current Max. (mA)	Standby Current Max. (μA)	Package
A27L6308-12	120	15	50	28Pin DIP
A27L6308L-12	120	15	50	32Pin PLCC

Package Information

P-DIP 28L Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.210	-	-	5.33
A_1	0.010	-	-	0.25	-	-
A_2	0.150	0.155	0.160	3.81	3.94	4.06
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.058	0.060	0.064	1.47	1.52	1.63
C	0.008	0.010	0.014	0.20	0.25	0.36
D	-	1.460	1.470	-	37.08	37.34
E	0.590	0.600	0.610	14.99	15.24	15.49
E_1	0.540	0.545	0.550	13.72	13.84	13.97
e_1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
α	0°	-	15°	0°	-	15°
e_A	0.630	0.650	0.670	16.00	16.51	17.02
S	-	-	0.090	-	-	2.29

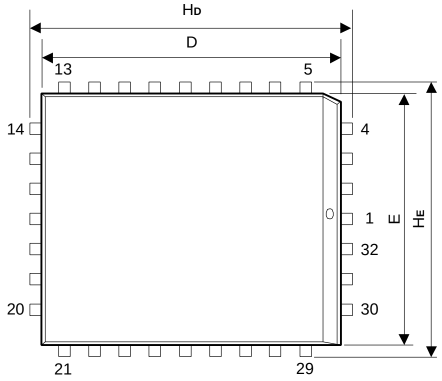
Notes:

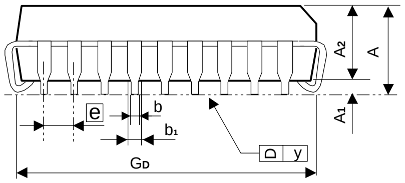
1. The maximum value of dimension D includes end flash.
2. Dimension E_1 does not include resin fins.
3. Dimension S includes end flash.

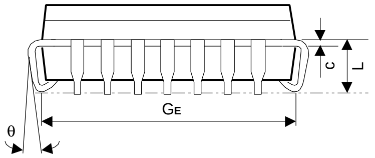
Package Information

PLCC 32L Outline Dimension

unit: inches/mm







Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.134	-	-	3.40
A_1	0.0185	-	-	0.47	-	-
A_2	0.105	0.110	0.115	2.67	2.80	2.93
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.021	0.41	0.46	0.54
C	0.008	0.010	0.014	0.20	0.254	0.35
D	0.547	0.550	0.553	13.89	13.97	14.05
E	0.447	0.450	0.453	11.35	11.43	11.51
$\boxed{e}$	0.044	0.050	0.056	1.12	1.27	1.42
G_D	0.490	0.510	0.530	12.45	12.95	13.46
G_E	0.390	0.410	0.430	9.91	10.41	10.92
H_D	0.585	0.590	0.595	14.86	14.99	15.11
H_E	0.485	0.490	0.495	12.32	12.45	12.57
L	0.075	0.090	0.095	1.91	2.29	2.41
y	-	-	0.003	-	-	0.075
θ	0°	-	10°	0°	-	10°

Notes:

1. Dimensions D and E do not include resin fins.
2. Dimensions G_D & G_E are for PC Board surface mount pad pitch design reference only.