June 1992
Edition 1.0

FUJITSU

DATA SHEET

T-46-13-29

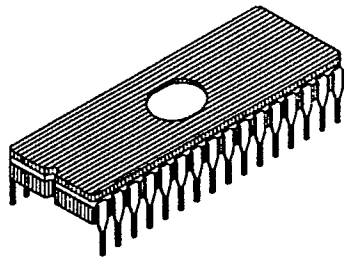
MBM27C2000 -12/-15
CMOS 2M-BIT UV EPROM

CMOS 2,097,152-BIT UV ERASABLE READ ONLY MEMORY (EPROM)

The Fujitsu MBM27C2000 EPROM is a high speed read-only static memory that is UV-erasable and reprogrammable. The device contains 2,097,152 programmable or reprogrammable bits organized in a 262,144-byte/8-bit format. The MBM27C2000 is housed in a 32-pin DIP with a transparent lid; when the lid is properly exposed to an ultraviolet light source, a previously programmed bit pattern is erased in approximately 15 to 20 minutes. A new bit pattern can then be written into memory.

The MBM27C2000 EPROM is fabricated using CMOS double poly-silicon gate technology with stacked single-transistor gate cells. The MBM27C2000 is an excellent choice for system development work and in other applications where program changes are frequently necessary. Once programmed, the device requires only a single +5V power supply; the current requirements are exceptionally low in both the active and standby modes of operation.

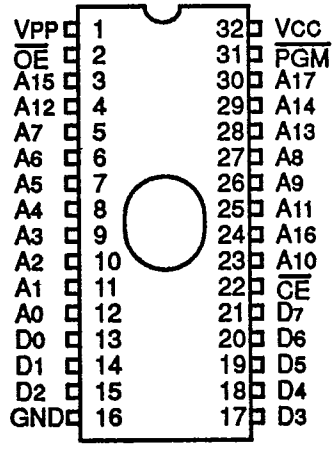
- 262,144-byte/8-bit organization with on-chip decoding
- Single-Byte or Four-Byte programming capability with high speed programming algorithm
- Static operation (no clocks required)
- Fast access time:
  120ns max. (MBM27C2000-12)
  150ns max. (MBM27C2000-15)
- Easy and simple memory expansion via @pin
- Three-state output for wired-OR capability
- TTL-compatible inputs/outputs
- Single +5V (±10%) power supply with low current drain:
  Active operation = 50mA(max)
  Standby operation = 0.1mA(max)
- Programming voltage: +12.5V
- 32-pin ceramic DIP Package (Suffix: P)



CERAMIC PACKAGE
DIP-32C-C02

PIN ASSIGNMENT

(TOP VIEW)



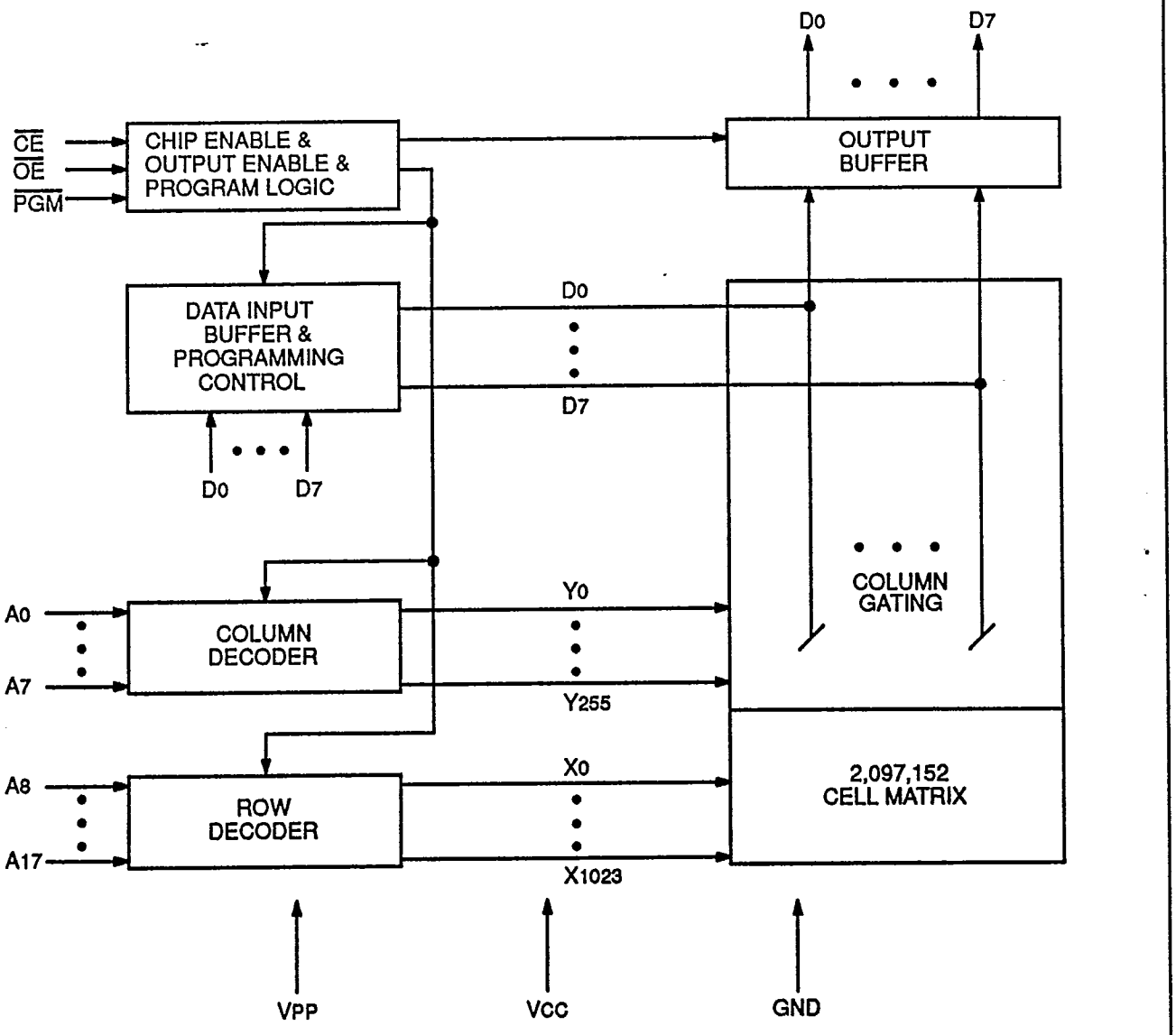
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Supply Voltage with respect to ground	VCC	−0.6 to +7.0	V
Programming Voltage with respect to ground	VPP	−0.6 to +14.0	V
Input/Output Voltage (except for A9 with respect to ground)	VIN1, VOUT	−0.6 to VCC +0.6	V
Programming Voltage with respect to ground	VIN2	−0.6 to +13.5	V
Temperature under Bias	TBIAS	−25 to +85	°C
Storage Temperature Range	TSTG	−65 to +125	°C

NOTE: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig.1 — BLOCK DIAGRAM



CAPACITANCE (TA= 25° C, f = 1MHz)

Parameter	Symbol	Values			Unit
		Min	Typ	Max	
Input Capacitance (VIN=0V)	CIN		5	5.8	pF
Output Capacitance (VOUT=0V)	COUT		8	8.7	pF

PIN DESCRIPTION

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Symbol	Pin No.	Function
V_{PP}	1	+12.5V programming voltage
$\overline{OE}$	2	Output enable. When $\overline{OE}$ and $\overline{CE}$ are active Low and the $\overline{PGM}$ strobe is active High; all output lines(D0 to D7) are enabled.
A0 to A17	3 to 12, 23 to 30	Address lines
D0 to D7	13 to 15, 17 to 21	Three-state output data lines
GND	16	Circuit ground
$\overline{CE}$	22	When active Low, the device is enabled for data read.
$\overline{PGM}$	31	When active Low, programming data from the input buffer is written into a specified address of memory.
V_{CC}	32	+5V power supply

FUNCTIONS AND PIN CONNECTIONS

OPERATING MODE	A0 to A8	A9	A10 to A17	Data	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	VCC	VPP	GND
Standby	X	X	X	Hi-Z	VIH	X	X	5V	5V	0V
Read	AIN	AIN	AIN	DOUT	VIL	VIL	VIH	5V	5V	0V
Output Disable	AIN	AIN	AIN	Hi-Z	VIL	VIH / X	X / VIL	5V	5V	0V
Electronic Signature	Note 1	12V	Note 1	CODE	VIL	VIL	VIH	5V	5V	0V
Single-Byte Program	AIN	AIN	AIN	DIN	VIL	VIH	VIL	6V	12.5V	0V
Single-Byte Verify	AIN	AIN	AIN	DOUT	VIL	VIL	VIH	6V	12.5V	0V
Single-Byte Program Inhibit	AIN	AIN	AIN	Hi-Z	VIL	VIH	VIH	6V	12.5V	0V
Four-Byte Program (Latch)	AIN	AIN	AIN	DIN	VIH	VIH	VIH	6V	12.5V	0V
Four-Byte Program	Note 2	AIN	AIN	Hi-Z	VIH	VIL	VIL	6V	12.5V	0V
Four-Byte Verify	AIN	AIN	AIN	DOUT	VIL	VIL	VIH	6V	12.5V	0V
Four-Byte Program Inhibit	AIN	AIN	AIN	Hi-Z	VIH	VIL	VIH	6V	12.5V	0V

Legend:
X = Don't care

Notes:
1. A0 is toggling address. A1 to A17 are V_{IL}.
2. A0 and A1 are "X". A2 to A8 are AIN.

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage *1	VPP	VCC −0.6	VCC	VCC +0.6	V
Input High Level	VIH	2.0		VCC +0.3	V
Input Low Level	VIL	−0.3		0.8	V
Operating Temperature	TA	0		70	°C

*1 : VPP supply voltage is applied posterior to or coincident with VCC supply voltage and cut off prior to or coincident with VCC supply voltage.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	
Input Leakage Current	$\|I_{LI}\|$	V_{IN} = VCC = 5.5V			10	µA
Output Leakage Current	$\|I_{LO}\|$	V_{OUT} = VCC = 5.5V			10	µA
VCC Standby Current	I_{SB1}	$\overline{CE}$ = VIH			1.0	mA
VCC Standby Current	I_{SB2}	$\overline{CE}$ = VCC ±0.3V			100	µA
VCC Operation Current	ICC	Cycle = min., IOUT = 0mA			50	mA
VPP Supply Current	IPP	VPP = VCC ±0.6V			100	µA
Output High Level	VOH1	IOH = −400µA	2.4			V
Output High Level	VOH2	IOH = −100µA	VCC −0.7			V
Output Low Level	VOL	IOL = 2.1mA			0.45	V

AC CHARACTERISTICS

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(Recommended operating conditions unless otherwise noted)

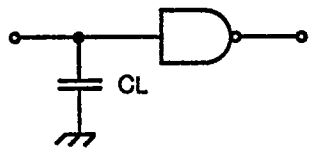
Parameter	Symbol	MBM27C2000-12 Values		MBM27C2000-15 Values		Unit
		Min	Max	Min	Max	
Address Access Time	tACC		120		150	ns
$\overline{CE}$ to Output Delay Time	tCE		120		150	ns
$\overline{OE}$ to Output Delay Time	tOE		60		70	ns
$\overline{PGM}$ to Output Delay Time	tPGM		60		70	ns
$\overline{CE}$ or $\overline{OE}$ to Output Float Delay (Note)	tDF		50		60	ns
Address to Output Hold Time	tOH	0		0		ns

NOTE: Output Float is defined as the point where data is no longer driven.

AC TEST CONDITIONS

Fig. 2 —AC TEST CONDITIONS

Input Pulse Levels:	0.45V to 2.4V
Input Rise/Fall Times:	≤20ns
Input Reference Levels:	0.8V to 2.0V
Output Reference Levels:	0.8V to 2.0V
Output Load:	1 TTL gate and CL = 100pF



AC CHARACTERISTICS

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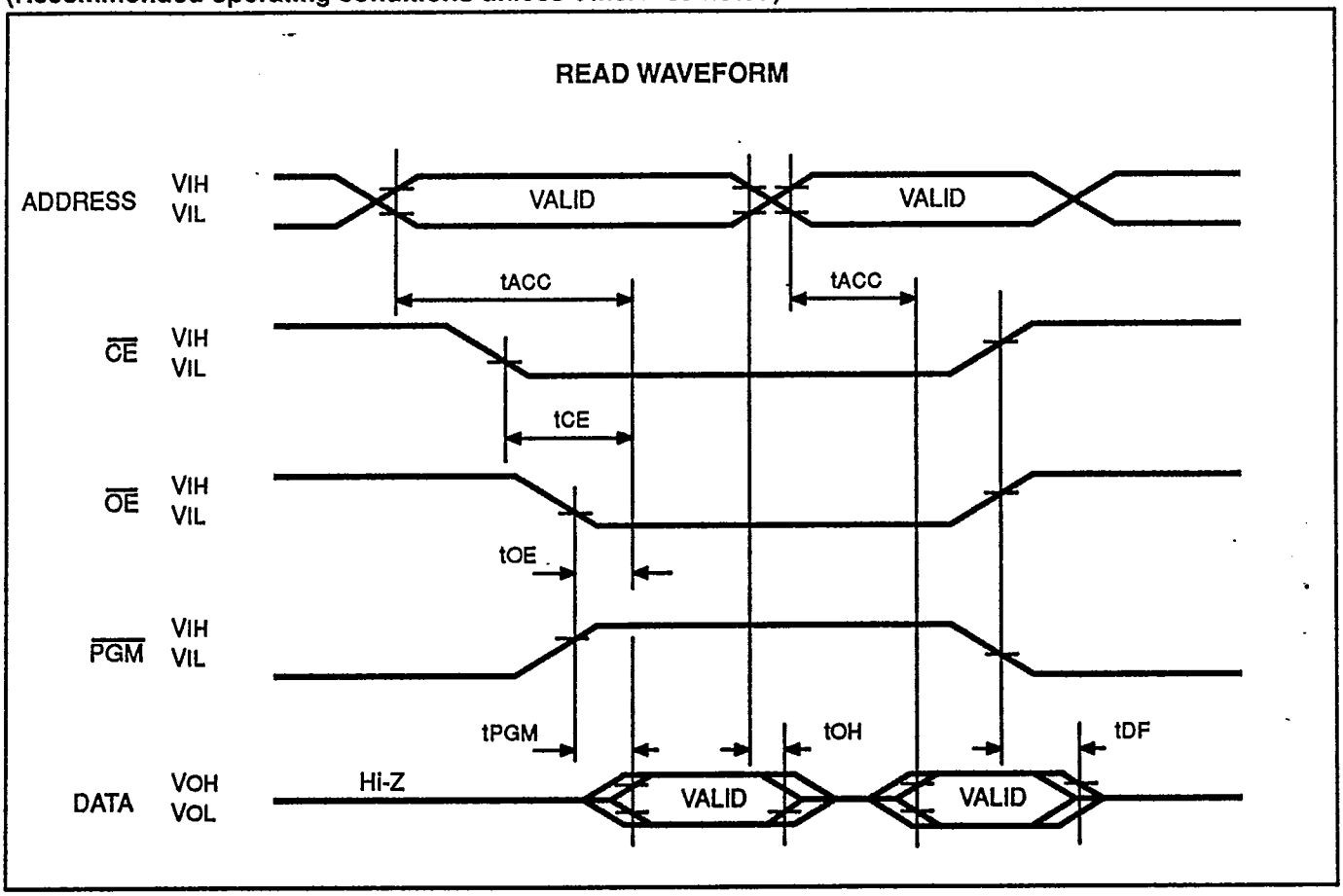
(Recommended operating conditions unless otherwise noted)

READ WAVEFORM



PROGRAMMING / ERASING INFORMATION

PROGRAMMING

Single-Byte Programming. When +12.5V(±0.3) volts is applied to VPP, +6(±0.25) volts is applied to VCC, $\overline{CE}$=VIL, $\overline{PGM}$ =VIH, and $\overline{OE}$= VIH, the programming mode is initiated. Next, the proper address is input and the data pattern is applied to the input buffer (Figure 1). When both address and data are stable, a 0.1-millisecond negative pulse is applied to the $\overline{PGM}$ pin. Upon verification of written data an over pulse (three times the initial pulse width times the number of pulses used to accomplish a write) should be applied to complete the programming of one byte. Refer to the PROGRAMMING FLOWCHART that follows for step-by-step programming procedures.

Four-Byte Programming. When compared to single-byte programming, the four-byte programming method reduces the programming time by about 75% one quarter. Voltages applied to VPP and VCC are the same as those for single-byte programming; however, some logic levels differ-refer to "Four-Byte Programming" in the Truth Table. In conjunction with the $\overline{OE}$ pin, address pins A0 and A1 are used to latch four bytes of data. When both address and data are stable, a 0.1-millisecond negative pulse is applied to the $\overline{PGM}$ pin. Upon verification of written data an over pulse (three times the initial pulse width times the number of pulses used to accomplish a write,) should be applied to complete the programming of four bytes. Refer to the PROGRAMMING FLOWCHART for step-by-step programming procedures.

Caution

The width of one programming pulse must not exceed 40-millisecond; thus, a continuous TTL low-level voltage should not be applied to the $\overline{PGM}$ pin. Also, a 0.1-microfarad capacitor must be connected between VPP and ground to prevent excessive voltage transients. Neglecting either of these precautions may cause device failure.

Electronic Signature/Programming Algorithm. When the MBM27C2000 is shipped from the factory, all memory cells (2,097,152 bits) are set to the High state (logic 1). During the programming procedure, affected bit cells are set to the Low (logic 0) state.

The MBM27C2000 is programmed with a fast programming algorithm designed by Fujitsu called high speed programming. Manufacturer and device codes are electronically stored in each device; these codes can be read at the output port (D0 to D7) for the purpose of matching the device with the high speed programming algorithm. The Electronic Signature Code List is shown in the table preceding the ELECTRICAL CHARACTERISTICS.

ERASING

In order to clear all memory cells of programmed contents, the MBM27C2000 must be exposed to an ultraviolet light source. To completely erase the memory (restore all cells to a logic 1 state), a dosage of 10Wsec/cm² is required. The required exposure can be obtained by using a UV-lamp with a wavelength of 2537 Angstroms and with an intensity of 12mW/cm² . Remove all filters from the lamp and clean the transparent lid of the MBM27C2000 with a non-abrasive cleaner. Hold the MBM27C2000 approximately one inch from the light source for 15 to 20 minutes. (Note. The MBM27C2000 and other similar devices can be erased by light sources with longer wavelengths: however, the erasing time is much greater. Nonetheless, exposure to fluorescents or sunlight will severely degrade and eventually erase the memory. When used in a lighted environment, it is recommended that the transparent window be covered with an opaque label.)

ELECTRONIC SIGNATURE CODE LIST

Definition	A0	A1 to A6	A9	A7, A8, A10 to A17	D0	D1	D2	D3	D4	D5	D6	D7	HEX
Manufacture	VIL	VIL	12(±0.5)V	VIL	0	0	1	0	0	0	0	0	#04
Device	VIH	VIL	12(±0.5)V	VIL	1	1	0	1	0	0	0	0	#0B

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PROGRAMMING INFORMATION (Cont'd)

DC CHARACTERISTICS

(TA = 25 °C ± 5°C, V_{CC} *1 = 6V ± 0.25V, V_{PP} *2 = 12.5V ± 0.3V)

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	
Input Leakage Current	|ILI|	VIN = 6.25V/0V			10	µA
VPP Supply Current (Single-Byte)	IPP1	$\overline{CE}$ = VIL, $\overline{OE}$ = VIH, $\overline{PGM}$ = VIL			30	mA
VPP Supply Current (Four-Byte)	IPP2	$\overline{CE}$ = VIH, $\overline{OE}$ = VIL, $\overline{PGM}$ = VIL			50	mA
VPP Supply Current (Program Inhibit)	IPP3	$\overline{PGM}$ = VIH			5	mA
VPP Supply Current (Program Verify)	IPP4	$\overline{CE}$ = VIL, $\overline{OE}$ = VIL, $\overline{PGM}$ = VIH			5	mA
VCC Supply Current	ICC				50	mA
Input Low Level	VIL		–0.1		0.8	V
Input High Level	VIH		2.0		VCC +0.3	V
Output Low Level	VOL	IOL = 2.1mA			0.45	V
Output High Level	VOH	IOH = –400µA	2.4			V

NOTE : *1 VCC must be applied either coincidentally or before VPP and removed either coincidentally or after VPP.
*2 VPP must not be 13.5volts or more including overshoot. Permanent device damage may occuer if the device is taken out or put into socket remaining VPP=12.5 volts. Also, during $\overline{CE}$=VIL, $\overline{OE}$=VIH, VPP must not be switched from VCC to VPP volts or vice versa.

AC CHARACTERISTICS

(TA = 25 °C ± 5°C, VCC = 6V ± 0.25V, VPP = 12.5V ± 0.3V)

Parameter	Symbol	Values			Unit
		Min	Typ	Max	
Address Setup Time	tAS	0.5			µs
Address Hold Time	tAH	0.5			µs
Data Setup Time	tDS	0.5			µs
Data Hold Time	tDH	0.5			µs
$\overline{OE}$ Hold Time("H")	tOEH	0.5			µs
Hold Time Before Programming	tHBP	2			µs
Programming Pulse Width	tPW	95	100	105	µs
Over Programming Pulse Number	N	1		50	times
Hold Time After Programming	tHAP	2			µs

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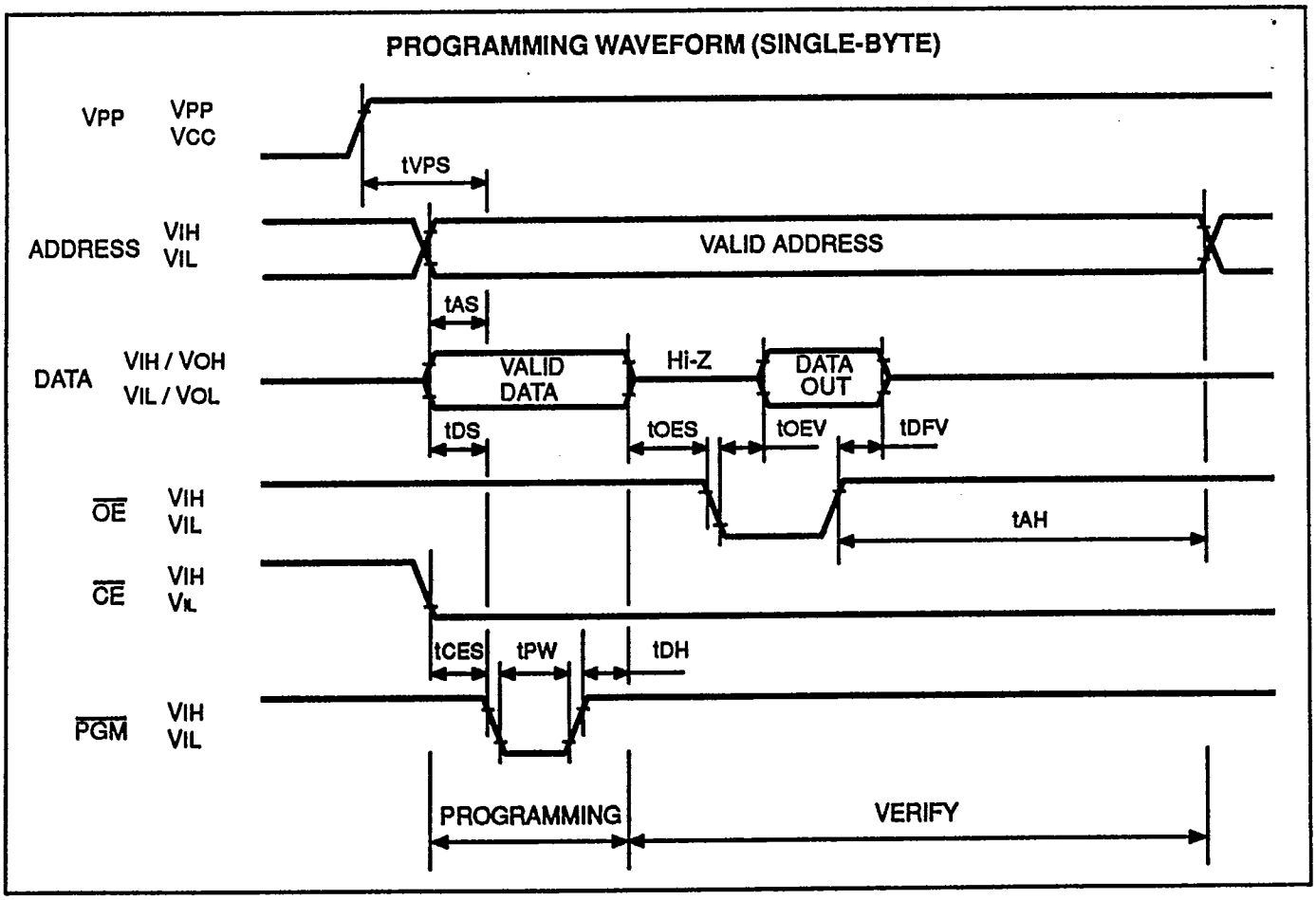
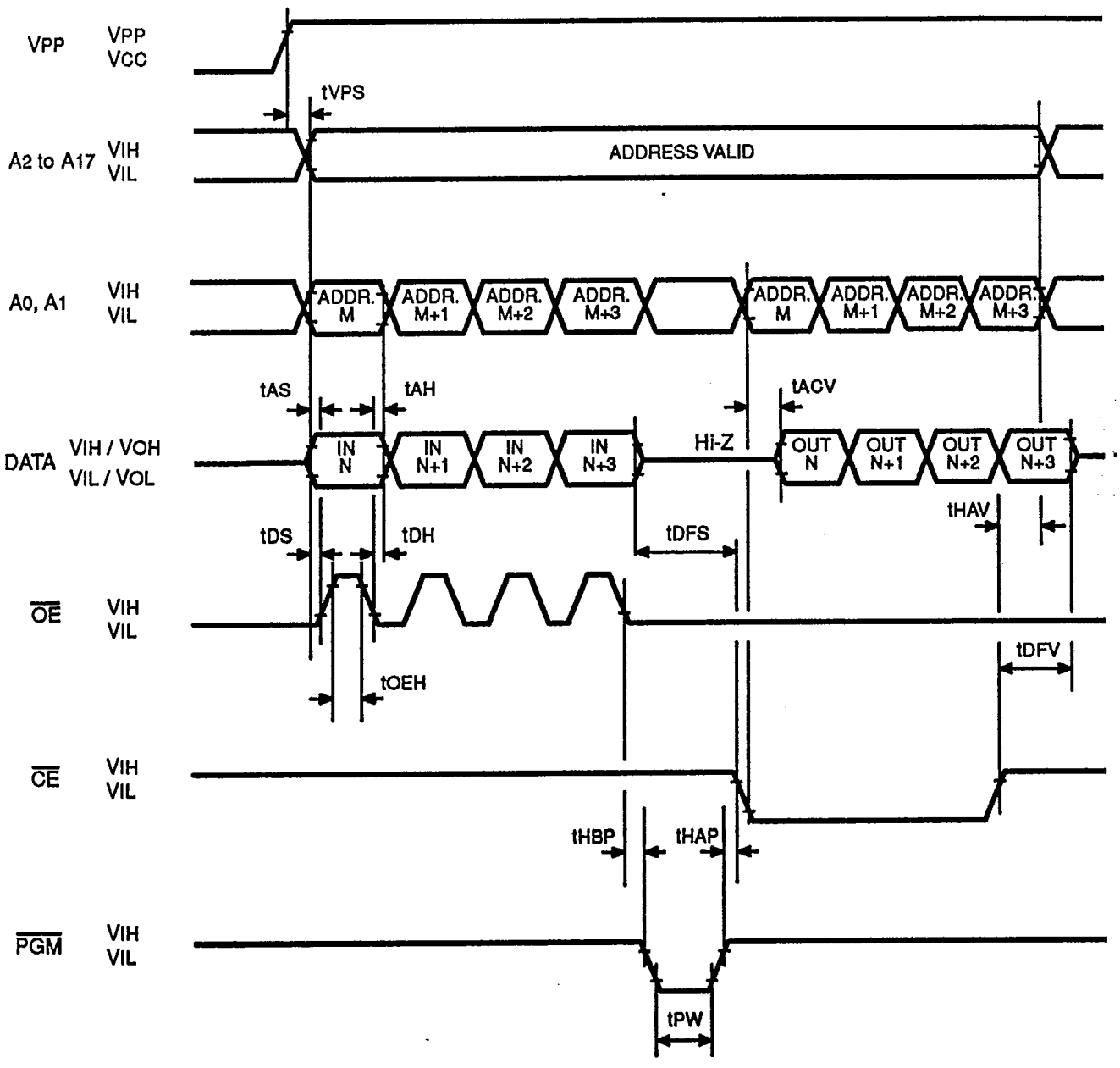
AC CHARACTERISTICS(Cont'd)

Parameter	Symbol	Values			Unit
		Min	Typ	Max	
$\overline{CE}$ Setup Time	tCES	2			µs
$\overline{OE}$ Setup Time	tOES	2			µs
Input Data Floating Setup Time	tDFS	1			µs
Address Access Time at Verify	tACV			500	ns
$\overline{OE}$ to Data Out	tOEV			500	ns
Output Disable to Output Float	tDFV			150	ns
Hold Time After Verify	tHAV	0			µs
V_{PP} Setup Time	tVPS	2			µs

PROGRAMMING WAVEFORM (SINGLE-BYTE)



PROGRAMMING WAVEFORM (FOUR-BYTE)



PROGRAMMING INFORMATION

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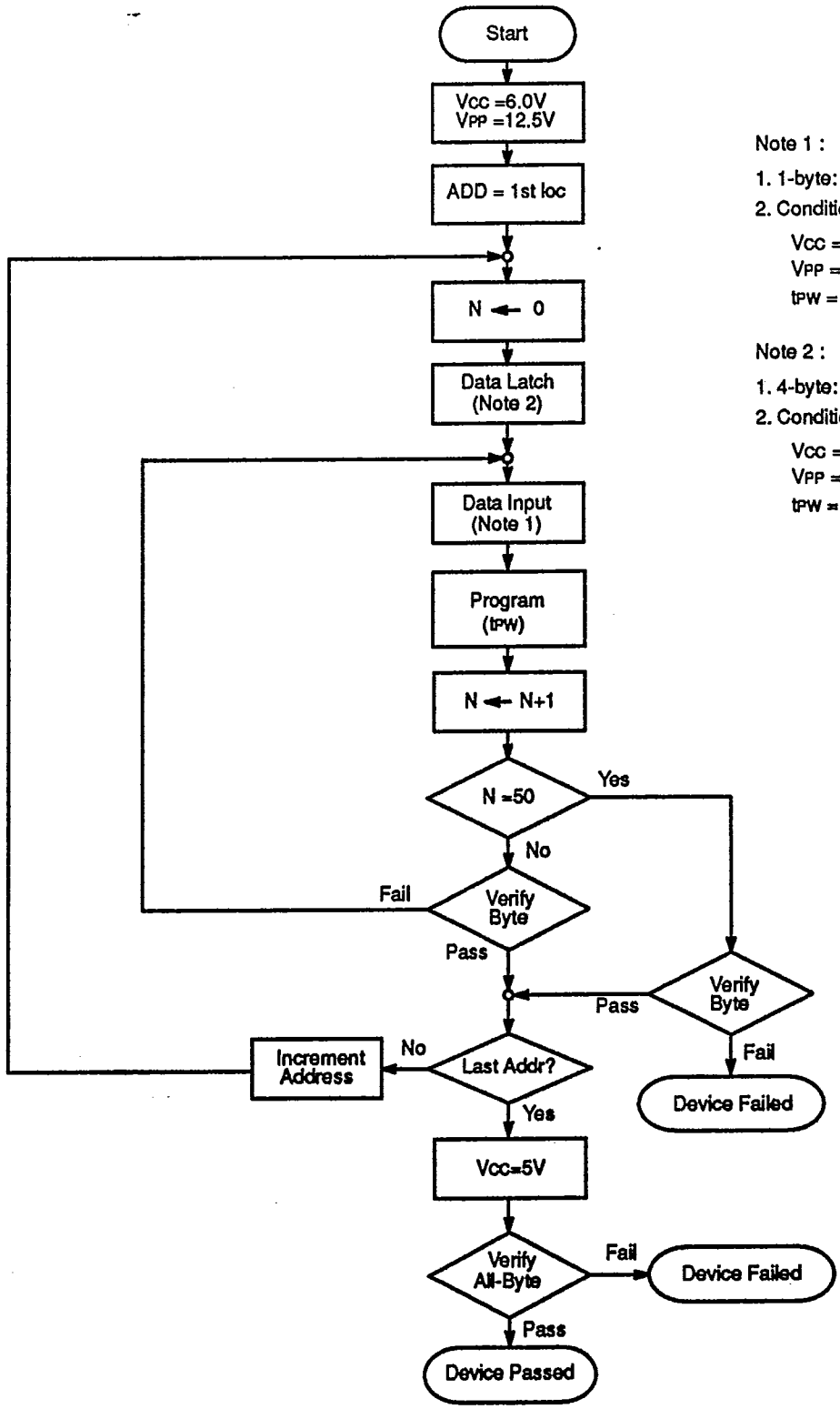
PROGRAMMING FLOWCHART(ADVANCED QUICK PROGRAMMING)



Note 1 :

1. 1-byte:
2. Conditions:

Vcc = 6V(±0.25)V
VPP = 12.5V(±0.3)V
tPW = 100±5µs

Note 2 :

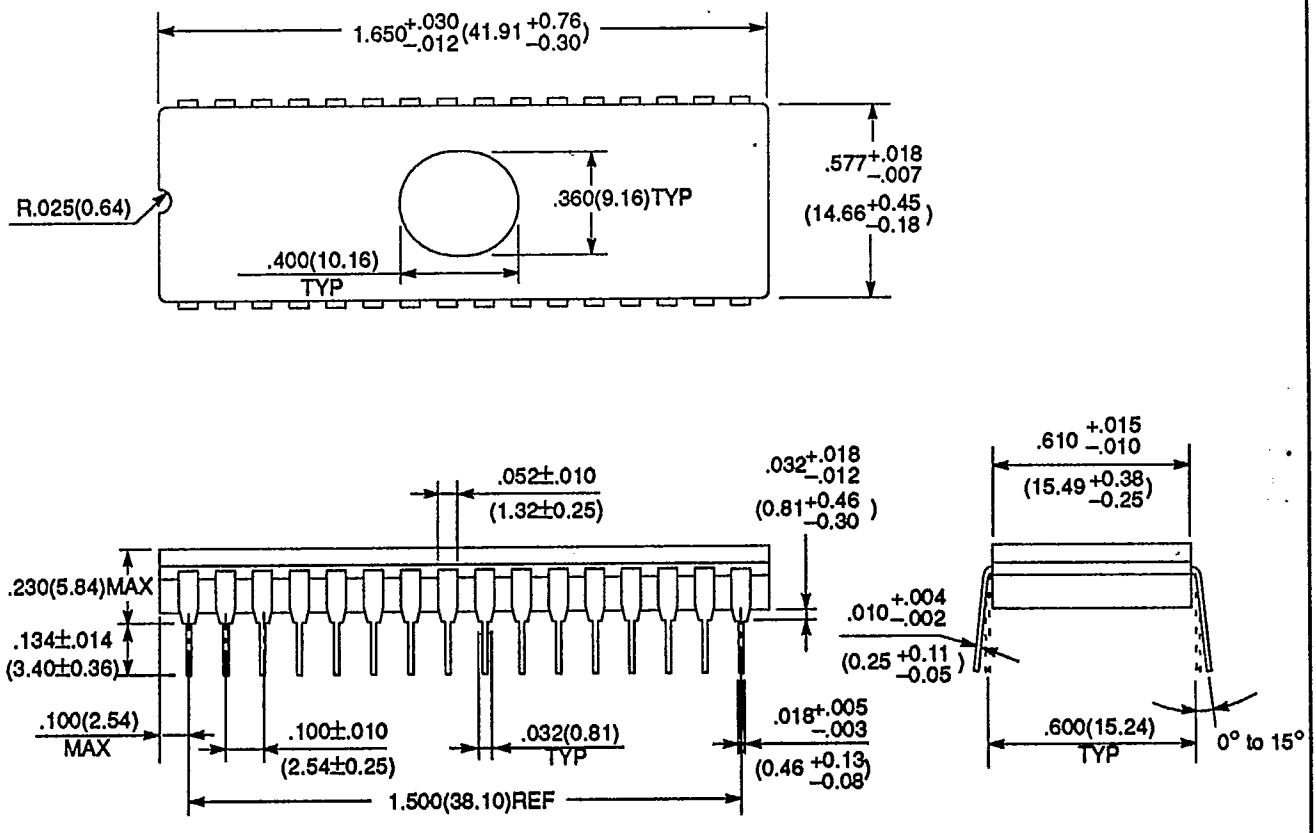
1. 4-byte:
2. Conditions:

Vcc = 6V(±0.25)V
VPP = 12.5V(±0.3)V
tPW = 100±5µs

PACKAGE DIMENSIONS

(Suffix: Z)

32-LEAD CERAMIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-32C-C02)



Dimensions in inches (millimeters)