HM 65756

32 K × 8 High Speed CMOS SRAM

Introduction

The HM 65756 is a high speed CMOS static RAM organised as 32,768 × 8 bits. It is manufactured using MHS's high performance CMOS technology.

Access time as fast as 15 ns are available with maximum power consumption of only 880 mW.

The HM 65756 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 80 % when the circuit is deselected.

Easy memory expansion is provided by an active low chip select ($\overline{CS}$) an active low output enable ($\overline{OE}$), and three state drivers.

All inputs or outputs of the HM-65756 are TTL compatible and operate from single 5 V supply thus simplifying system design.

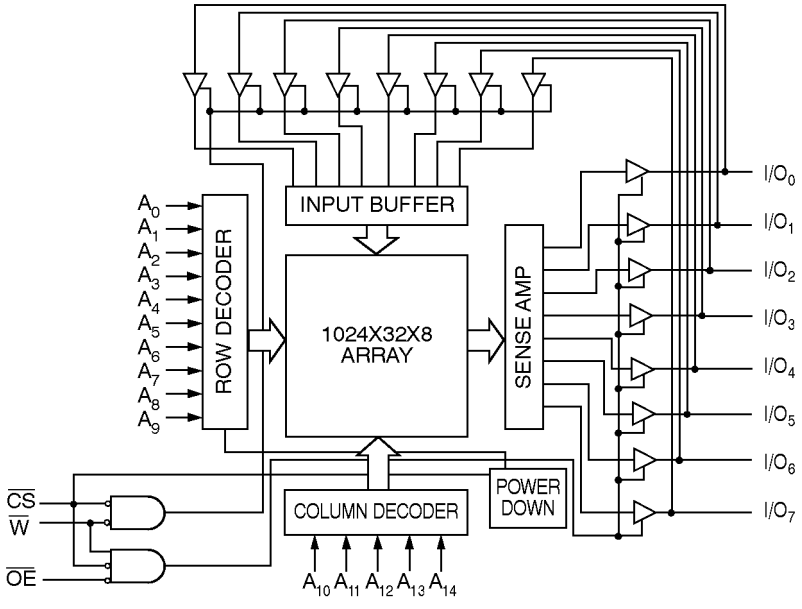
For military application the HM 65756 is processed according to the methods of the latest revision of the MIL STD 883.

Features

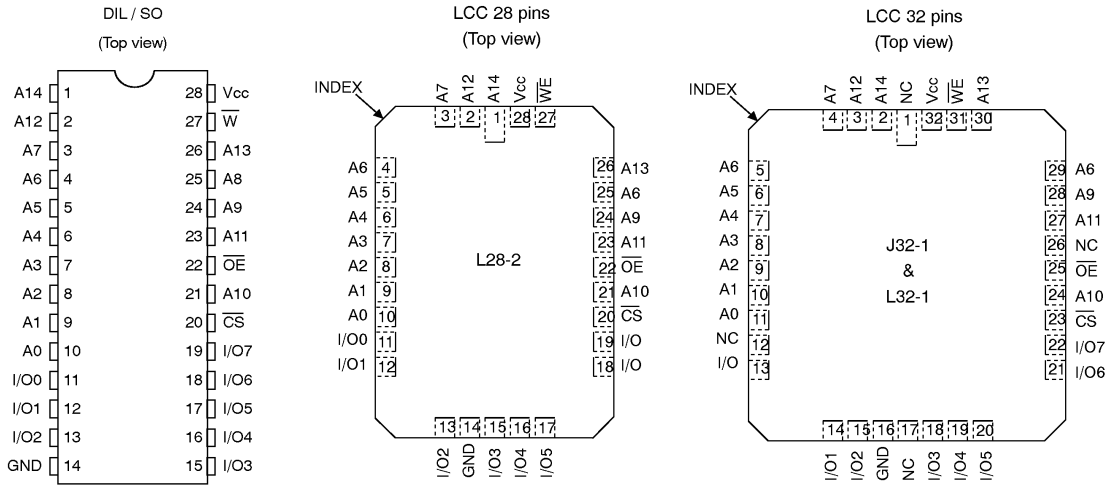
- Fast access time
  Commercial : 15/20/25/35/45 ns
  Industrial : 20/25/35/45 ns
  Automotive/military : 25/35/45 ns
- Low power consumption
  Active : 880 mW
  Standby : 220 mW
- Wide temperature range :
  – 55°C to + 125°C
- 300 and 600 mils width package
- TTL compatible inputs and outputs
- Asynchronous
- Capable of withstanding greater than 2 000 V electrostatic discharge
- Output enable
- Single 5 volt supply
- 3.3 v versions are also available. please consult sales

Interface

Block Diagram



Pin Configuration



Pin Names

A0–A14: Address inputs		$\overline{CS}$	: Chip-select
I/00–I/07	: Inputs/Outputs	$\overline{OE}$	: Output enable
VCC	: Power	$\overline{W}$	: Write Enable
GND	: Ground		

Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{W}$	INPUT/OUTPUT	MODE
H	X	X	Z	Deselect/ Power down
L	L	H	Output	Read
L	X	L	Input	Write
L	H	H	Z	Output Disable

L = Low, H = High, X = H or L, Z = High impedance.

Electrical Characteristics

Absolute Maximum Ratings

Supply voltage to GND potential : . . . . . –0.5 V to +7.0 V
DC input voltage : . . . . . –3.0 V to +7.0 V
DC output voltage in high Z state : . . . . . –0.5 V to +7.0 V

Storage temperature : . . . . . –65°C to +150°C
Output current into outputs (low) : . . . . . 20 mA
Electro Static Discharge Voltage . . . . . > 2000 V
(MIL STD 883 METHOD 3015)

Operating Range

		OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	(– 2)	5 V ± 10 %	– 55°C to + 125°C
Automotive	(– A)	5 V ± 10 %	– 40°C to + 125°C
Industrial	(– 9)	5 V ± 10 %	– 40°C to + 85°C
Commercial	(– 5)	5 V ± 10 %	– 0°C to + 70°C

DC Operating Conditions

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply Voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL	Input low voltage	– 0.3	0.0	0.8	V
VIH	Input high voltage	2.2	–	VCC	V

DC Parameters

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX	(2)	Input leakage current	– 10.0	–	10.0	µA
IOZ	(2)	Output leakage current	– 10.0	–	10.0	µA
IOS	(3)	Output short circuit current	–	–	– 300.0	mA
VOL	(4)	Output low voltage	–	–	0.4	V
VOH	(5)	Output high voltage	2.4	–	–	V

Note : 2. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
3. Vcc = max, Vout = Gnd, duration of the short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.
4. Vcc min, IOL = 8.0 mA.
5. Vcc min, IOH = –4.0 mA.

Consumption for Commercial (–5) Specification

SYMBOL		PARAMETER	65756 E–5	65756 F–5	65756 H–5	65756 K–5	65756 M–5	UNIT	VALUE
ICCSB	(6)	Standby supply current	30	40	35	35	35	mA	max
ICCSB1	(7)	Standby supply current	10	20	20	20	20	mA	max
ICCOP	(8)	Dynamic operating current	155	160	160	150	150	mA	max

Consumption for Automotive (–A), Industrial (–9) and Military (–2) Specification

SYMBOL		PARAMETER	65756 F–9	65756 H–9/–2 /–A	65756 K–9/–2 /–A	65756 M–9/–2 /–A	UNIT	VALUE
ICCSB	(6)	Standby supply current	40	35	35	35	mA	max
ICCSB1	(7)	Standby supply current	20	20	20	20	mA	max
ICCOP	(8)	Dynamic operating current	170	170	160	160	mA	max

Note : 6. $\overline{CS} \geq$ VIH, a pull-up resistor to Vcc on the $\overline{CS}$ is required to keep the device unselected during the Vcc power-up. Otherwise IccSB will exceed the above values. Min duty cycle = 100 %.
7. $\overline{CS} \geq V_{CC} - 0.3$ V, $V_{IN} - 0.3$ V or $V_{IN} \leq 0.3$ V.
8. V_{CC} max, Output current = 0 mA, f = max, Vin = Vcc or Gnd.

Capacitance

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin	(1)	Input capacitance	–	–	5	pF
Cout	(1)	Output capacitance	–	–	7	pF

Note : 1. TA = 25°C, f = 1 MHz, Vcc = 5.0 V, these parameters are not tested.

AC Parameters

Input pulse levels : . . . . . Gnd to 3.0 V
Input rise : . . . . . ≤ 5 ns
Input timing reference levels : . . . . . 1.5 V
Output loading IOL/IOH *(see figure 1a and 1b)* : . . . . . +30 pF

AC Test Loads and Waveforms

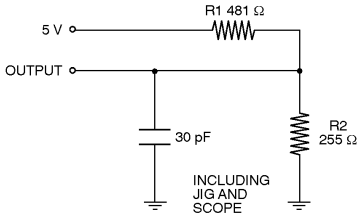


Figure 1 a

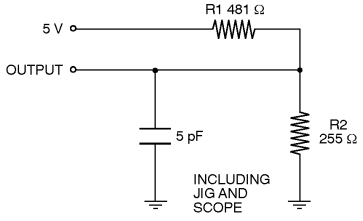


Figure 1 b

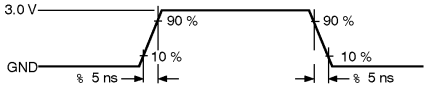
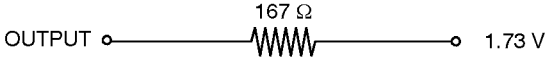


Figure 2

Equivalent to : THEVENIN EQUIVALENT

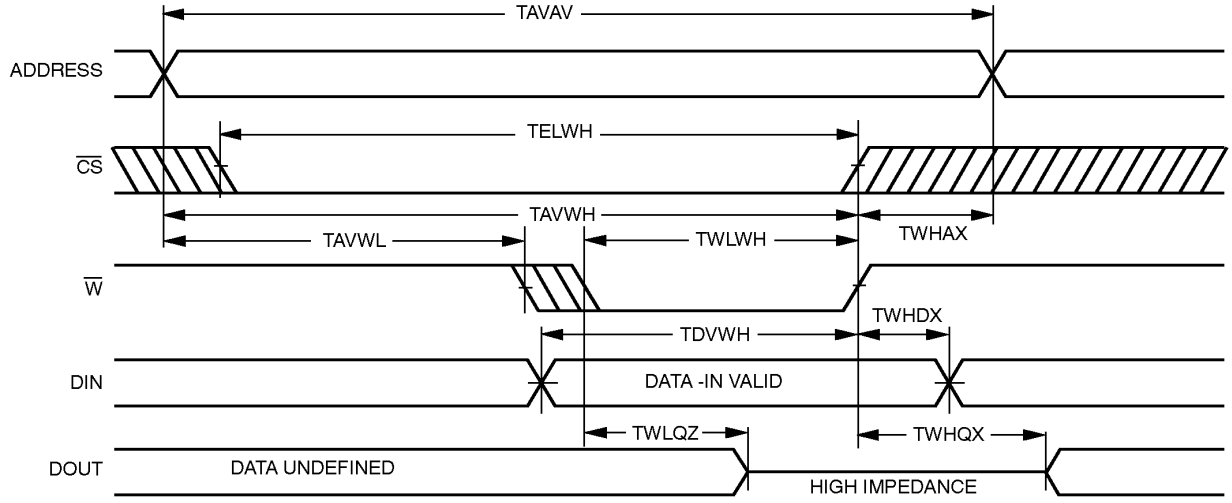


Write Cycle Specification : Automotive, Commercial, Industrial and Military (note 9)

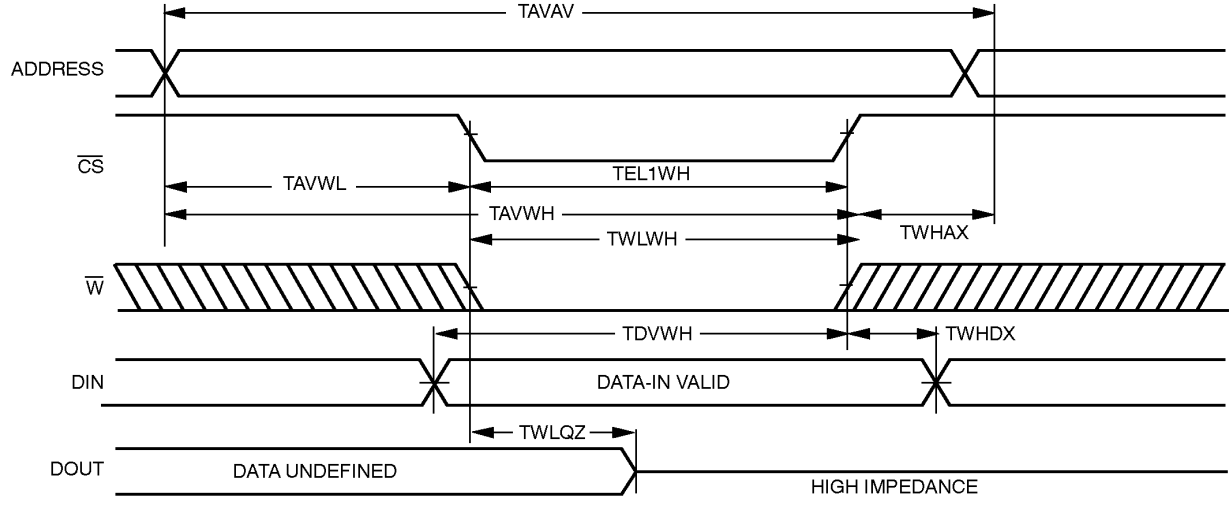
SYMBOL	PARAMETER	65756 E–5	65756 F–5/–9	65756 H–5–9/ –2/–A	65756 K–5/–9/ –2/–A	65756 M–5/–9/ –2/–A	UNIT	VALUE
TAVAV	Write cycle time	15	20	25	35	45	ns	min
TAVWL	Address set–up time	0	0	0	0	0	ns	min
TAVWH	Address Valid to write end	10	15	20	30	40	ns	min
TDVWH	Data set–up time	9	10	15	17	20	ns	min
TELWH	$\overline{CS}$ low to write end	10	15	20 (*)	30	40	ns	min
TWLQZ(8)	Write low to high Z	7	10	13	15	20	ns	max
TWLWH	Write pulse width	9	15	20 (*)	25	30	ns	min
TWHAX	Address hold from write end	0	0	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	0	0	ns	min
TWHQX (8)	Write high to low Z	3	3	3	3	3	ns	min

Note : 8. Specified with CL = 5 pF (see figure 1b).
(*) For commercial (–5) and PDIL, package value is 16 ns.

Write Cycle 1 : $\overline{W}$ Controlled (note 9)



Write Cycle 2 : $\overline{CS}$ controlled (note 9)



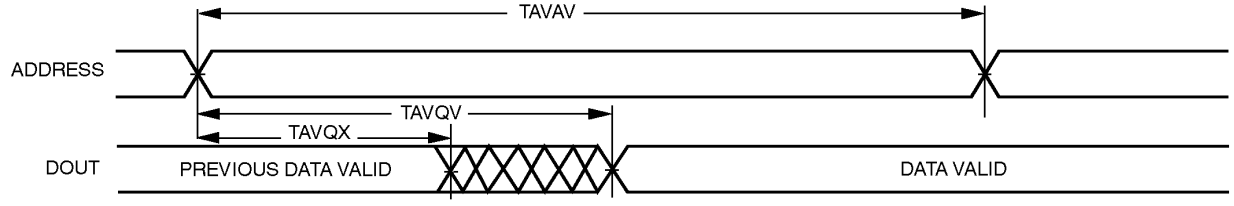
Note : 9. The internal write of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to rising edge of the signal that terminates the write.
Data out will be high impedance if $\overline{OE}$ = VIH.

Read Cycle Specification : Automotive, Commercial, Industrial and Military

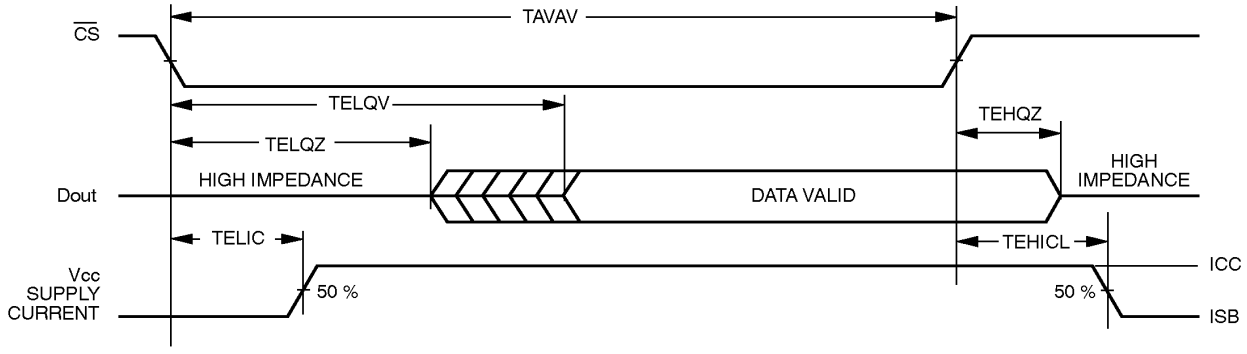
SYMBOL	PARAMETER	65756 E–5	65756 F–5/–9	65756 H–5–9/ –2/–A	65756 K–5/–9 –2/–A	65756 M–5/–9 –2/–A	UNIT	VALUE
TAVAV	Read cycle time	15	20	25	35	45	ns	min
TAVQV	Address access time	15	20	25	35	45	ns	max
TAVQX (10)	Address valid to low Z	3	3	3	3	3	ns	min
TELQV	Chip–select access time	15	20	25	35	45	ns	max
TELQX (10)	$\overline{CS}$ low to low Z	3	3	3	3	3	ns	min
TEHQZ (10)	$\overline{CS}$ high to high Z	7	10	13	15	20	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	15	20	20	20	25	ns	max
TGLQV	Output Enable access time	7	10	15	20	20	ns	max
TGLQX (10)	$\overline{OE}$ low to low Z	0	0	3	3	3	ns	min
TGHQZ (10)	$\overline{OE}$ high to high Z	7	10	13	15	20	ns	max

Note : 10. Specified with CL = 5 pF (see figure 1b).

Read Cycle 1 (note 11, 12, 13)

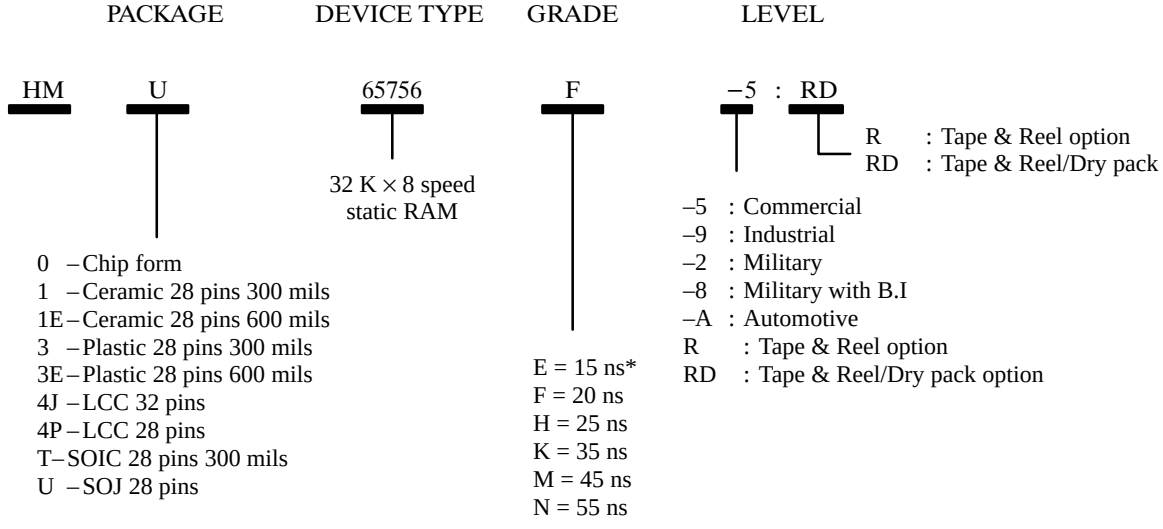


Read Cycle 2 (note 11, 13)



Notes : 11. $\overline{W}$ is high for read cycle.
12. Device is continuously selected, $\overline{CS}$ = VIL, $\overline{OE}$ = VIL.
13. Address valid prior or coincident with $\overline{CS}$ transition low.

Ordering Information



* available in commercial range on PDIL.3 (code 3) and SOJ (code U). For other package please consult your sales office.