

## Description

The μPD41257 is a 262,144-word by 1-bit dynamic NMOS RAM designed to operate from a single +5-volt power supply. A double-polylayer N-channel silicon gate fabrication process provides for high storage cell density, high performance, and high reliability. The device also uses a single-transistor dynamic storage cell and advanced dynamic circuitry, including 1024 sense amplifiers, which ensure that power dissipation is minimized. The negative voltage substrate bias is automatically generated internally.

The three-state output is controlled by  $\overline{\text{CAS}}$  independent of RAS. Nibble mode read or write cycles are available by cycling  $\overline{\text{CAS}}$ .

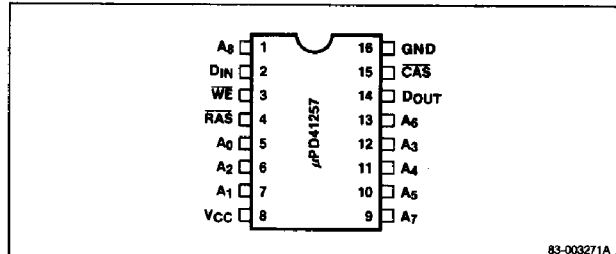
Refreshing is initiated by a  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  cycle that enables internal generation of the refresh address. Refreshing is also accomplished by means of  $\overline{\text{RAS}}$ -only refresh cycles, hidden refresh cycles, or by normal read or write cycles on the 256 address combinations of A<sub>0</sub>-A<sub>7</sub> during a 4-ms period.

## Features

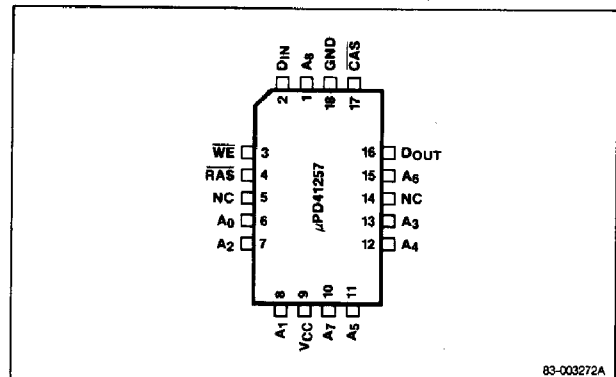
- 262,144-word x 1-bit organization
- Multiplexed address inputs
- Single +5-volt ±10% power supply
- Nibble read, write, or read-modify-write cycles
- $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  internal refreshing
- Low power dissipation
  - 28 mW max (standby)
  - 413 mW max (active, t<sub>RC</sub> = 220 ns)
- Nonlatched, three-state output
- TTL-compatible inputs with low input capacitance
- 256-cycle/4-ms refresh period (A<sub>0</sub>-A<sub>7</sub> are refresh addresses)
- High-density plastic DIP and PLCC packaging

## Pin Configurations

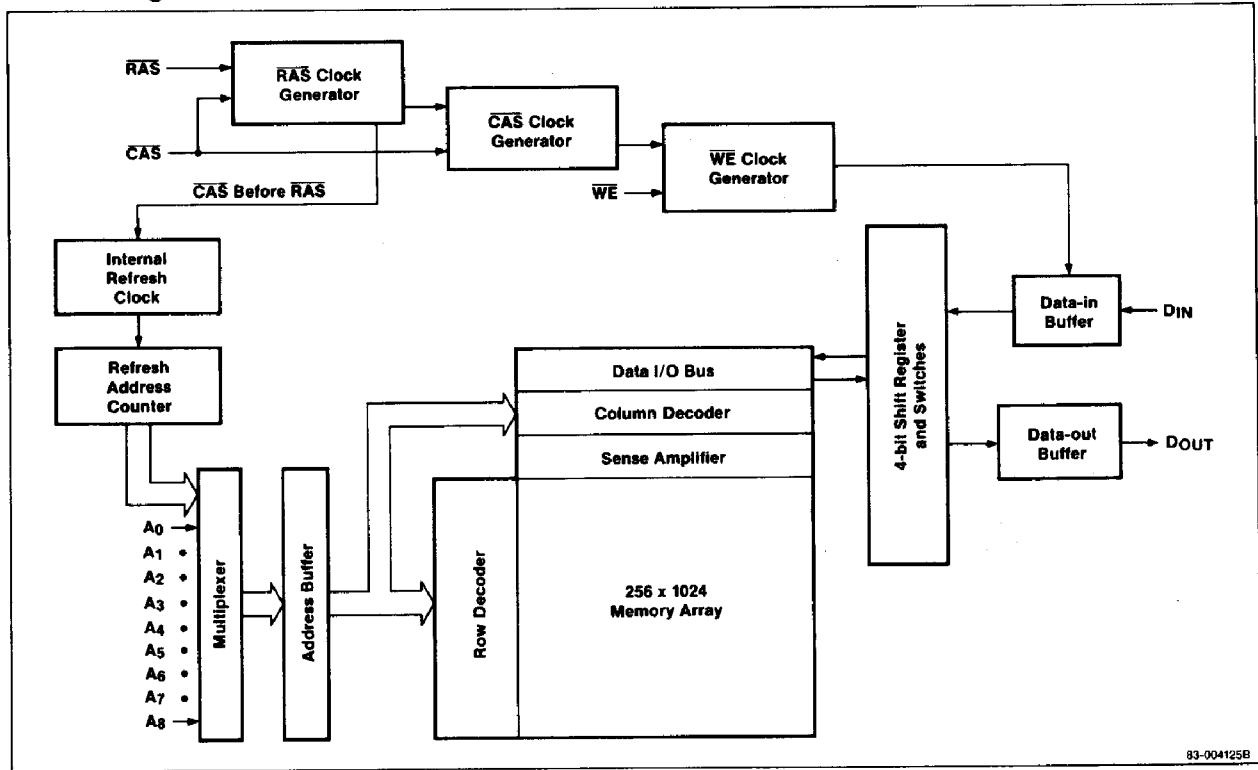
### 16-Pin Plastic DIP



### 18-Pin Plastic Leaded Chip Carrier (PLCC)



**Block Diagram**



**Pin Identification**

Symbol	Function
A <sub>0</sub> -A <sub>8</sub>	Address inputs
D <sub>IN</sub>	Data input
D <sub>OUT</sub>	Data output
WE	Write enable
RAS	Row address strobe
CAS	Column address strobe
GND	Ground
V <sub>CC</sub>	+5.0-volt power supply

**Capacitance**

T<sub>A</sub> = 0 to +70°C; V<sub>CC</sub> = +5.0 V ±10%

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Input capacitance	C <sub>11</sub>		5		pF	A <sub>0</sub> -A <sub>8</sub> , D <sub>IN</sub>
	C <sub>12</sub>		8		pF	RAS, CAS, WE
Output capacitance	C <sub>0</sub>		7		pF	D <sub>OUT</sub>

**Absolute Maximum Ratings**

Voltage on any pin relative to GND	-1.0 to +7.0 V
Short-circuit output current	50 mA
Power dissipation, P <sub>D</sub>	1 W
Operating temperature, T <sub>A</sub>	0 to +70°C
Storage temperature, T <sub>STG</sub>	-55 to +150°C

**Comment:** Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

**Ordering Information**

Part Number	Access Time (max)	R/W Cycle (min)	Package
μPD41257C-12	120 ns	220 ns	16-pin plastic DIP
C-15	150 ns	260 ns	
C-20	200 ns	330 ns	
μPD41257L-12	120 ns	220 ns	18-pin PLCC
L-15	150 ns	260 ns	
L-20	200 ns	330 ns	

## DC Characteristics

$T_A = 0$  to  $+70^\circ\text{C}$ ;  $V_{CC} = 5.0\text{ V} \pm 10\%$ ;  $\text{GND} = 0\text{ V}$

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Standby power supply current	$I_{CC2}$			5	mA	$\overline{\text{RAS}} = V_{IH}$ ; $D_{OUT} = \text{high impedance}$
Input leakage current	$I_{I(L)}$	-10		10	μA	Any input $V_{IN} = 0\text{ V}$ to $V_{CC}$ ; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	-10		10	μA	$D_{OUT}$ disabled; $V_{OUT} = 0$ to 5.5 V
Output voltage, high	$V_{OH}$	2.4		$V_{CC}$	V	$I_{OUT} = -5\text{ mA}$
Output voltage, low	$V_{OL}$	0		0.4	V	$I_{OUT} = 4.2\text{ mA}$
Supply voltage	$V_{CC}$	4.5	5.0	5.5	V	
	GND	0	0	0	V	
Input voltage, high	$V_{IH}$	2.4		5.5	V	All inputs
Input voltage, low	$V_{IL}$	-1.0		0.8	V	All inputs

## AC Characteristics

$T_A = 0$  to  $+70^\circ\text{C}$ ;  $V_{CC} = 5.0\text{ V} \pm 10\%$

Parameter	Symbol	Limits						Unit	Test Conditions
		μPD41257-12		μPD41257-15		μPD41257-20			
		Min	Max	Min	Max	Min	Max		
<b>Standard Operation</b>									
Average power supply operating current	$I_{CC1}$		75		70		60	mA	$\overline{\text{RAS}}, \overline{\text{CAS}}$ cycling; $t_{RC} = t_{RC\text{ min}}$ (Note 5)
Average power supply current, refresh cycle	$I_{CC3}$		60		55		55	mA	$\overline{\text{RAS}}$ cycling; $\text{CAS} = V_{IH}$ ; $t_{RC} = t_{RC\text{ min}}$ (Note 5)
Random read or write cycle time	$t_{RC}$	220		260		330		ns	(Note 6)
Read-write cycle time	$t_{RWC}$	265		310		390		ns	(Note 6)
Access time from $\overline{\text{RAS}}$	$t_{RAC}$		120		150		200	ns	(Notes 7, 8)
Access time from $\overline{\text{CAS}}$	$t_{CAC}$		60		75		100	ns	(Notes 7, 9)
Output buffer turnoff delay	$t_{OFF}$	0	30	0	40	0	50	ns	(Note 10)
Rise and fall transition time	$t_T$	3	50	3	50	3	50	ns	(Note 4)
$\overline{\text{RAS}}$ precharge time	$t_{RP}$	90		100		120		ns	
$\overline{\text{RAS}}$ pulse width	$t_{RAS}$	120	10,000	150	10,000	200	10,000	ns	
$\overline{\text{RAS}}$ hold time	$t_{RSH}$	60		75		100		ns	
$\overline{\text{CAS}}$ pulse width	$t_{CAS}$	60	10,000	75	10,000	100	10,000	ns	
$\overline{\text{CAS}}$ hold time	$t_{CSH}$	120		150		200		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	$t_{RCD}$	25	60	25	75	35	100	ns	(Note 11)
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	$t_{CRP}$	10		10		10		ns	(Note 12)
$\overline{\text{CAS}}$ precharge time	$t_{CPN}$	30		30		35		ns	
$\overline{\text{RAS}}$ precharge $\overline{\text{CAS}}$ hold time	$t_{RPC}$	0		0		0		ns	
Row address setup time	$t_{ASR}$	0		0		0		ns	

**AC Characteristics (cont)**

Parameter	Symbol	μPD41257-12		μPD41257-15		μPD41257-20		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
<b>Standard Operation (cont)</b>									
Row address hold time	t <sub>RAH</sub>	15		15		25		ns	
Column address setup time	t <sub>ASC</sub>	0		0		0		ns	
Column address hold time	t <sub>CAH</sub>	20		25		55		ns	
Column address hold time referenced to RAS	t <sub>AR</sub>	80		100		155		ns	
Read command setup time	t <sub>RCS</sub>	0		0		0		ns	
Read command hold time referenced to RAS	t <sub>RRH</sub>	10		10		25		ns	(Note 13)
Read command hold time referenced to CAS	t <sub>RCH</sub>	0		0		0		ns	(Note 13)
Write command hold time	t <sub>WCH</sub>	30		40		55		ns	
Write command hold time referenced to RAS	t <sub>WCR</sub>	90		115		155		ns	
Write command pulse width	t <sub>WP</sub>	20		25		55		ns	
Write command to RAS lead time	t <sub>RWL</sub>	40		45		55		ns	
Write command to CAS lead time	t <sub>CWL</sub>	40		45		55		ns	
Data-in setup time	t <sub>DS</sub>	0		0		0		ns	(Note 14)
Data-in hold time	t <sub>DH</sub>	30		40		55		ns	(Note 14)
Data-in hold time referenced to RAS	t <sub>DHR</sub>	90		115		155		ns	
Refresh period	t <sub>REF</sub>		4		4		4	ms	
WE command setup time	t <sub>WCS</sub>	0		0		0		ns	(Note 15)
CAS to WE delay	t <sub>CWD</sub>	60		75		100		ns	(Note 15)
RAS to WE delay	t <sub>RWD</sub>	120		150		200		ns	(Note 15)
<b>Nibble Mode</b>									
Average power supply current, nibble mode	I <sub>CC6</sub>		35		27		27	mA	RAS = V <sub>IL</sub> ; CAS cycling; t <sub>NC</sub> = t <sub>NC</sub> min (Note 5)
Nibble-mode cycle time	t <sub>NC</sub>	60		70		100		ns	(Note 6)
Nibble-mode access time	t <sub>NAC</sub>		30		35		50	ns	(Note 7)
Nibble-mode precharge time	t <sub>NP</sub>	20		25		40		ns	
Nibble-mode WE pulse width	t <sub>NWP</sub>	20		25		40		ns	
Nibble-mode CAS pulse width	t <sub>NAS</sub>	30		35		50		ns	
Nibble-mode RAS hold time (read cycle)	t <sub>NRRSH</sub>	30		35		50		ns	
Nibble-mode RAS hold time (write cycle)	t <sub>NWRSH</sub>	35		35		50		ns	
Nibble-mode CAS to WE delay	t <sub>NCWD</sub>	30		35		50		ns	
Nibble-mode WE to CAS lead time	t <sub>NCWL</sub>	30		35		50		ns	

## AC Characteristics (cont)

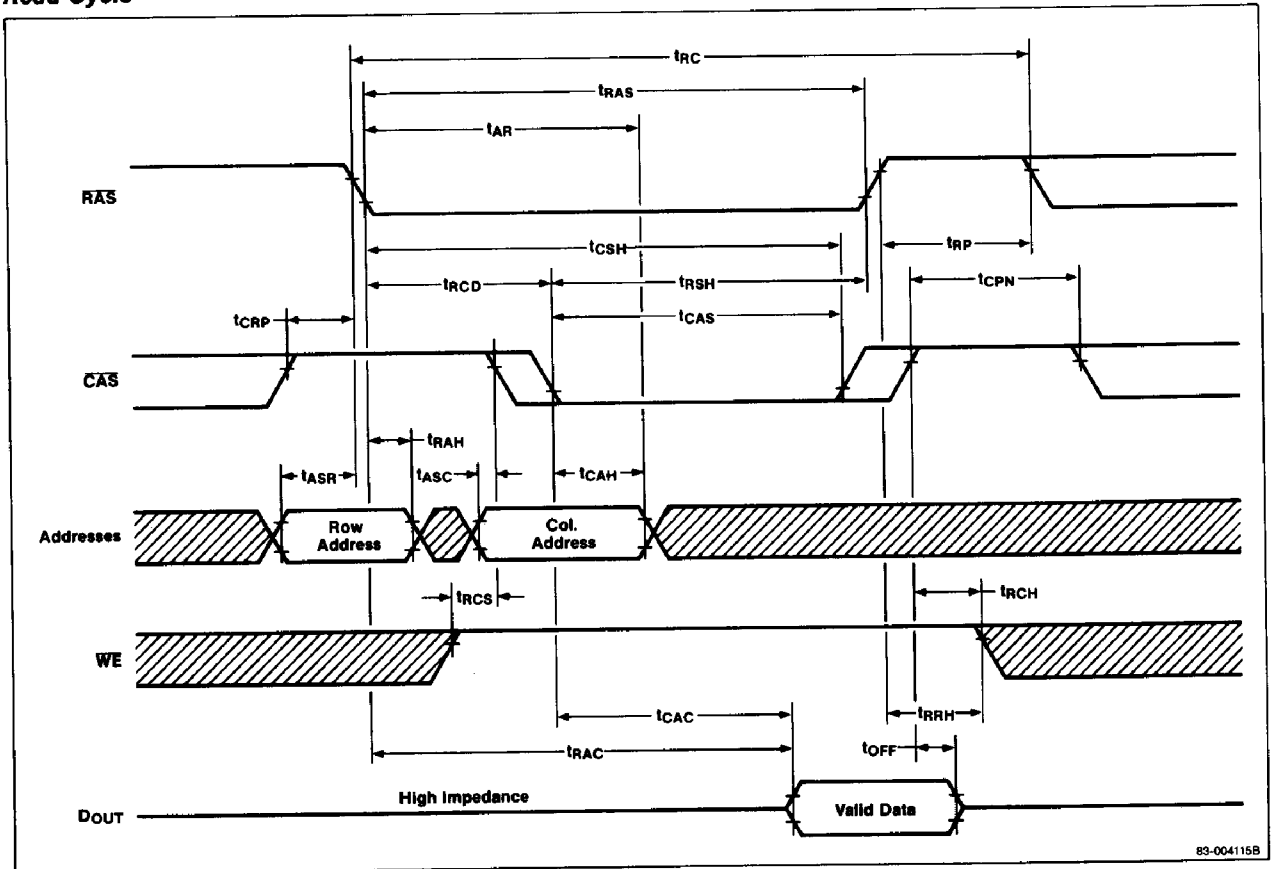
Parameter	Symbol	μPD41257-12		μPD41257-15		μPD41257-20		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
<b>CAS Before RAS Refresh Cycle</b>									
Average power supply current, CAS before RAS refreshing	$I_{CC4}$		65	60		55		mA	RAS cycling; $\overline{CAS} = V_{IL}$ ; $t_{RC} = t_{RC \text{ min}}$ (Note 5)
CAS setup time for CAS before RAS refreshing	$t_{CSR}$	10		10		10		ns	
CAS hold time for CAS before RAS refreshing	$t_{CHR}$	25		30		30		ns	
Read or write cycle time (counter test cycle)	$t_{TRC}$	245		285		350		ns	
Read-write cycle time (counter test cycle)	$t_{TRWC}$	290		335		410		ns	
CAS precharge time (counter test cycle)	$t_{TCP}$	50		60		80		ns	

### Notes:

- (1) An initial pause of 100 μs is required after power-up, followed by any eight RAS cycles before proper device operation is achieved.
- (2) Ac measurements assume  $t_T = 5$  ns.
- (3)  $V_{IH}$  (min) and  $V_{IL}$  (max) are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
- (4) All voltages are referenced to GND.
- (5)  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$ , and  $I_{CC6}$  depend on output loading and cycle rates. Specified values are obtained with the output open.
- (6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range ( $T_A = 0$  to  $+70^\circ\text{C}$ ) is assured.
- (7) Load = 2 TTL loads and 100 pF.
- (8) Assumes that  $t_{RCD} \leq t_{RCD}(\text{max})$ . If  $t_{RCD}$  is greater than the maximum recommended value in this table,  $t_{RAC}$  increases by the amount that  $t_{RCD}$  exceeds the value shown. For the CAS before RAS refresh counter test cycle,  $t_{RAC}$  is specified as  $t_{RAC} = t_{CHR} + t_{TCP} + t_{CAC} + 2t_T$  and is greater than the maximum specified value shown in this table.
- (9) Assumes that  $t_{RCD} \geq t_{RCD}(\text{max})$ .
- (10)  $t_{OFF}(\text{max})$  defines the time at which the output achieves the open-circuit condition and is not referenced to  $V_{OH}$  or  $V_{OL}$ .
- (11) Operation within the  $t_{RCD}(\text{max})$  limit assures that  $t_{RAC}(\text{max})$  can be met. Time  $t_{RCD}(\text{max})$  is specified as a reference point only; if  $t_{RCD}$  is greater than  $t_{RCD}(\text{max})$ , access time is controlled exclusively by  $t_{CAC}$ .
- (12) The  $t_{CRP}$  requirement should be applicable for  $\overline{RAS}/\overline{CAS}$  cycles preceded by any cycle.
- (13) Either  $t_{RRH}$  or  $t_{RCH}$  must be satisfied for a read cycle.
- (14) These parameters are referenced to the leading edge of  $\overline{CAS}$  for early write cycles and to the leading edge of  $\overline{WE}$  for delayed write or read-modify-write cycles.
- (15)  $t_{WCS}$ ,  $t_{CWD}$ ,  $t_{NCWD}$ , and  $t_{RWD}$  are restrictive operating parameters in read-write/read-modify-write cycles only.
  - If  $t_{WCS} \geq t_{WCS}(\text{min})$ , the cycle is an early write cycle or a nibble mode early write cycle and the data output pin will remain open-circuit throughout the entire cycle.
  - If  $t_{CWD} \geq t_{CWD}(\text{min})$  and  $t_{RWD} \geq t_{RWD}(\text{min})$ , the cycle is a read-write cycle and the data output pin will contain data read from the selected cell.
  - If  $t_{NCWD} \geq t_{NCWD}(\text{min})$ , the cycle is a nibble mode read-write cycle and the data output pin will contain data read from the selected cell.
  - If none of the above conditions is met, the condition of the data output pin (at access time and until  $\overline{CAS}$  returns to  $V_{IH}$ ) is indeterminate.

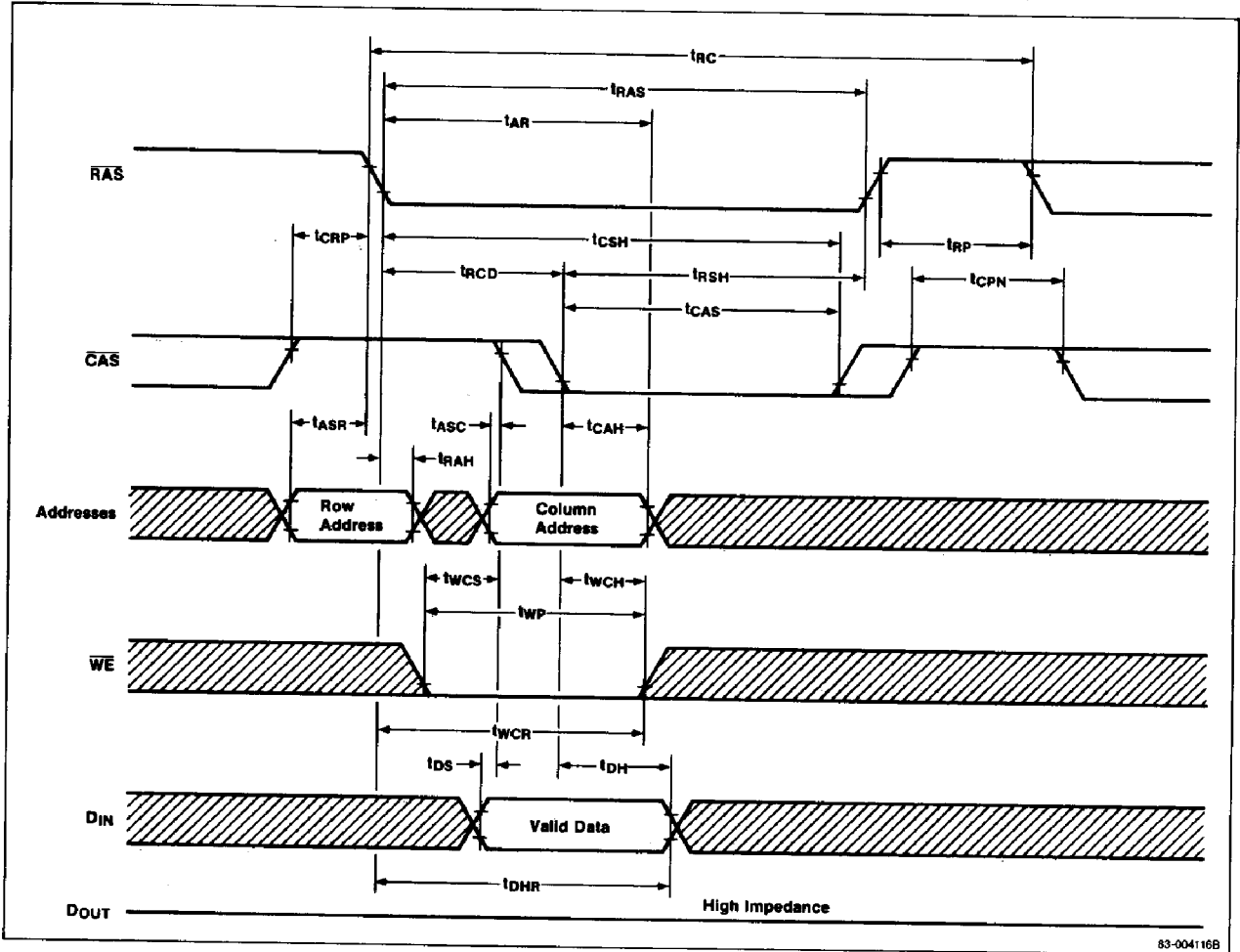
Timing Waveforms

Read Cycle



## Timing Waveforms (cont)

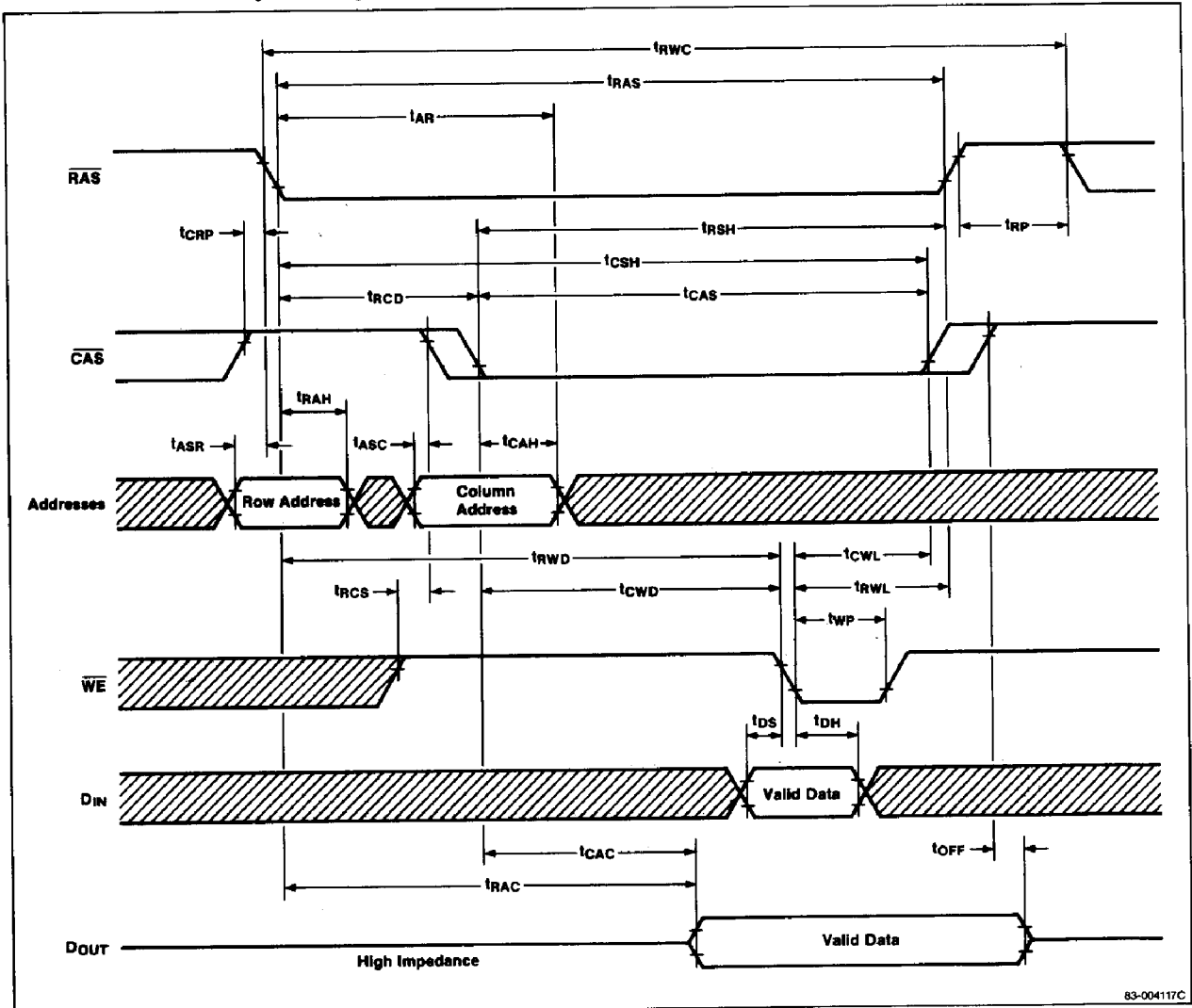
### Write Cycle (Early Write)



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Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle

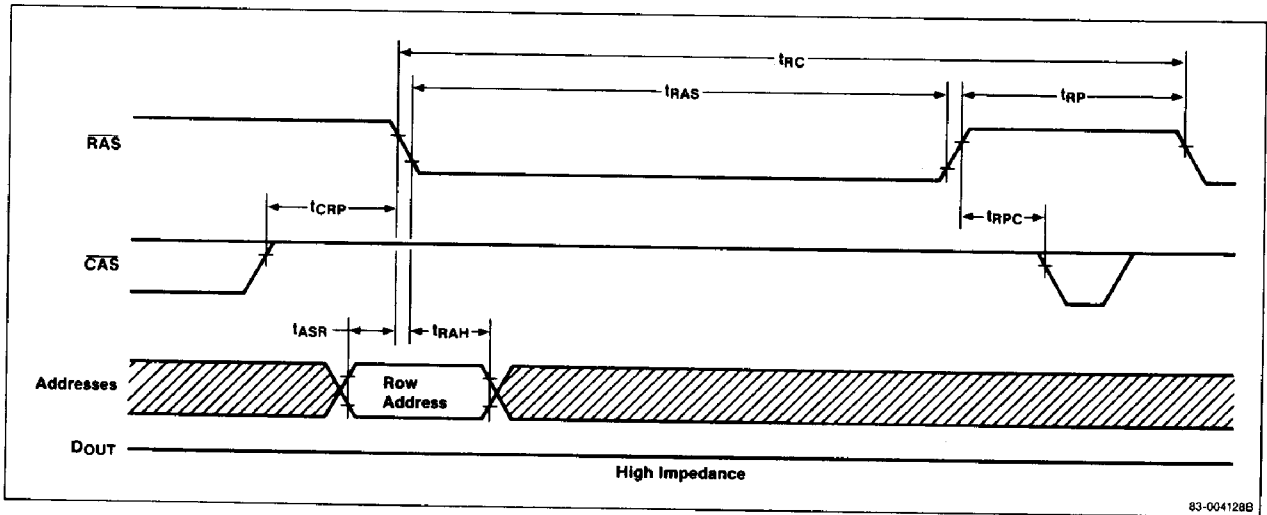


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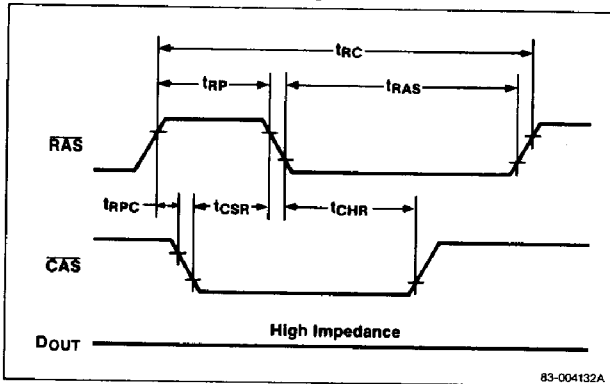


## Timing Waveforms (cont)

### $\overline{\text{RAS}}$ -Only Refresh Cycle



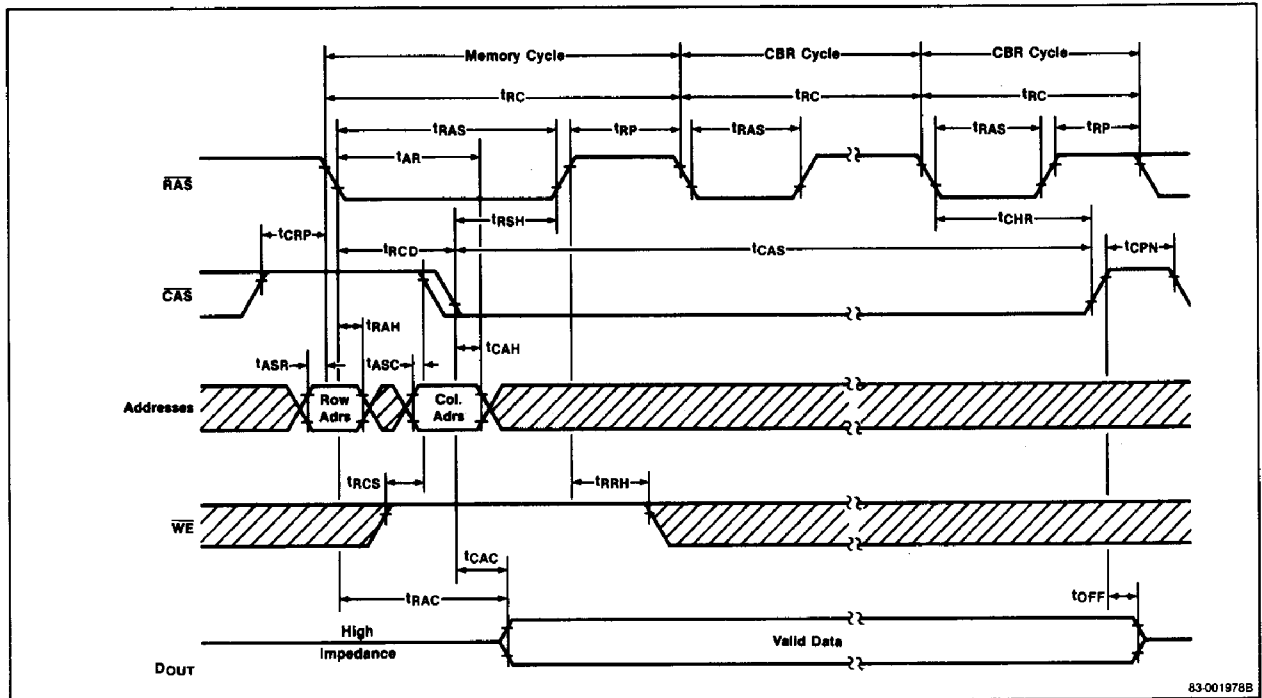
### $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle



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**Timing Waveforms (cont)**

**Hidden Refresh Cycle**



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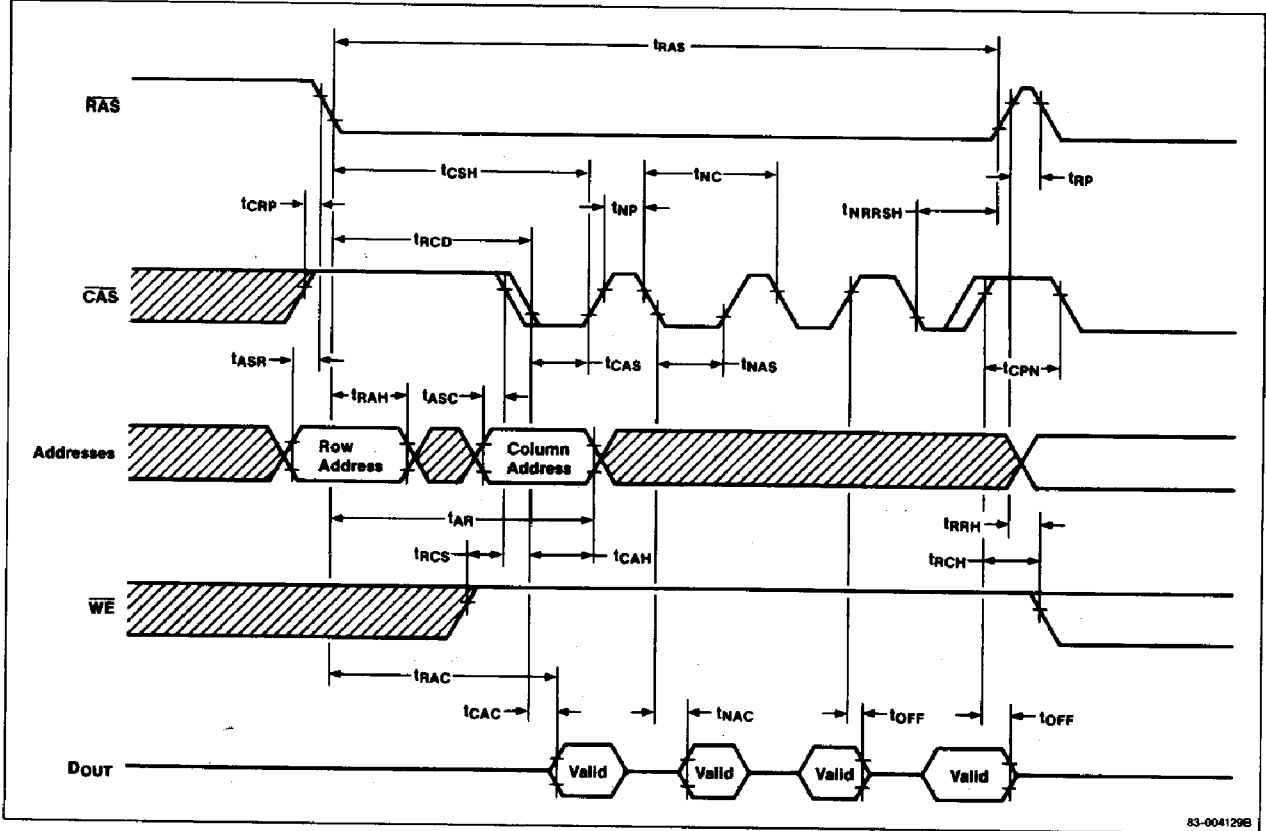
**Nibble Mode**

The μPD41257 is capable of executing nibble read, write, or read-modify-write cycles. Nibble mode allows high-speed serial access of a maximum of 4 data bits. The first bit is determined by the row and column addresses, and the next bits are accessed automatically by cycling CAS while RAS is held low. The addresses of nibble bits are determined by the combination of row address A<sub>8</sub> and column address A<sub>8</sub> in the following sequence.

Sequence	Nibble Bit	Row Address								Column Address								Comment		
		A <sub>8</sub>	A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	A <sub>8</sub>	A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>		A <sub>1</sub>	A <sub>0</sub>
RAS/CAS	1	0	1	0	0	0	1	0	1	0	0	1	0	1	0	1	0	0	0	Example: external address input
CAS cycling	2	1	1	0	0	0	1	0	1	0	0	1	0	1	0	1	0	0	0	Internal address generated
CAS cycling	3	0	1	0	0	0	1	0	1	0	1	1	0	1	0	1	0	0	0	
CAS cycling	4	1	1	0	0	0	1	0	1	0	1	1	0	1	0	1	0	0	0	
CAS cycling	1	0	1	0	0	0	1	0	1	0	0	1	0	1	0	1	0	0	0	Repeated sequence

## Timing Waveforms (cont)

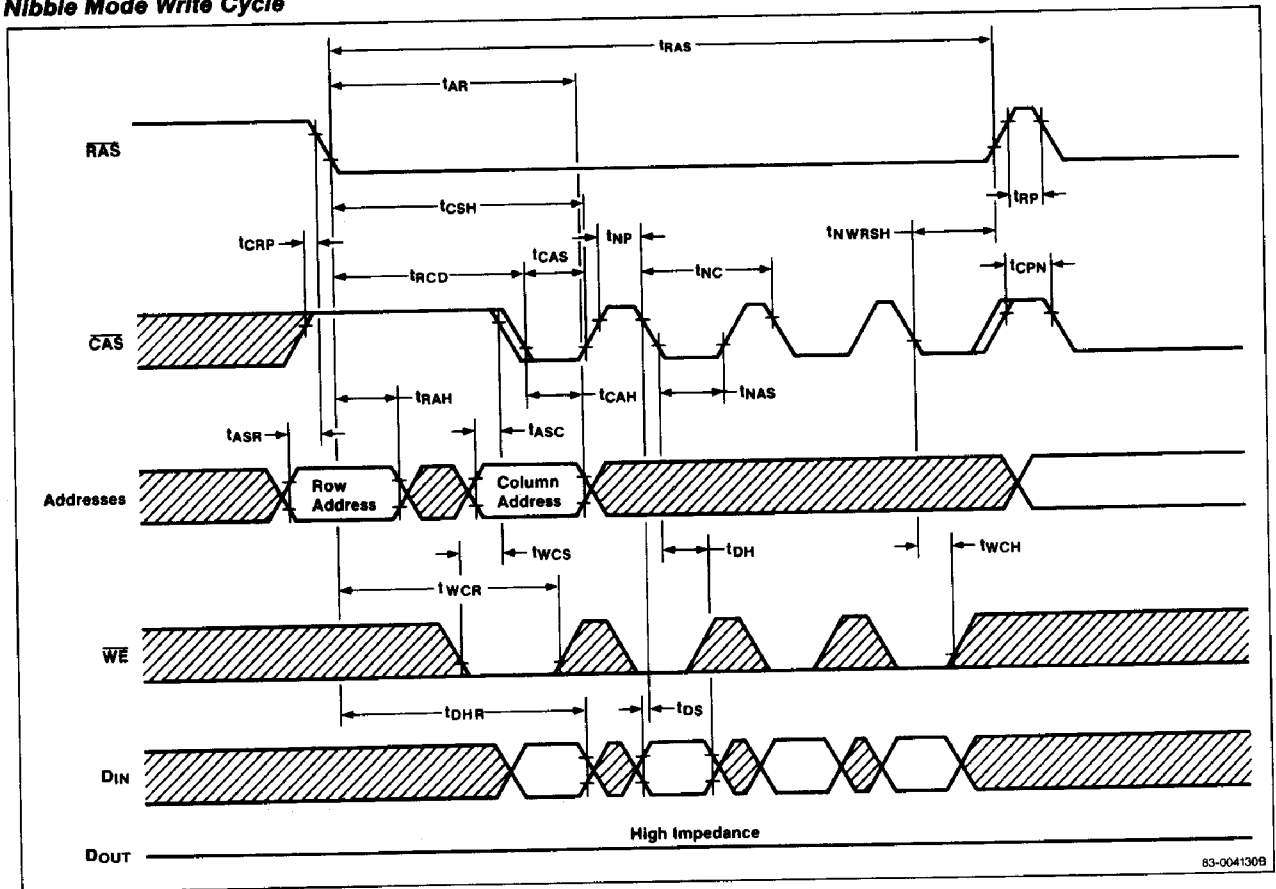
### Nibble Mode Read Cycle



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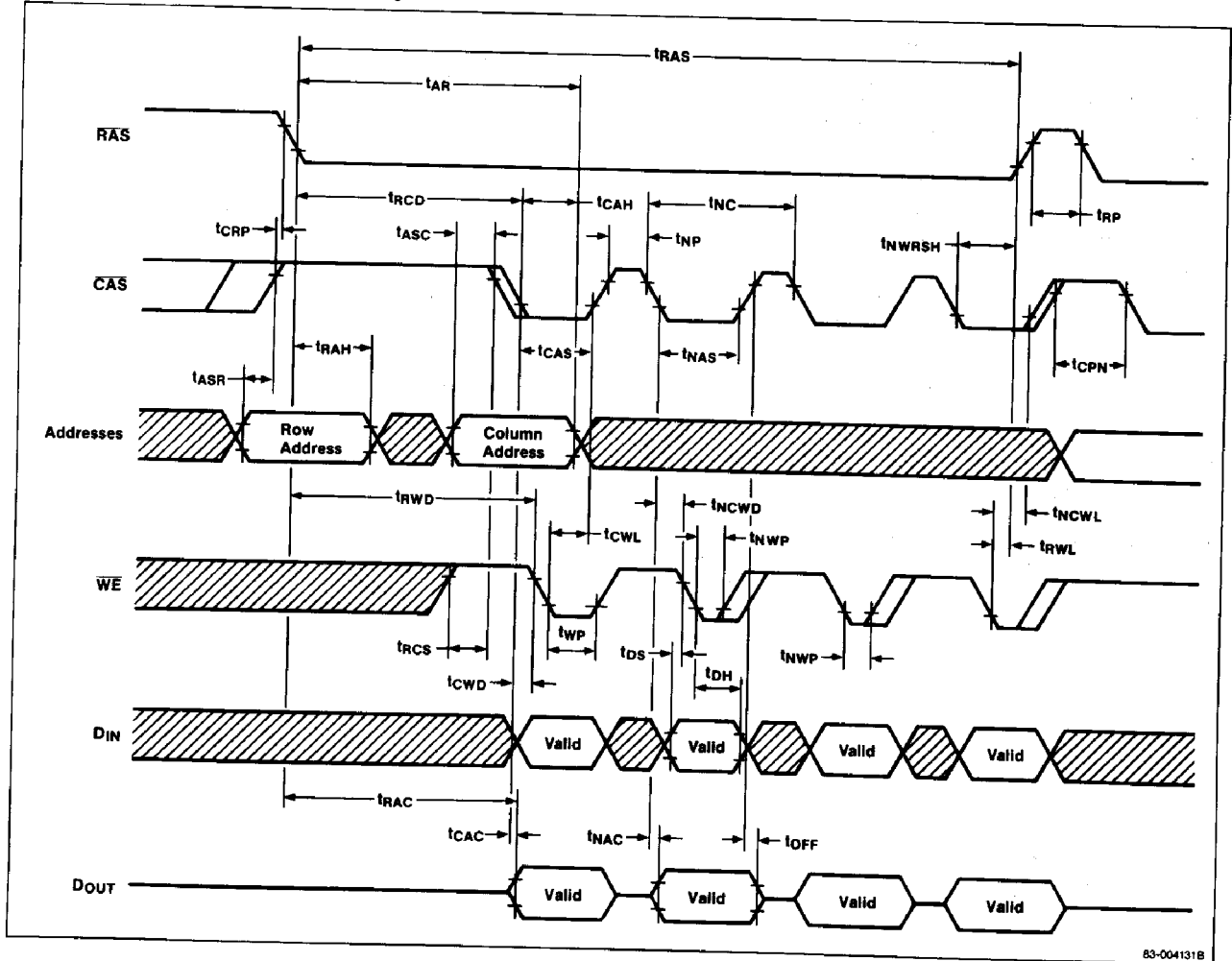
Timing Waveforms (cont)

Nibble Mode Write Cycle



## Timing Waveforms (cont)

### Nibble Mode Read-Modify-Write Cycle



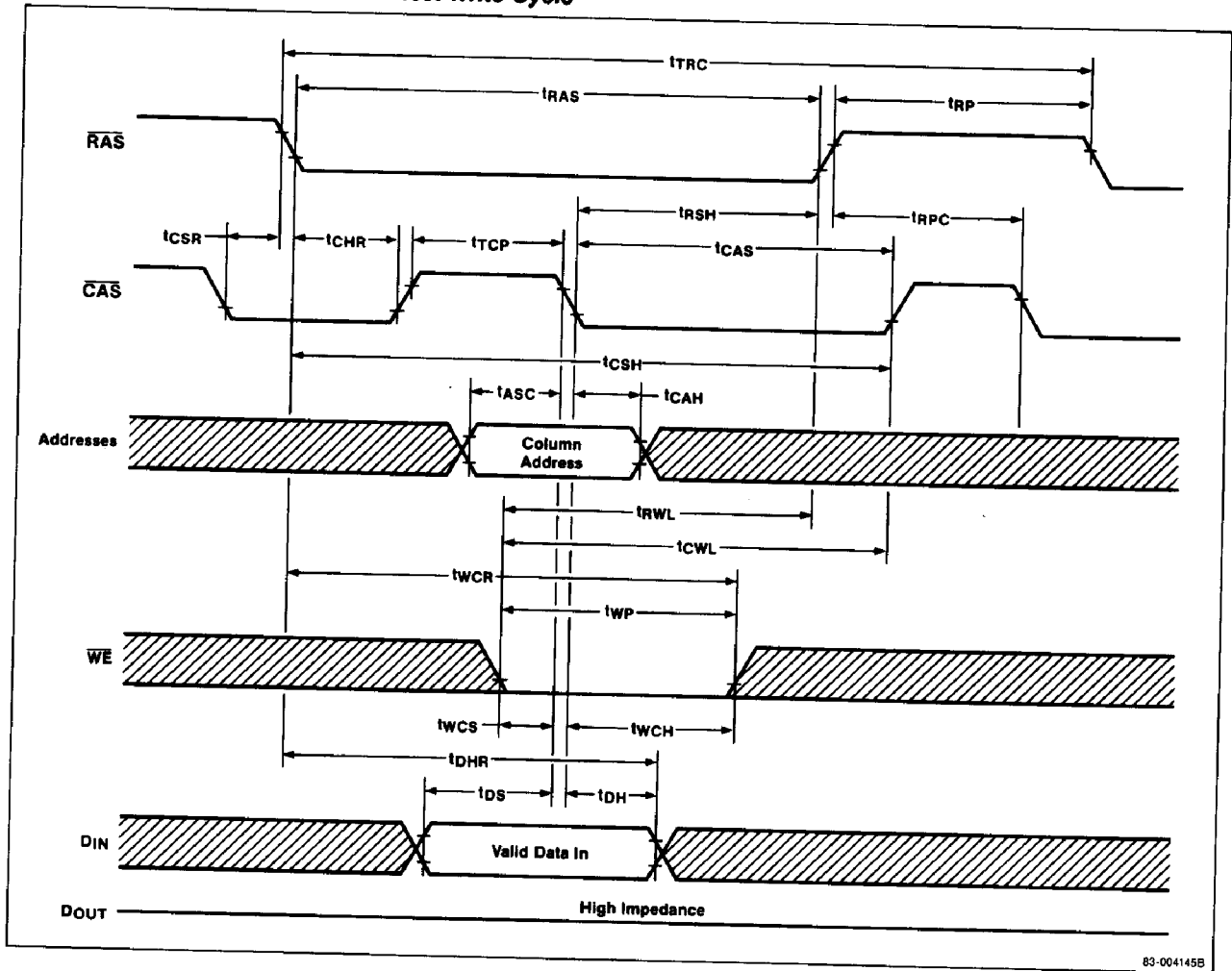
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## Timing Waveforms (cont)

### $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Counter Test Write Cycle

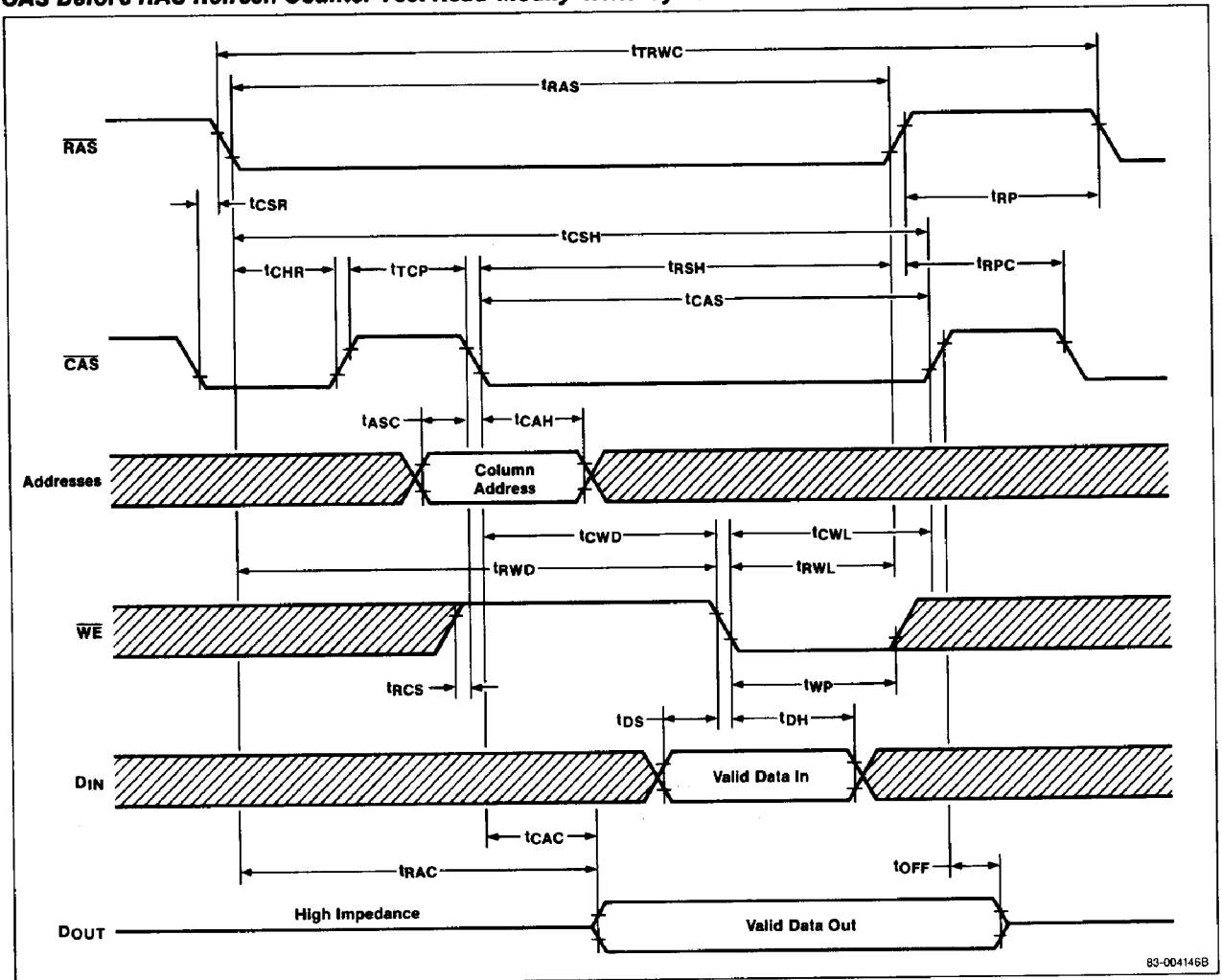


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Timing Waveforms (cont)

CAS Before RAS Refresh Counter Test Read-Modify-Write Cycle



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