PYRAMID SEMICONDUCTOR CORPORATION

P4C1026/P4C1026L

ULTRA HIGH SPEED 256K X 4 STATIC CMOS RAMS

FEATURES

- **Full CMOS, 6T Cell**
- **High Speed (Equal Access and Cycle Times)**
  - **– 15/20/25/35 ns (Commercial/Industrial)**
  - **– 20/25/35 ns (Military)**
- **Low Power**
- **Single 5V±10% Power Supply**
- **Data Retention with 2.0V Supply (P4C1026L only)**
- **Three-State Outputs**
- **TTL/CMOS Compatible Outputs**
- **Fully TTL Compatible Inputs**
- **Standard Pinout (JEDEC Approved)**
  - **– 28-Pin 300 mil SOJ**
  - **– 28-Pin 400 mil SOJ**
  - **– 28-Pin 400 mil Ceramic DIP**
  - **– 32-Pin Ceramic LCC**

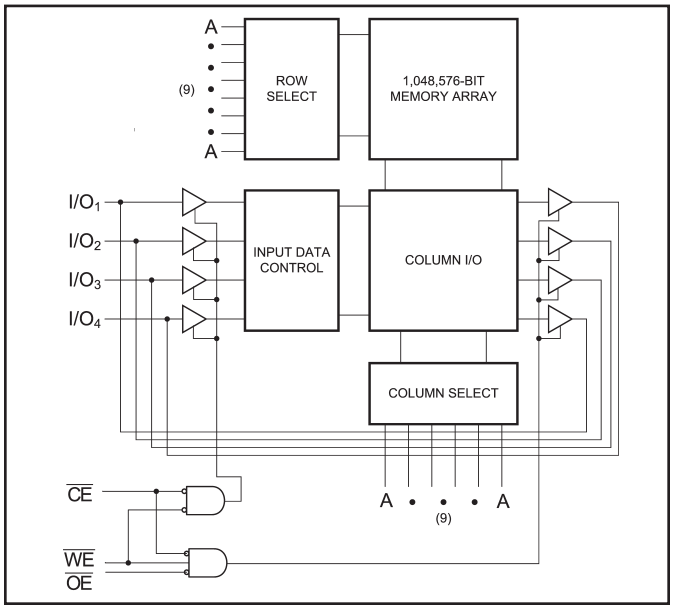
DESCRIPTION

The P4C1026/P4C1026L is a 1 Meg ultra high speed static RAM organized as 256K x 4. The CMOS memory requires no clock or refreshing and has equal access and cycle times. Inputs and outputs are fully TTL-compatible. The RAM operates from a single 5V±10% tolerance power supply. With battery backup (P4C1026L only), data integrity is maintained for supply voltages down to 2.0V.

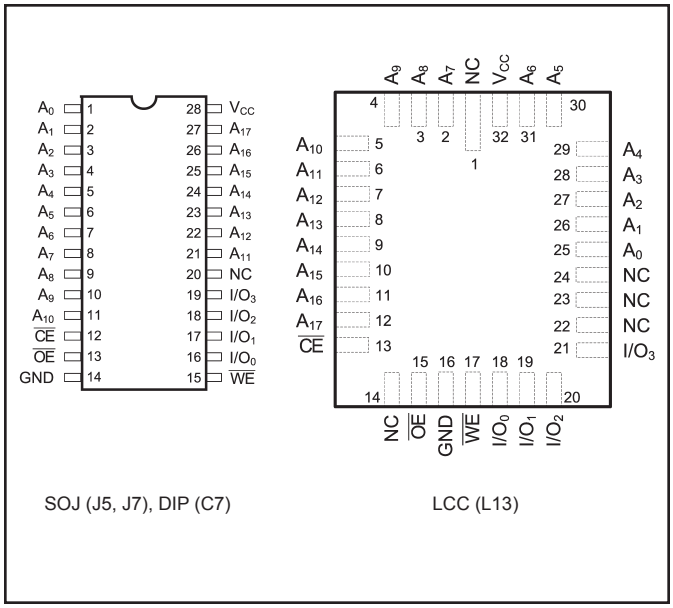
Access times as fast as 15 nanoseconds are available, permitting greatly enhanced system speeds. CMOS is utilized to reduce power consumption.

The P4C1026/P4C1026L is available in a 28-pin 300 mil and 400 mil SOJ packages, as well as Ceramic DIP and LCC packages, providing excellent board level densities.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



MAXIMUM RATINGS[1]

Sym	Parameter	Value	Unit
V_{CC}	Power Supply Pin with Respect to GND	-0.5 to +7	V
V_{TERM}	Terminal Voltage with Respect to GND (up to 7.0V)	-0.5 to VCC + 0.5	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

RECOMMENDED OPERATING CONDITIONS

Grade[2]	Ambient Temp	GND	V_{CC}
Commercial	0°C to 70°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%
Military	-55°C to +125°C	0V	5.0V ± 10%

CAPACITANCES[4]

(V_{CC} = 5.0V, T_A = 25°C, f = 1.0MHz)

Sym	Parameter	Conditions	Typ	Unit
C_{IN}	Input Capacitance	V_{IN}=0V	7	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	10	pF

DC ELECTRICAL CHARACTERISTICS

(Over Recommended Operating Temperature & Supply Voltage)[2]

Sym	Parameter	Test Conditions	P4C1026		P4C1026L		Unit
			Min	Max	Min	Max	
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.5	2.2	V_{CC} + 0.5	V
V_{IL}	Input Low Voltage		-0.5[3]	0.8	-0.5[3]	0.8	V
V_{HC}	CMOS Input High Voltage		V_{CC} - 0.2	V_{CC} + 0.5	V_{CC} - 0.2	V_{CC} + 0.5	V
V_{LC}	CMOS Input Low Voltage		-0.5[3]	0.2	-0.5[3]	0.2	V
V_{CD}	Input Clamp Diode Voltage	V_{CC} = Min, I_{IN} = -18 mA		-1.2		-1.2	V
V_{OL}	Output Low Voltage (TTL Load)	I_{OL} = +8 mA, V_{CC} = Min		0.4		0.4	V
V_{OH}	Output High Voltage (TTL Load)	I_{OH} = -4 mA, V_{CC} = Min	2.4		2.4		V
I_{LI}	Input Leakage Current	V_{CC} = Max, V_{IN} = GND to V_{CC}	-5	+5	-5	+5	µA
I_{LO}	Output Leakage Current	V_{CC} = Max, $\overline{CE}$ = V_{IH}, V_{OUT} = GND to V_{CC}	-5	+5	-5	+5	µA
I_{SB}	Standby Power Supply Current (TTL Input Levels)	$\overline{CE}$ ≥ V_{IH}, V_{CC} = Max, f = Max, Outputs Open	—	35	—	20	mA
I_{SB1}	Standby Power Supply Current (CMOS Input Levels)	$\overline{CE}$ ≥ V_{HC}, V_{CC} = Max, f = 0, Outputs Open V_{IN} ≤ V_{LC} or V_{IN} ≥ V_{HC}	—	10	—	2	mA

N/A = Not applicable

POWER DISSIPATION CHARACTERISTICS VS. SPEED

Sym	Parameter	Temperature Range	-15	-20	-25	-35	Unit
I_{CC}	Dynamic Operating Current*	Commercial	80	75	75	75	mA
		Industrial	90	80	80	80	mA

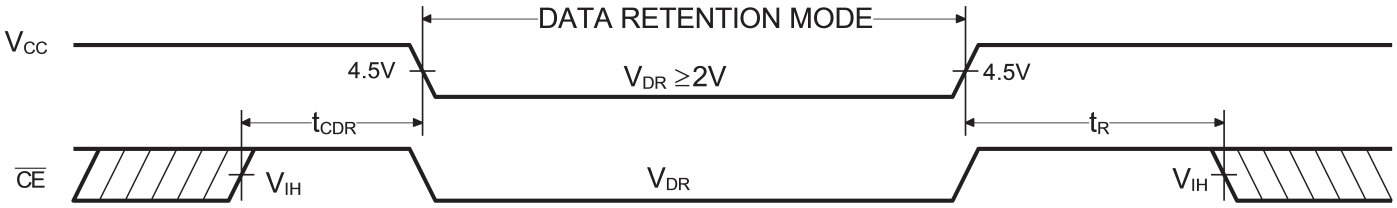
* V_{CC} = 5.5V. Tested with outputs open. f = Max. Switching inputs are 0V and 3V. $\overline{CE}$ = V_{IL}

DATA RETENTION CHARACTERISTICS (P4C1026L only)

Sym	Parameter	Test Conditions	Min	Typ* V_{cc}=		Max V_{cc}=		Unit
				2.0V	3.0V	2.0V	3.0V	
V_{DR}	V_{CC} for Data Retention		2.0					V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{CC}$ -0.2V, $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq 0.2V$		10	15	250	500	µA
t_{CDR}	Chip Deselect to Data Retention Time		0					ns
t_R†	Operation Recovery Time		t_{RC}§					ns

* T_A = +25°C
§ t_{RC} = Read Cycle Time
† This Parameter is guaranteed but not tested

DATA RETENTION WAVEFORM

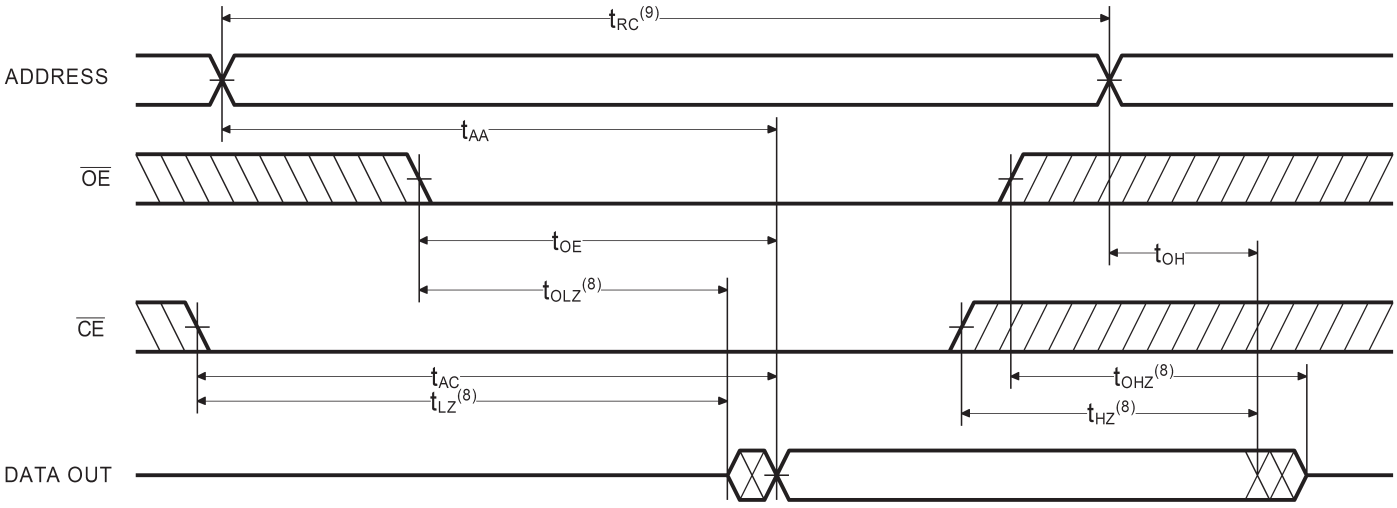


AC ELECTRICAL CHARACTERISTICS—READ CYCLE

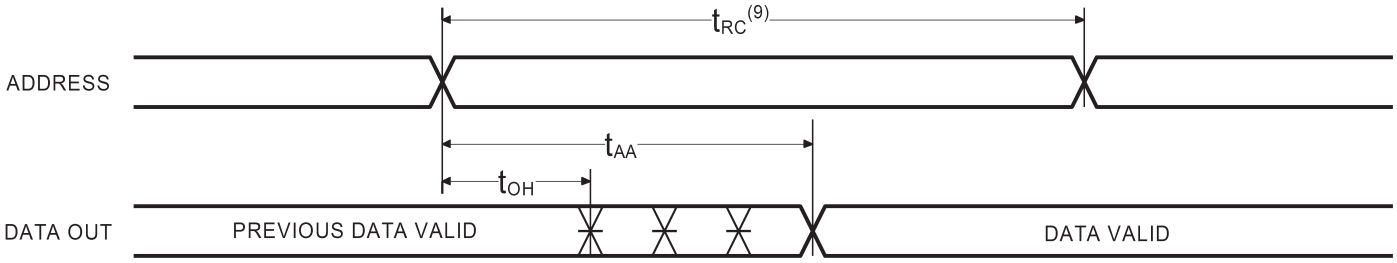
(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

Sym	Parameter	-15		-20		-25		-35		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	15		20		25		35		ns
t_{AA}	Address Access Time		15		20		25		35	ns
t_{AC}	Chip Enable Access Time		15		20		25		35	ns
t_{OH}	Output Hold from Address Change	2		2		2		2		ns
t_{LZ}	Chip Enable to Output in Low Z	2		3		3		3		ns
t_{HZ}	Chip Disable to Output in High Z		8		9		10		11	ns
t_{PU}	Chip Enable to Power Up Time	0		0		0		0		ns
t_{PD}	Chip Disable to Power Down		15		20		25		35	ns

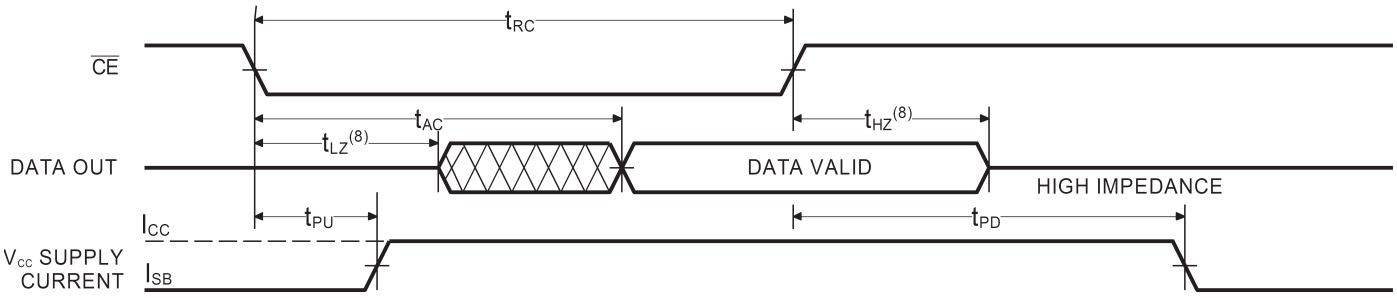
TIMING WAVEFORM OF READ CYCLE NO. 1 ($\overline{OE}$ CONTROLLED)[5]



TIMING WAVEFORM OF READ CYCLE NO. 2 (ADDRESS CONTROLLED)[5,6]



TIMING WAVEFORM OF READ CYCLE NO. 3 ($\overline{CE}$ CONTROLLED)[5,7]



Notes:

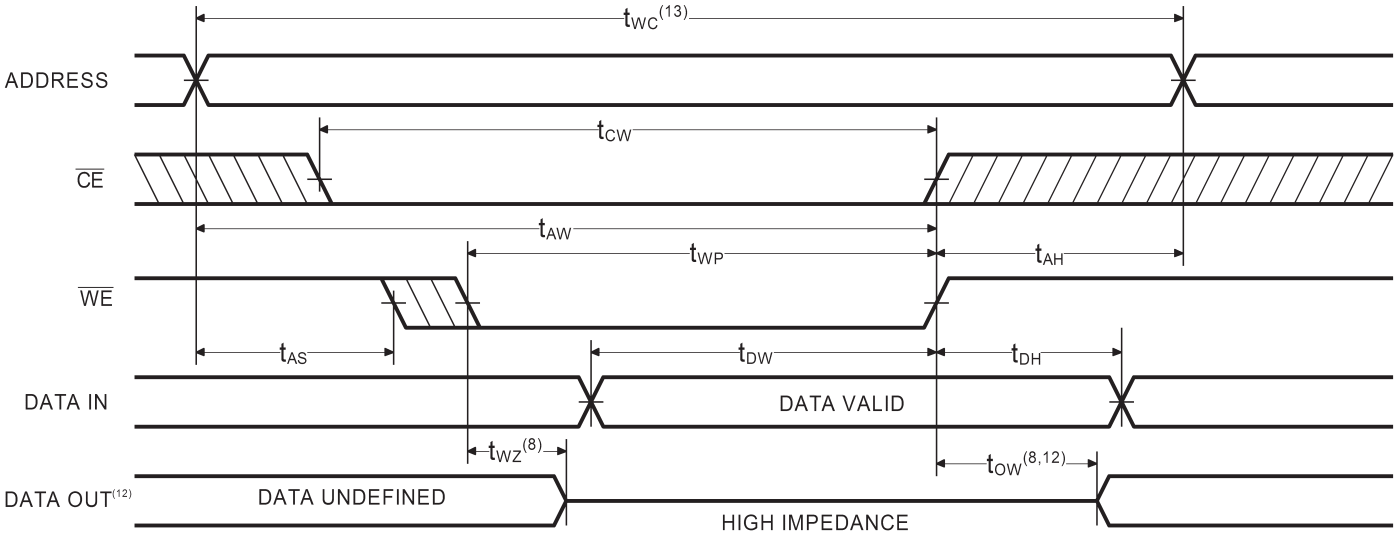
1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
2. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
3. Transient inputs with V_{IL} and I_{IL} not more negative than –3.0V and –100mA, respectively, are permissible for pulse widths up to 20 ns.
4. This parameter is sampled and not 100% tested.
5. $\overline{WE}$ is HIGH for READ cycle.
6. $\overline{CE}$ is LOW and $\overline{OE}$ is LOW for READ cycle.
7. ADDRESS must be valid prior to, or coincident with $\overline{CE}$ transition LOW.
8. Transition is measured ± 200 mV from steady state voltage prior to change, with loading as specified in Figure 1. This parameter is sampled and not 100% tested.
9. Read Cycle Time is measured from the last valid address to the first transitioning address.

AC CHARACTERISTICS—WRITE CYCLE

(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

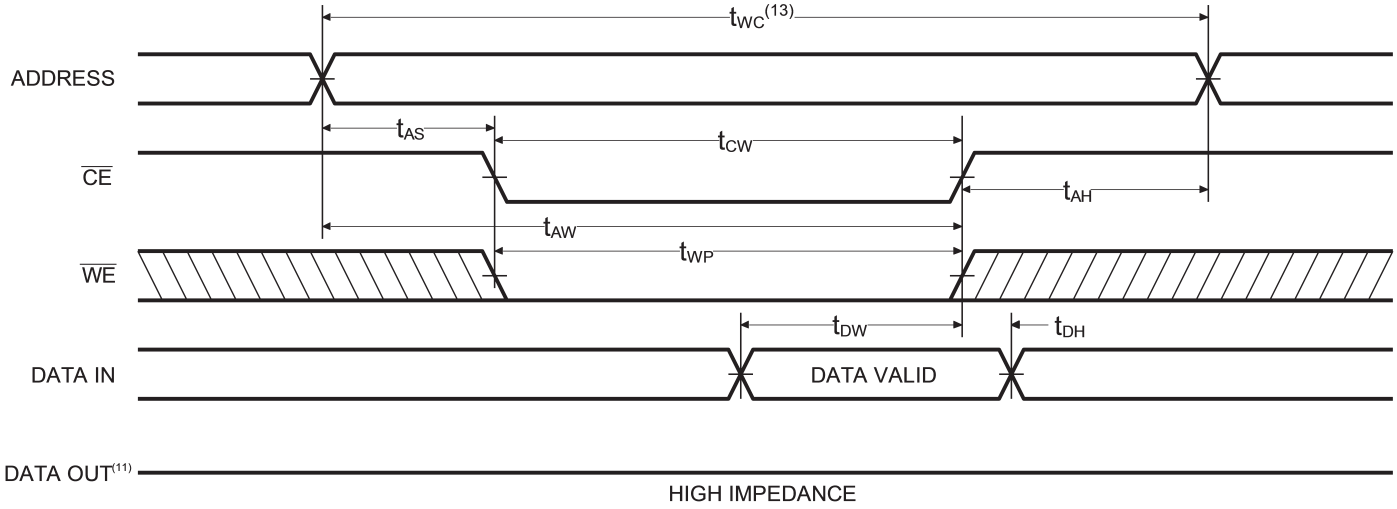
Sym	Parameter	-15		-20		-25		-35		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	13		20		25		35		ns
t_{CW}	Chip Enable Time to End of Write	12		15		18		25		ns
t_{AW}	Address Valid to End of Write	12		15		18		25		ns
t_{AS}	Address Setup Time	0		0		0		0		ns
t_{WP}	Write Pulse Width	12		15		18		25		ns
t_{AH}	Address Hold Time	0		0		0		0		ns
t_{DW}	Data Valid to End of Write	7		8		10		15		ns
t_{DH}	Data Hold Time	0		0		0		0		ns
t_{WZ}	Write Enable to Output in High Z		6		8		10		15	ns
t_{OW}	Output Active from End of Write	2		2		2		3		ns

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)[10,11]



Notes:
10. $\overline{CE}$ and $\overline{WE}$ must be LOW for WRITE cycle.
11. $\overline{OE}$ is LOW for this WRITE cycle to show t_{WZ} and t_{OW}.
12. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high impedance state
13. Write Cycle Time is measured from the last valid address to the first transitioning address.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CE}$ CONTROLLED)[10]



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Figures 1 and 2

TRUTH TABLE

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	Power
Standby	H	X	X	High Z	Standby
D_{OUT} Disabled	L	H	H	High Z	Active
Read	L	L	H	D_{OUT}	Active
Write	L	X	L	High Z	Active

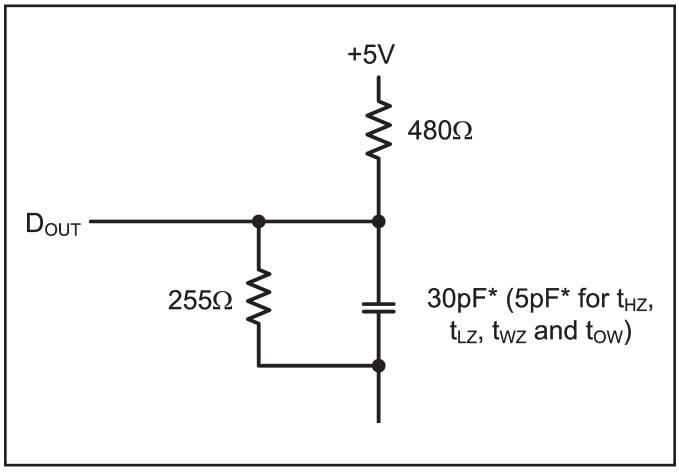


Figure 1. Output Load

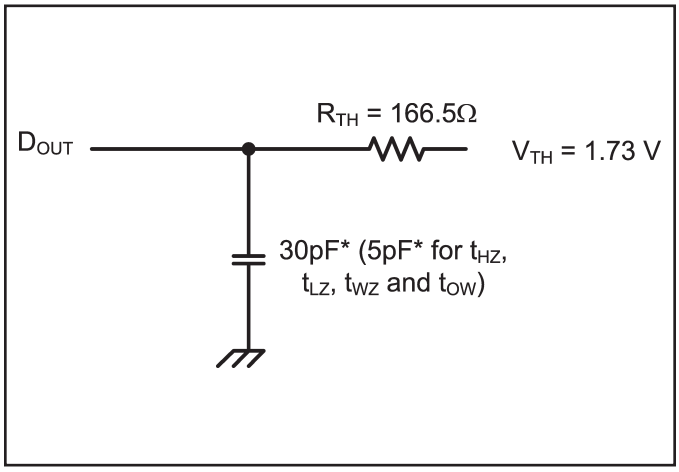
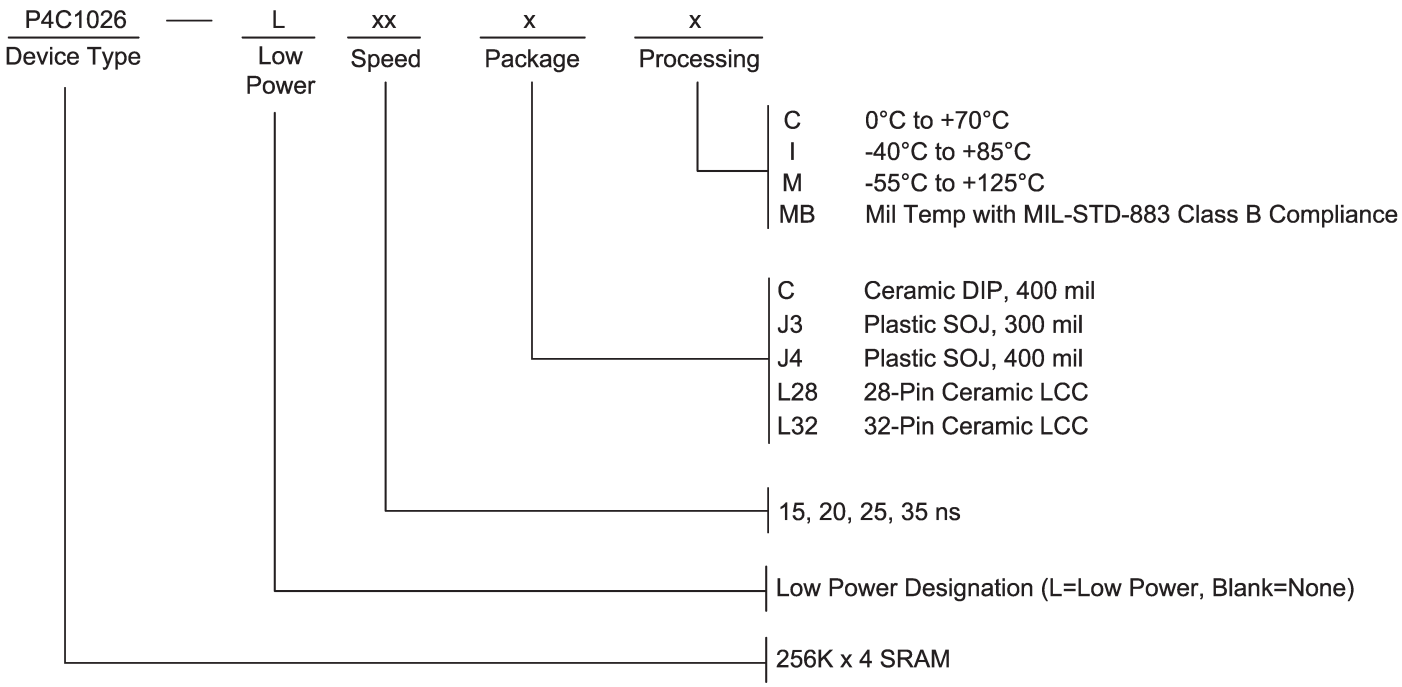


Figure 2. Thevenin Equivalent

* including scope and test fixture.

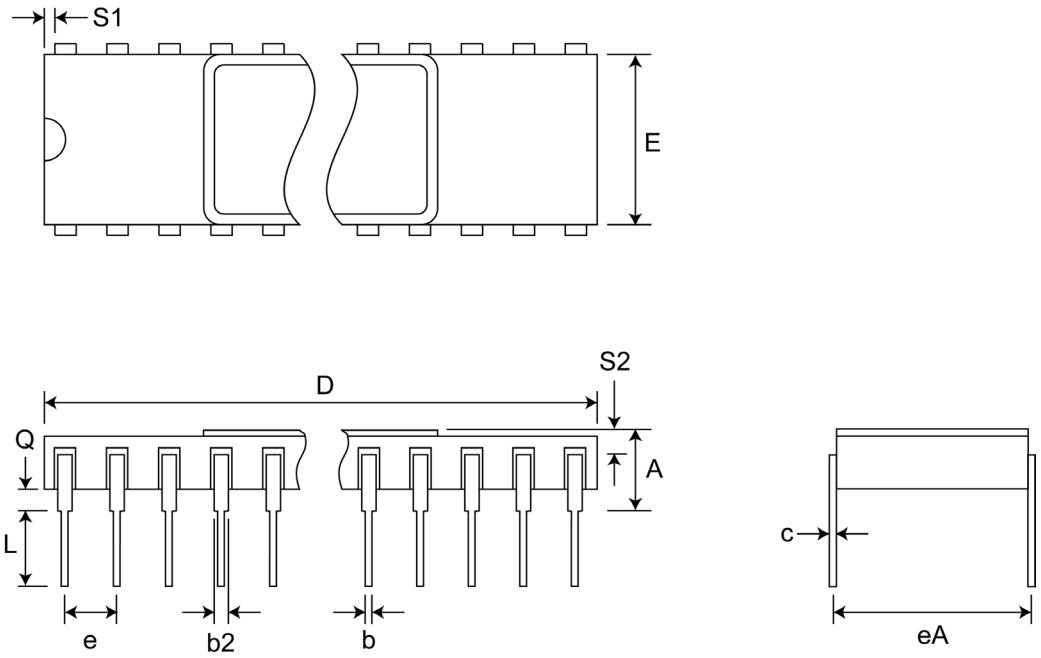
Note:
Because of the ultra-high speed of the P4C1026/L, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116Ω resistor must be used in series with D_{OUT} to match 166Ω (Thevenin Resistance).

ORDERING INFORMATION



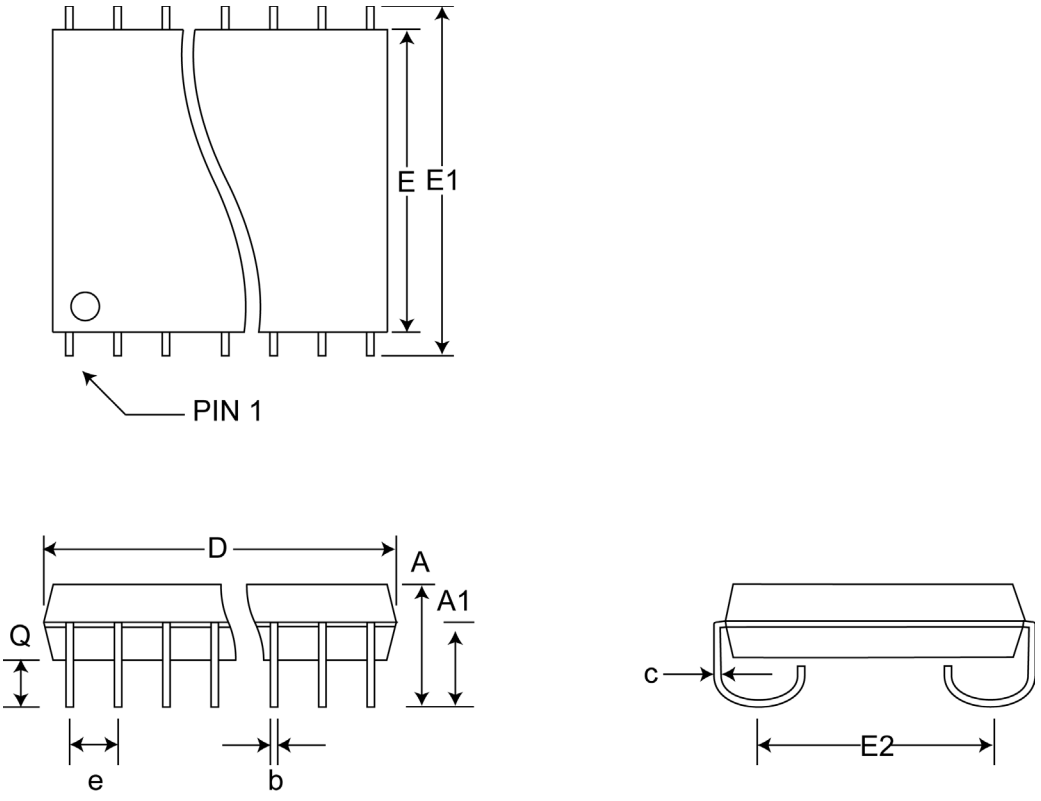
Pkg #	C7	
# Pins	28 (400 mil)	
Symbol	**Min**	**Max**
A	0.115	0.255
b	0.016	0.020
b2	0.045	0.065
C	0.008	0.018
D	1.384	1.416
e	0.100 BSC	
E	0.387	0.403
eA	0.400 BSC	
L	0.125	0.200
Q	0.015	0.070
S1	0.005	—
S2	0.005	—

SIDEBRAZED DUAL IN-LINE PACKAGE



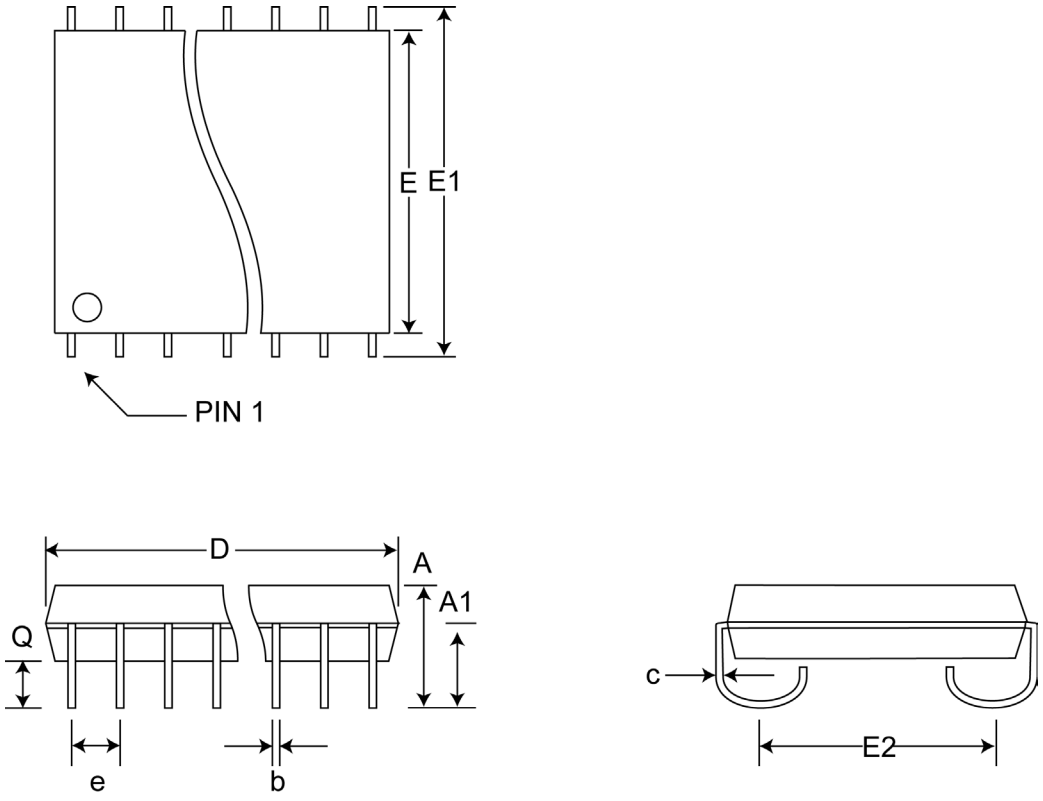
Pkg #	J5	
# Pins	28 (300 mil)	
Symbol	**Min**	**Max**
A	0.120	0.148
A1	0.078	-
b	0.014	0.020
C	0.007	0.011
D	0.700	0.730
e	0.050 BSC	
E	0.292	0.300
E1	0.335	0.347
E2	0.262	0.272
Q	0.025	-

SOJ SMALL OUTLINE IC PACKAGE



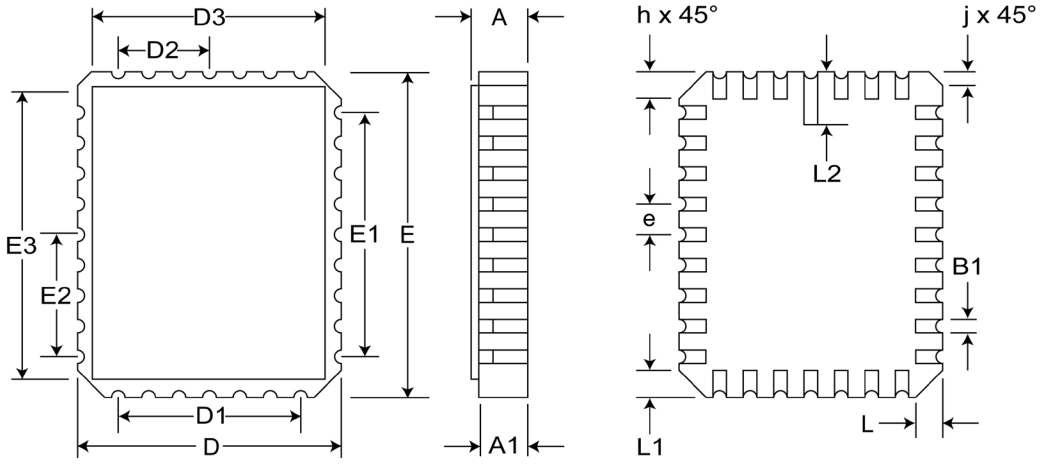
Pkg #	J7	
# Pins	28 (400 mil)	
Symbol	**Min**	**Max**
A	0.128	0.148
A1	0.082	-
b	0.013	0.019
C	0.007	0.013
D	0.720	0.730
e	0.050 BSC	
E	0.395	0.405
E1	0.435	0.445
E2	0.362	0.372
Q	0.025	-

SOJ SMALL OUTLINE IC PACKAGE



Pkg #	L13	
# Pins	32	
Symbol	**Min**	**Max**
A	0.070	0.093
A1	0.054	0.066
B1	0.025	0.031
D	0.442	0.458
D1	0.300 BSC	
D2	0.150 BSC	
D3	—	0.458
E	0.742	0.758
E1	0.400 BSC	
E2	0.200 BSC	
E3		0.558
e	0.050 TYP	
h		
j		
L	0.045	0.055
L1	0.045	0.055
L2	0.075	0.095
ND	7	
NE	9	

RECTANGULAR LEADLESS CHIP CARRIER



REVISIONS

DOCUMENT NUMBER	SRAM 127
DOCUMENT TITLE	P4C1026/P4C1026L ULTRA HIGH SPEED 256K x 4 STATIC CMOS RAMS

REV	ISSUE DATE	ORIGINATOR	DESCRIPTION OF CHANGE
OR	Oct-05	JDB	New Data Sheet
A	Aug-06	JDB	Updated SOJ package information
B	Oct-06	JDB	Added Ceramic DIP, LCC packages and military processing
C	Dec-06	JDB	Added L13 package, removed L12 package
D	Mar-07	JDB	Minor typographic corrections
E	Apr-07	JDB	Corrected LCC pin configuration
F	Jul-15	JDB	Added P4C1026L