WAFERSCALE INTEGRATION, INC.

WS27C010F

ADVANCE INFORMATION

T-46-13-29

1 Meg (128K x 8) CMOS EPROM

KEY FEATURES

- **High Performance**
  - 55 ns
- **Simplified Upgrade Path**
  - V_{PP} and PGM Are "Don't Care" During Normal Read Operation
  - Expandable to 8M Bits
- **Pin Compatible with WS27C010L**
- **EPI Processing**
  - Latch-Up Immunity to 200 mA
  - ESD Protection Exceeds 2000 Volts
- **JEDEC Standard Pin Configuration**
  - 32 Pin Dip Package

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GENERAL DESCRIPTION

The WS27C010F is a high performance, 1,048,576-bit Electrically Programmable UV Erasable Read Only Memory. It is organized as 128 K-words of 8 bits each. The 55 ns access time of the WS27C010F enables it to operate in high performance systems. The "Don't Care" feature during read operations enables memory expansions up to 8M bits with no printed circuit board changes.

High performance microprocessors such as the 80386 and 68020 require 55 ns memory access times to operate at or near full speed. The WS27C010F enables such systems to incorporate operating systems and/or applications software into EPROM. This enhances system utility by freeing up valuable RAM space for data or other program store and eliminating disk accesses for the EPROM resident routines.

The WS27C010F pin configuration was established to enable memory upgrades to 8M bits without hardware changes to the printed circuit board. Pins 1 and 31 are "don't care" during normal read operation. This enables higher order addresses to be connected to these pins (see DIP Pin Configurations). When higher density memories are required, the printed circuit board is ready to accept the higher density device with no hardware changes.

The WS27C010F is part of an eight product megabit EPROM family. Byte-wide family members (128K x 8) are the WS27C010L, WS27C010F (described herein) and WS57C010F as the high-speed version. Word-wide (64K x 16) family members are the WS27C210L, WS27C210F and the high-speed WS57C210F. The WS57C010M and WS57C210M are high speed, high bus drive EPROM modules.

The WS27C010F is manufactured using WSI's advanced CMOS technology.

PRODUCT SELECTION GUIDE

PARAMETER	WS27C010F-55	WS27C010F-70	WS27C010F-90	WS27C010F-10
Address Access Time (Max)	55 ns	70 ns	90 ns	100 ns
Chip Select Time (Max)	55 ns	70 ns	90 ns	100 ns
Output Enable Time (Max)	25 ns	25 ns	30 ns	30 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... −65°C to +125°C
Voltage on Any Pin with
Respect to Ground ..... −0.6V to +7V
V_{PP} with Respect to Ground ..... −0.6V to +14V
V_{CC} Supply Voltage with
Respect to Ground ..... −0.6V to +7V
ESD Protection ..... >2000V

***Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTICE: Specifications contained within the following tables are subject to change.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Comm'l	0° to +70°C	+5V ± 5%
Industrial	−40° to +85°C	+5V ± 10%
Military	−55° to +125°C	+5V ± 10%

READ OPERATION

DC CHARACTERISTICS $0°C \leq T_A \leq +70°C$; V_{CC} (Comm'l/Military) = +5V ± 10%.

SYMBOL	PARAMETER	CONDITIONS	LIMITS		
			MIN	MAX	UNITS
I_{LI}	Input Load Current	V_{IN} = 5.5V		10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V		10	µA
I_{PP}(1)	V_{PP} Load Current	$V_{PP} \leq V_{CC}$		10	µA
I_{SB} TTL	V_{CC} Current Standby	$\overline{CE}$ = V_{IH}		2	mA
I_{SB} CMOS	V_{CC} Current Standby	$\overline{CE}$ = V_{IH}		500	µA
I_{CC}(1)	V_{CC} Current Active	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		40(3)	mA
V_{IL}	Input Low Voltage		−0.1	+0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −400 µA	2.4		V
V_{PP}(1)	V_{PP} Read Voltage	V_{CC} = 5.0V ± 0.25	−0.1	V_{CC}+1	V

AC CHARACTERISTICS $0°C \leq T_A \leq +70°C$

SYMBOL	CHARACTERISTICS	TEST CONDITIONS	-55		-70		-90		-10		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		55		70		90		100	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		55		70		90		100	
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		25		25		30		30	
t_{DF}(2)	$\overline{OE}$ High to Output Float	$\overline{CE}$ = V_{IL}	0	25	0	25	0	30	0	30	
t_{OH}	Output Hold From Addresses $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0		0		0		0		

NOTES:
1. V_{PP} should be at a TTL level except during programming. The supply current would then be the sum of I_{CC} and I_{PP}. The maximum current value is with Outputs O_0 to O_7 unloaded.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
3. Add 2 mA/MHz for A.C. power component.

AC READ TIMING DIAGRAM

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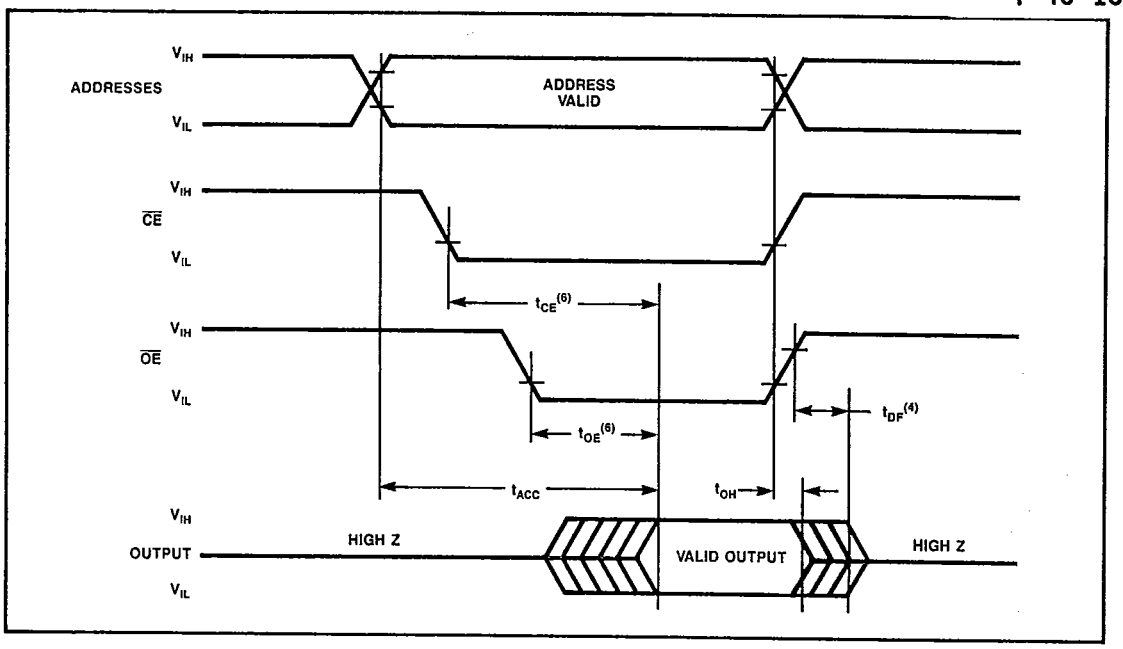

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CAPACITANCE[4] T_A = 25°C, f = 1 MHz

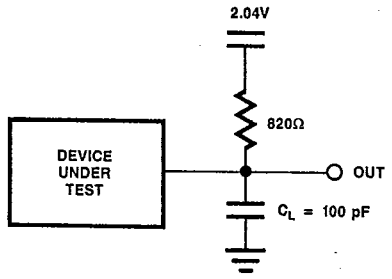
SYMBOL	PARAMETER	CONDITIONS	TYP[5]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES:
4. This parameter is only sampled and is not 100% tested.
5. Typical values are for T_A = 25°C and nominal supply voltages.
6. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.

A.C. TESTING INPUT/OUTPUT WAVEFORM

A.C. testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0." Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0."

A.C. TESTING LOAD CIRCUIT



C_L includes Jig Capacitance

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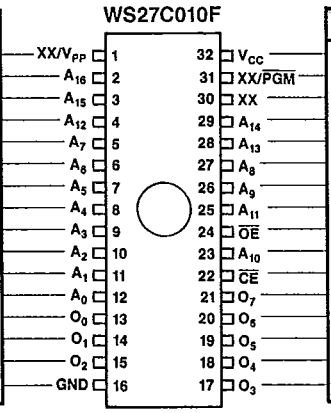
DIP PIN CONFIGURATIONS

8 Mbit	4 Mbit	2 Mbit	27512	27256
A_{19}	XX/V_{PP}	XX/V_{PP}		
A_{16}	A_{16}	A_{16}		
A_{15}	A_{15}	A_{15}	A_{15}	V_{PP}
A_{12}	A_{12}	A_{12}	A_{12}	A_{12}
A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND



27256	27512	2 Mbit	4 Mbit	8 Mbit
		V_{CC}	V_{CC}	V_{CC}
		XX/PGM	A_{18}	A_{18}
V_{CC}	V_{CC}	A_{17}	A_{17}	A_{17}
A_{14}	A_{14}	A_{14}	A_{14}	A_{14}
A_{13}	A_{13}	A_{13}	A_{13}	A_{13}
A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9
A_{11}	A_{11}	A_{11}	A_{11}	A_{11}
OE	OE/V_{PP}	OE	OE	OE/V_{PP}
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
CE	CE	CE	CE	CE
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

NOTE: Compatible EPROM pin configurations are shown in the blocks adjacent to the WS27C010F pins.

PIN NAMES

A_0–A_{16}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)