PRELIMINARY

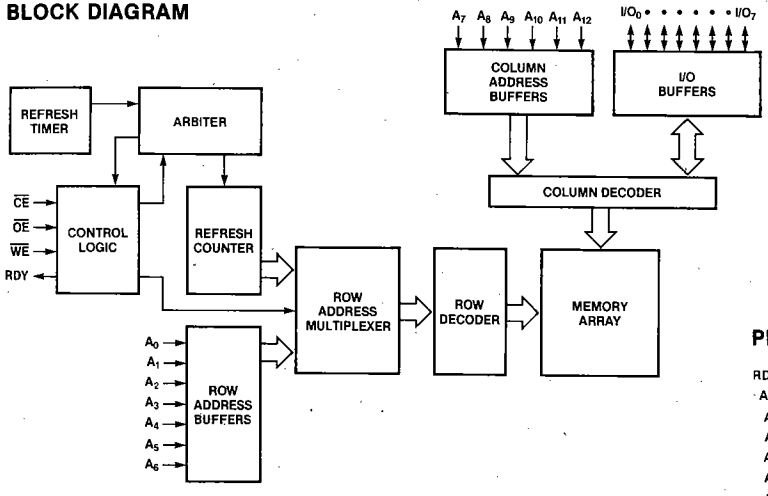
2186
8192 × 8 BIT INTEGRATED RAM

- **Low-cost, high-volume HMOS technology**
- **High density one transistor cell**
- **Single +5V ± 10% supply**
- **Proven HMOS reliability**
- **Low active current (70 mA)**
- **Simple asynchronous refresh operation/ static RAM compatible**
- **2764 EPROM compatible pin-out**
- **Two-line bus control**
- **JEDEC standard 28-pin site**
- **Low standby current (20 mA)**

The Intel 2186 is a 8192 word by 8-bit integrated random access memory (iRAM) fabricated on Intel's proven HMOS dynamic RAM technology. Integrated refresh control provides static RAM characteristics at a significantly lower cost. Packaged in the industry standard 28-pin DIP, the 2186 conforms to the industry standard JEDEC 28-pin site. Designs based on 2186 timings can be made fully compatible with EPROMs and static RAMs.

The 2186 is particularly suited for microprocessor applications and incorporates many requisite system features including low power dissipation, automatic initialization, extended cycle operation and two-line bus control to eliminate bus contention.

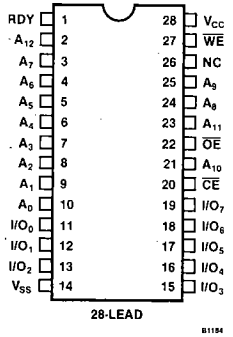
BLOCK DIAGRAM



PIN NAMES

A_0-A_{12}	ADDRESS INPUTS
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O_0-I/O_7	DATA INPUT/OUTPUT
RDY	READY
V_{CC}	+5V POWER
V_{SS}	GROUND

PIN CONFIGURATION



28-LEAD

B1184

September 1982
Order Number: 210460-001

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −10°C to +80°C
Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin with
Respect to Ground ..... −1.0 V to +7 V
D.C. Continuous Current per Output ..... 10 mA
D.C. Maximum Data Out Current ..... 50 mA
D.C. Power Dissipation ..... 1.0 W

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. AND OPERATING CHARACTERISTICS[1]

TA = 0°C to +70°C, VCC = +5V ± 10% unless otherwise noted.

Symbol	Parameter	Limits Min.	Limits Max.	Unit	Test Conditions	Notes
ILI	Input Load Current (All Input Pins)		10	μA	VIH = VSS to VCC	
|ILO|	Output Leakage Current		10	μA	$\overline{OE}$ = VIH	
ICC	Operating Current		70	mA	Minimum Cycle Time	2
ISB	Standby Current		20	mA	$\overline{CE}$ = VIH	
VIL	Input Low Voltage	−1.0	0.8	V		3
VIH	Input High Voltage	2.4	7.0	V		
VOL	Output Low Voltage		0.45	V	IOL = 2.1 mA	4
VOH	Output High Voltage	2.4		V	IOH = −1.0 mA	

NOTES:
1. Typical limits are VCC = +5V, TA = 25°C.
2. ICC is dependent on output loading when the device output is selected. Specified ICC max. is measured with the output open.
3. Specified VIL min. is for steady state operation. During transitions the inputs may overshoot to −2.0V for periods not to exceed 20 nsec.
4. IOL for RDY is 10 mA.

A.C. TEST CONDITIONS

Input Pulse and Timing
Reference Levels ..... 0.8V to 2.4V
Input Rise and Fall Times ..... 10 nsec
Output Timing Reference Levels .. 0.45V and 2.4V
Output Load ..... See Figure 1

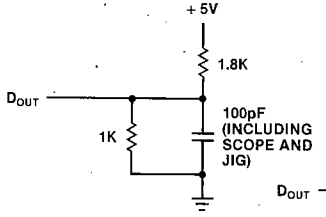


Figure 1.

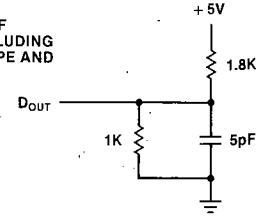


Figure 2.
(FOR HIGH IMPEDANCE MEASUREMENTS ONLY)

CAPACITANCE[5]

TA = 25°C, f = 1.0 MHz

Symbol	Parameter	Max.	Unit	Conditions
C_{ADD}	Address Capacitance	8	pF	V_{ADD} = 0V
$C_{I/O}$	I/O Capacitance	14	pF	$V_{I/O}$ = 0V
C_{IN}	Control Capacitance	14	pF	V_{IN} = 0V

NOTE: 5. This parameter is characterized and not 100% tested.

A.C. CHARACTERISTICS

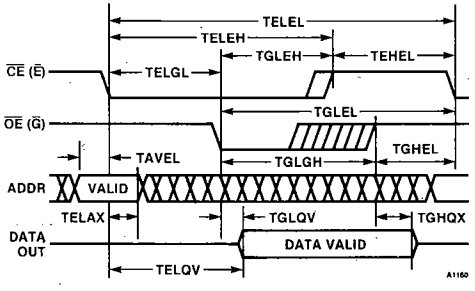
$T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 10\%$ unless otherwise noted.

READ CYCLE ($\overline{WE}$ = VIH)

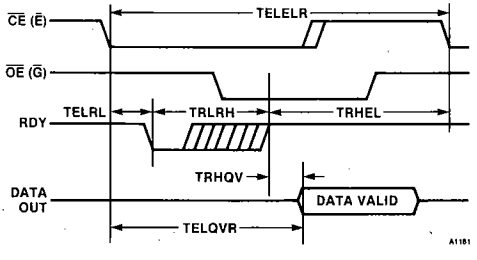
Symbol	Parameter	2186-25		2186-30		2186-35		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
TELEL	Cycle Time	425		500		600		ns	1
TELQV	Access Time from $\overline{CE}$		250		300		350	ns	1
TELELR	Cycle Time with Refresh	850		1000		1200		ns	2
TELQVR	Access Time from $\overline{CE}$ w/Refresh		675		800		950	ns	2
TGLQV	Access Time from $\overline{OE}$		65		70		75	ns	
TELEH	$\overline{CE}$ Pulse Width	40		40		40		ns	
TEHEL	$\overline{CE}$ High Time	40		40		40		ns	
TAVEL	Address Set-Up Time	0		0		0		ns	
TELAX	Address Hold Time	30		30		30		ns	
TGLEL	$\overline{OE}$ low to next $\overline{CE}$ low	250		275		300		ns	
TGLGH	$\overline{OE}$ Pulse Width	65		70		75		ns	
TGHEL	$\overline{OE}$ high to next $\overline{CE}$ low	40		40		40		ns	
TGHQX	$\overline{OE}$ high to Data Float	10	60	10	60	10	60	ns	3
TELGL	$\overline{CE}$ low to $\overline{OE}$ low — Pulse Mode	0	90	0	90	0	90	ns	4,5
TGLEH	$\overline{OE}$ low to $\overline{CE}$ high — Long Mode	40		40		40		ns	4
TELRL	$\overline{CE}$ low to RDY low		50		60		70	ns	6
TRLRH	RDY Pulse Width	100		100		100		ns	6
TRHQV	RDY high to Data Valid		60		70		95	ns	
TRHEL	RDY high to next $\overline{CE}$ low	250		275		350		ns	

WAVEFORMS

READ CYCLE



READ CYCLE WITH REFRESH



A.C. CHARACTERISTICS

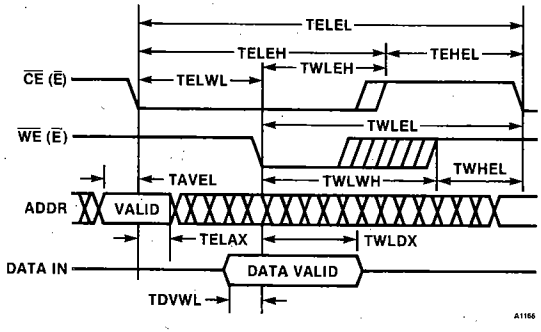
TA = 0°C to +70°C, VCC = +5V ± 10% unless otherwise noted.

WRITE CYCLE ($\overline{OE}$ = VIH)

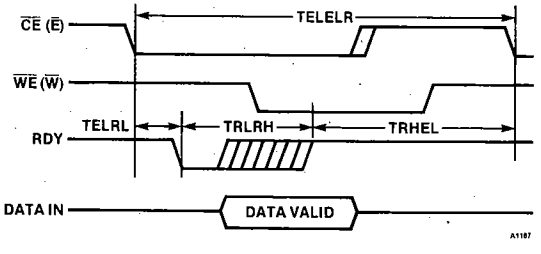
Symbol	Parameter	2186-25		2186-30		2186-35		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
TELEL	Cycle Time	425		500		600		ns	1
TELELR	Cycle Time with Refresh	850		1000		1200		ns	2
TELEH	$\overline{CE}$ Pulse Width	40		40		40		ns	
TEHEL	$\overline{CE}$ High Time	40		40		40		ns	
TAVEL	Address Set-Up Time	0		0		0		ns	
TELAX	Address Hold Time	30		30		30		ns	
TWLEL	$\overline{WE}$ low to next $\overline{CE}$ low	250		300		350		ns	
TWLWH	$\overline{WE}$ Pulse Width	40		40		40		ns	
TWHEL	$\overline{WE}$ high to next $\overline{CE}$ low	40		40		40		ns	
TDVWL	Data Set-Up to $\overline{WE}$ low	0		0		0		ns	
TWLDX	Data Hold from $\overline{WE}$ low	40		45		50		ns	
TELWL	$\overline{CE}$ low to $\overline{WE}$ low — Pulse Mode	0	90	0	90	0	90	ns	4,5
TWLEH	$\overline{WE}$ low to $\overline{CE}$ high — Long Mode	40		40		40		ns	4
TELRL	$\overline{CE}$ low to RDY low		50		60		70	ns	6
TRLRH	RDY Pulse Width	100		100		100		ns	6
TRHEL	RDY high to next $\overline{CE}$ low	250		275		350		ns	

WAVEFORMS

WRITE CYCLE



WRITE CYCLE WITH REFRESH



A.C. CHARACTERISTICS

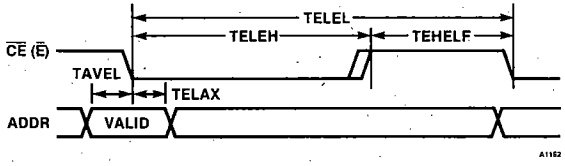
$T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 10\%$ unless otherwise noted.

FALSE MEMORY CYCLE ($\overline{OE}$ and $\overline{WE}$ = VIH)

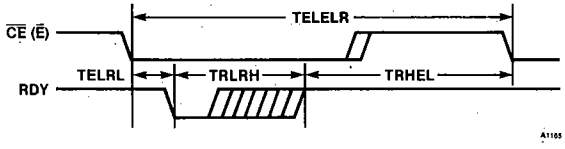
Symbol	Parameter	2186-25		2186-30		2186-35		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
TELEL	Cycle Time	425		500		600		ns	1
TELELR	Cycle Time with Refresh	850		1000		1200		ns	2
TELEH	$\overline{CE}$ Pulse Width	40	10000	40	10000	40	10000	ns	7
TEHELF	$\overline{CE}$ High Time for F.M.C.	200		250		275		ns	8
TAVEL	Address Set-Up Time	0		0		0		ns	
TELAX	Address Hold Time	30		30		30		ns	
TELRL	$\overline{CE}$ low to RDY low		50		60		70	ns	6
TRLRH	RDY Pulse Width	100		100		100		ns	6
TRHEL	RDY high to next $\overline{CE}$ low	250		275		350		ns	

WAVEFORMS

FALSE MEMORY CYCLE



FALSE MEMORY CYCLE WITH REFRESH



NOTES:

1. TELEL < TELELR and TELQV < TELQVR.
2. For reference only.
3. Transition is measured ±500 mV from steady state logic level with specified loading in Figure 2.
4. For Pulse Mode TELEH ≤ $TELGL_{max}$ + $TGLEH_{min}$ or TELEH ≤ $TELWL_{max}$ + $TWLEH_{min}$. For Long Mode TELEH > $TELGL_{max}$ + $TGLEH_{min}$ or TELEH > $TELWL_{max}$ + $TWLEH_{min}$.
5. For Long Mode $TELGL_{max}$ and $TELWL_{max}$ = 10 μsec.
6. C_{RDY} < 100 pF and R_{EXT} = 510Ω.
7. False Memory Cycles Only.
8. Note TEHELF > TEHEL.

FUNCTIONAL DESCRIPTION

The 2186 has three control pins: $\overline{CE}$ (Chip Enable), $\overline{OE}$ (Output Enable), and $\overline{WE}$ (Write Enable). An open-drain output pin called RDY indicates if refresh is occurring during an access request. *RDY will only respond when the 2186 has been selected by $\overline{CE}$ going active low during a refresh cycle.*

Cycles are initiated by latching addresses into the 2186 with the leading (falling) edge of $\overline{CE}$. When $\overline{CE}$ goes active during internal refresh, the RDY pin is pulled low signaling a delay. RDY remains low until shortly before both refresh and access (Read/Write) cycles are complete.

On-chip control circuitry tracks all operations for nearly transparent refresh. A high-speed on-chip arbitration circuit prevents conflicts from occurring between refresh and access cycles.

Access Cycles

READ CYCLE

A read cycle is initiated by $\overline{CE}$ and $\overline{OE}$ both going active low during the same cycle. $\overline{CE}$ may be either pulsed to initiate a cycle or held active low throughout the cycle. $\overline{OE}$ is a logic level; $\overline{OE}$ controls the 2186 data output bus. Access times are specified from both $\overline{OE}$ and $\overline{CE}$. Data remains on the data bus until $\overline{OE}$ returns inactive (high) *independent of $\overline{CE}$*. $\overline{WE}$ may not go active during a Read cycle.

WRITE CYCLE

A Write cycle is initiated by $\overline{CE}$ and $\overline{WE}$ going active low during the same cycle. $\overline{CE}$ may be a pulse or a logic level. *$\overline{WE}$ leading edge* latches data from the data bus into the 2186. $\overline{OE}$ may not go active during a Write cycle.

FALSE MEMORY CYCLE (FMC)

A False Memory cycle is initiated by $\overline{CE}$ going active *without* either $\overline{OE}$ or $\overline{WE}$ going active. No memory cycle will be performed. Note that address set-up and hold times must be observed for False Memory cycle operation.

Operating Modes

REFRESH OPERATION

Refresh is totally automatic and requires no external stimulas. All refresh functions are controlled internally.

A high-speed arbitration circuit will resolve any potential conflict arising between simultaneous external access and internal refresh cycle requests. The internal timer period is specified as 24 μsec. ± 50%.

The 2186 may also be refreshed by performing Read, Write, or False Memory cycles on all 128 rows (A0 through A6) within a two millisecond period.

EXTENDED CYCLE OPERATION

Extended cycle operation is defined as holding $\overline{OE}$ or $\overline{WE}$ valid (low) for indefinite periods. ($\overline{CE}$ is allowed to return high.) Data will remain valid on the bus as long as $\overline{OE}$ is valid. $\overline{WE}$ latches data on the leading (falling) edge. Automatic refreshes will continue to be performed as needed, even while $\overline{OE}$ or $\overline{WE}$ is held low; RDY will *not* respond during these extended cycle refreshes.

INITIALIZATION

To guarantee initialization, all control inputs must be inactive (high) for a 100 microsecond period after V_{CC} is within specification. No extra cycles are required before normal operation may begin.

Interfacing Considerations

The 2186 is an edge enabled RAM. Below is an illustration of a simple interface for connecting microprocessors with edge enable memories. *A stable $\overline{CE}$ clock is necessary to avoid accidentally selecting the RAM.* Generally, stable select signals are desirable in all types of microsystem applications. Most common decoding circuits allow addresses to flow directly through the decoder (i.e. decoder permanently "enabled"). This technique may allow false decoder outputs to occur when addresses are in transition. This may result in false $\overline{CE}$ signals and potentially, invalid memory requests. A simple gating circuit will inhibit enabling the decoder until addresses are valid at the decoder inputs.

Another interfacing consideration is the relationship between $\overline{WE}$ and valid data. The 2186 performs a write operation on the leading edge of $\overline{WE}$. In a minimum mode 8088 or 8086 system, $\overline{WE}$ occurs before data is valid. The cross-coupled NAND gate configuration shown below on the $\overline{WR}$ signal will prevent this from occurring. This implementation also guarantees valid data on the rising (trailing) edge of $\overline{WE}$ to maintain compatibility with fully static RAMs. (For maximum mode 8088 or 8086 operation, the control signal $\overline{MWTC}$ directly from the 8288 bus controller serves the same function.) For a more detailed description of designing iRAM

systems, refer to Intel App. Note #132 on *"Designing Memory Systems with the 8K × 8 iRAM"*

Layout Considerations

To ensure compatibility with other 28-pin memory devices such as EPROMs, several pins require close examination; specifically, pins number 1, 26 and 27. Following is a discussion of the system level operation and the design considerations for these pins.

PIN #1

Pin 1 on all EPROMs is reserved for the high voltage programming bias, V_{PP}. EPROMs are usually programmed external to the system. Therefore, in normal system operation, pin 1 is connected to V_{CC}.

Pin 1 on the 2186 is the microprocessor handshake signal, RDY. The RDY signal may be bussed to the RDY input of either the microprocessor or clock generator. Because RDY is an open drain output, all 2186 RDY signals may be "wire OR'd" with any other RDY signals in the system. A 510 ohm pull-up resistor is required between RDY and V_{CC}. For the 2186 application, a trace should be run from pin 1 of each socket location to the RDY input of either the microprocessor or clock generator. Also, a provision for a pull-up resistor to V_{CC} is needed.

PIN #26

While pin 26 is a No Connect for both the 2186 or the 2764 EPROM, a trace to pin 26 from V_{CC} will guarantee compatibility between 24 pin and 28 pin EPROMs. Pin 26 will carry the additional address bit required to future higher density memories. For flexibility, provide a jumper for an address bit and/or V_{CC} on pin 26.

PIN #27

Pin 27 is labelled $\overline{WE}$ on the RAM and $\overline{PGM}$ on the EPROM. While $\overline{WE}$ is a system level control signal, $\overline{PGM}$ is only used when programming the EPROM (V_{PP} at +21V). $\overline{PGM}$ may be allowed to toggle during normal EPROM operation (V_{PP} at +5V). Therefore, $\overline{WE}$ may be bussed to every socket location with no jeopardy of illegal operation.