



Silicon Gate MOS 2708/2704

8192/4096 BIT ERASABLE AND ELECTRICALLY REPROGRAMMABLE READ ONLY MEMORY

- 2708 1024x8 Organization
- 2704 512x8 Organization

- Fast Programming — Typ. 100 sec. For All 8K Bits
- Low Power During Programming
- Access Time — 450 ns
- Standard Power Supplies — +12V, ±5V
- Static — No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Three-State Output — OR-Tie Capability

The Intel 2708/2704 are high speed 8192/4096 bit erasable and electrically reprogrammable ROM's (EPROM) ideally suited where fast turn around and pattern experimentation are important requirements.

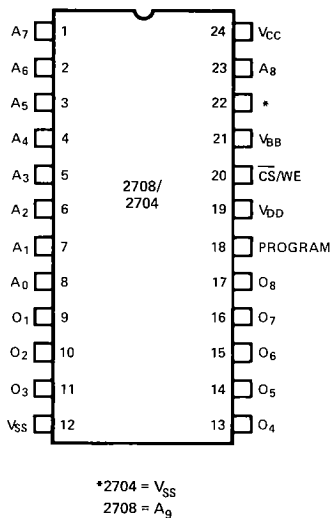
The 2708/2704 are packaged in a 24 pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the devices.

A pin for pin mask programmed ROM, the Intel 2308, is available for large volume production runs of systems initially using the 2708.

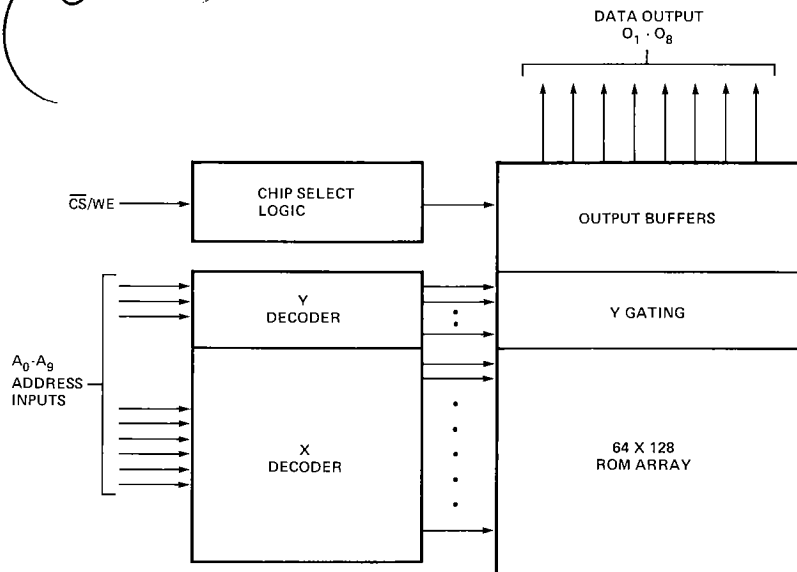
The 2708/2704 is fabricated with the time proven 1.5 micron silicon gate technology.

OFFICE COPY
(OLD)

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN NAMES

A ₀ -A ₉	ADDRESS INPUTS
O ₁ -O ₈	DATA OUTPUTS
CS/WE	CHIP SELECT/WRITE ENABLE INPUT

Absolute Maximum Ratings*

Temperature Under Bias	-25°C to +85°C
Storage Temperature	-65°C to +125°C
All Input or Output Voltages with Respect to V_{BB} (except Program)	+15V to -0.3V
Program Input to V_{BB}	+35V to -0.3V
Supply Voltages V_{CC} and V_{SS} with Respect to V_{BB}	+15V to -0.3V
V_{DD} with Respect to V_{BB}	+20V to -0.3V
Power Dissipation	1.5W

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION

D.C. and Operating Characteristics

$T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = +5V \pm 5\%$, $V_{DD} = +12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{SS} = 0V$, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Conditions
I_{LI}	Address and Chip Select Input Load Current			10	μA	$V_{IN} = 5.25V$
I_{LO}	Output Leakage Current			10	μA	$V_{OUT} = 5.25V$, $\overline{CS}/WE = 5V$
I_{DD}	V_{DD} Supply Current		50	65	mA	Worst Case Supply Currents: All Inputs High $\overline{CS}/WE = 5V$; $T_A = 0^\circ\text{C}$
I_{CC}	V_{CC} Supply Current		6	10	mA	
I_{BB}	V_{BB} Supply Current		30	45	mA	
V_{IL}	Input Low Voltage	V_{SS}		0.65	V	
V_{IH}	Input High Voltage	3.0		$V_{CC}+1$	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 1.6\text{mA}$
V_{OH1}	Output High Voltage	3.7			V	$I_{OH} = -100\mu\text{A}$
V_{OH2}	Output High Voltage	2.4			V	$I_{OH} = -1\text{mA}$
P_D	Power Dissipation			800	mW	$T_A = 70^\circ\text{C}$

- NOTES: 1. Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltages.
2. The program input (Pin 18) may be tied to V_{SS} or V_{CC} during the read mode.

SILICON GATE MOS 2708/2704

A.C. Characteristics

$T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = +5\text{V} \pm 5\%$, $V_{DD} = +12\text{V} \pm 5\%$, $V_{BB} = -5\text{V} \pm 5\%$, $V_{SS} = 0\text{V}$, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{ACC}	Address to Output Delay		280	450	ns
t_{CO}	Chip Select to Output Delay			120	ns
t_{DF}	Chip De-Select to Output Float	0		120	ns
t_{OH}	Address to Output Hold	0			ns

Capacitance^[1]: $T_A = 25^\circ\text{C}$, $f = 1\text{MHz}$

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN}=0\text{V}$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT}=0\text{V}$

Note 1. This parameter is periodically sampled and not 100% tested.

A.C. Test Conditions:

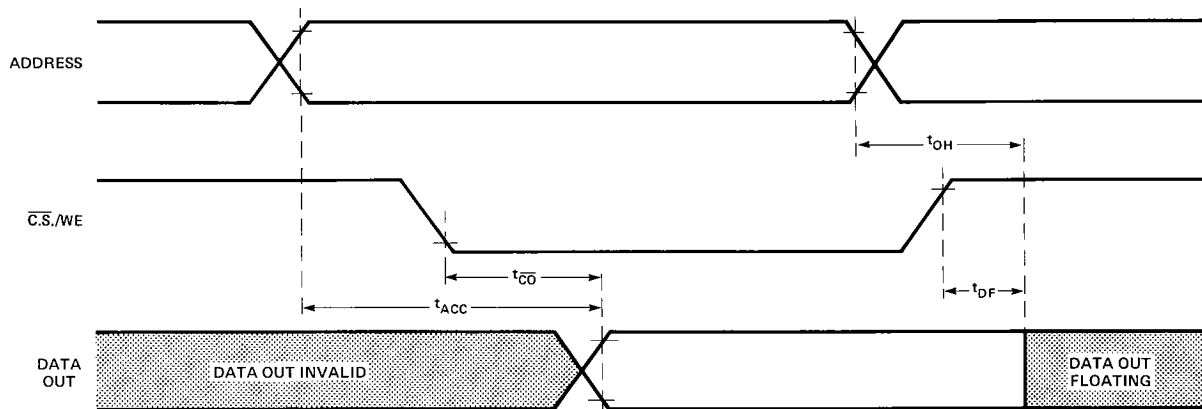
Output Load: 1 TTL gate and $C_L = 100\text{pF}$

Input Rise and Fall Times: $\leq 20\text{ns}$

Timing Measurement Reference Levels: 0.8V and 2.8V for inputs; 0.8V and 2.4V for outputs

Input Pulse Levels: 0.65V to 3.0V

Waveforms



PROGRAMMING OPERATION

Description

Initially, and after each erasure, all bits of the 2708/2704 are in the "1" state (Output High). Information is introduced by selectively programming "0" into the desired bit locations.

The circuit is set up for programming operation by raising the \overline{CS}/WE input (Pin 20) to +12V. The word address is selected in the same manner as in the read mode. Data to be programmed are presented, 8-bits in parallel, to the data output lines (O_1-O_8). Logic levels for address and data lines and the supply voltages are the same as for the read mode. After address and data set up one program pulse (V_P) per address is applied to the program input (Pin 18). One pass through all addresses to be programmed is defined as a program loop. The number of loops (N) required is a function of the program pulse width (t_{PW}) according to $N \times t_{PW} \geq 100$ ms.

For program verification, program loops and read loops may be alternated as shown in waveform B.

Program Characteristics

$T_A = 25^\circ C$, $V_{CC} = +5V \pm 5\%$, $V_{DD} = +12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{SS} = 0V$, $\overline{CS}/WE = +12V$, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{AS}	Address Setup Time	10			μs
t_{CSS}	\overline{CS}/WE Setup Time	10			μs
t_{DS}	Data Setup Time	10			μs
t_{AH}	Address Hold Time	1			μs
t_{CH}	\overline{CS}/WE Hold Time	.5			μs
t_{DH}	Data Hold Time	1			μs
t_{DF}	Chip Deselect to Output Float Delay	0		120	ns
t_{DPR}	Program To Read Delay			10	μs
t_{PW}	Program Pulse Width	.1		1.0	ms
t_{PR}	Program Pulse Rise Time	.5		2.0	μs
t_{PF}	Program Pulse Fall Time	.5		2.0	μs
I_P	Programming Current		10	20	mA
V_P	Program Pulse Amplitude	25		27	V

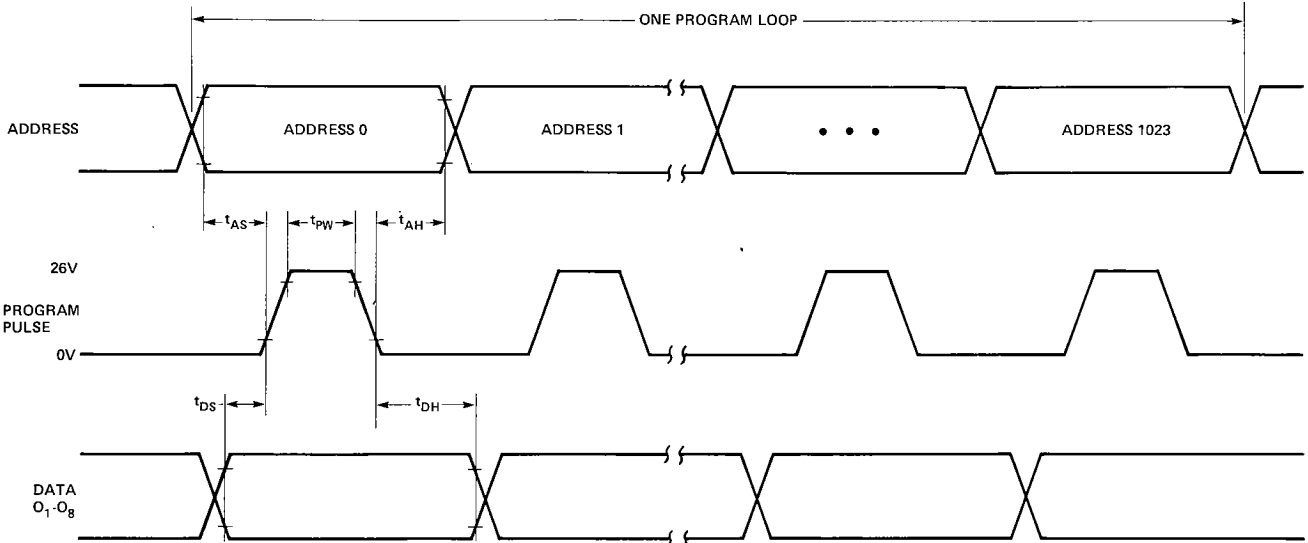
NOTE: Intel's standard product warranty applies only to devices programmed to specifications described herein.

Waveforms

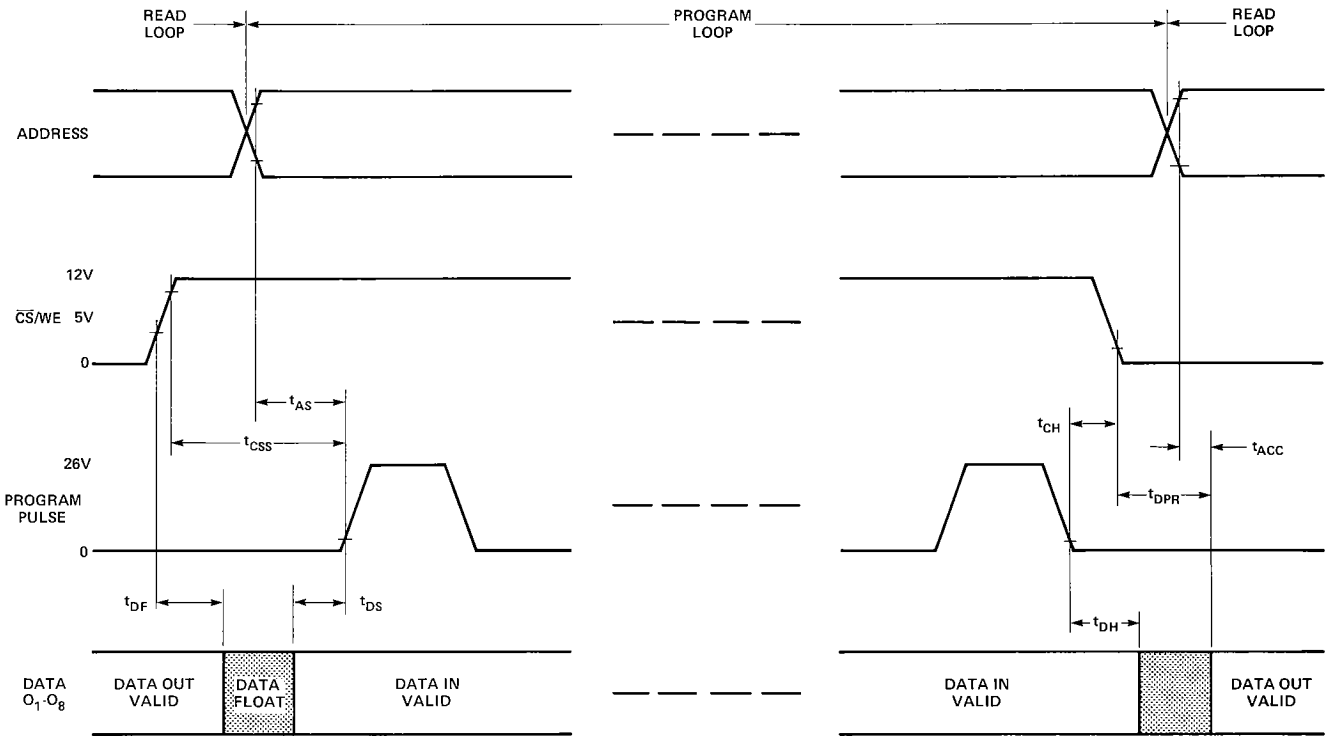
(Logic levels and timing reference levels same as in the Read Mode unless noted otherwise.)

A) Program Mode

$\overline{CS}/WE = +12V$

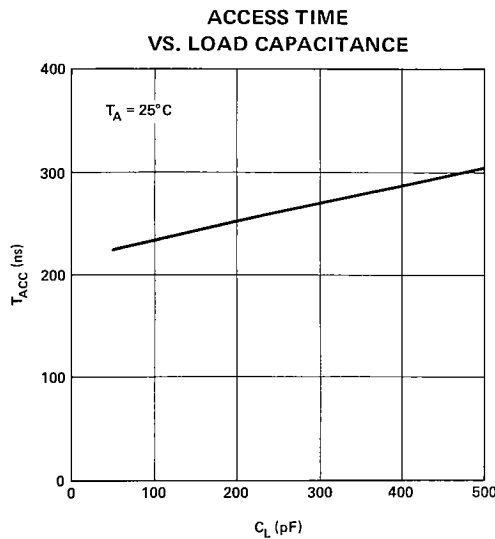
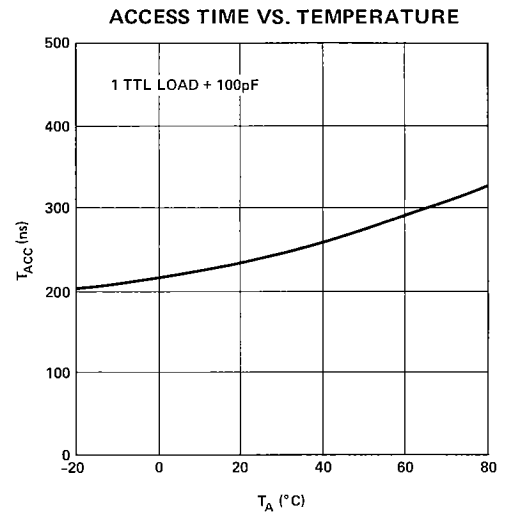
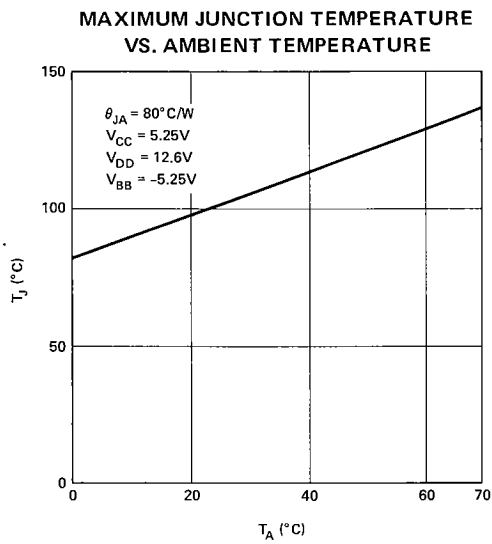
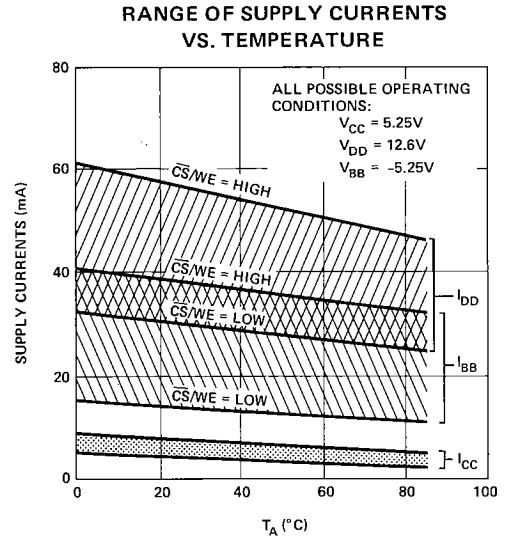
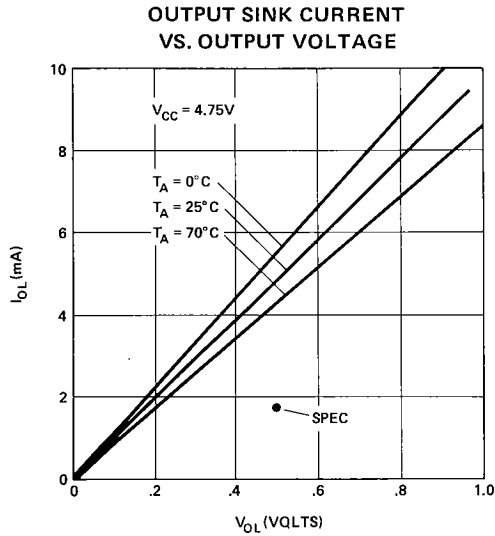


B) Read/Program/Read Transitions



SILICON GATE MOS 2708/2704

Typical Characteristics (Nominal supply voltages unless otherwise noted):





U.S. MARKETING HEADQUARTERS

Intel Corporation
3065 Bowers Avenue
Santa Clara, California 95051
Tel: (408) 246-7501
TWX: 910-338-0026
TELEX: 34-6372

WESTERN

1651 East 4th Street
Suite 228
Santa Ana, California 92701
Tel: (714) 835-9642
TWX: 910-595-1114

MID-AMERICA

6350 L.B.J. Freeway
Suite 178
Dallas, Texas 75240
Tel: (214) 661-8829
TWX: 910-860-5487

GREAT LAKES REGION

8312 North Main Street
Dayton, Ohio 45415
Tel: (513) 890-5350
TELEX: 288-004

EASTERN

2 Militia Drive
Suite 4
Lexington, Massachusetts 02173
Tel: (617) 861-1136
TWX: 710-321-0187

MID-ATLANTIC

520 Pennsylvania Ave., Suite 102
Fort Washington, Pennsylvania 19034
Tel: (215) 542-9444
TWX: 510-661-3055

57 W. Timonium Rd., Suite 307
Timonium, Maryland 21093
Tel: (301) 252-7742

EUROPE

Belgium
Intel Office
216 Avenue Louise
B-1050 Brussels
Tel: (02) 649-2003
TELEX: 24814

ORIENT

Japan
Intel Japan Corporation
Kasahara Bldg.
1-6-10, Uchikanda
Chiyoda-ku
Tokyo 101
Tel: (03) 295-5441
TELEX: 781-28426