SRAM

4K x 4 SRAM

WITH SEPARATE INPUTS AND OUTPUTS

FEATURES

- High speed: 12, 15, 20, 25, 30 and 35ns
- High-performance, low-power, CMOS double metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL compatible
- MT5C1606 – output tracks input during WRITE
- MT5C1607 – output high impedance during WRITE

OPTIONS — MARKING

- Timing

12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
30ns access	-30
35ns access	-35

- Packages

Plastic DIP (300 mil)	None
Ceramic DIP (300 mil)	C
Plastic SOJ (300 mil)	DJ
Ceramic LCC	EC

- Two Volt Data Retention — L

GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

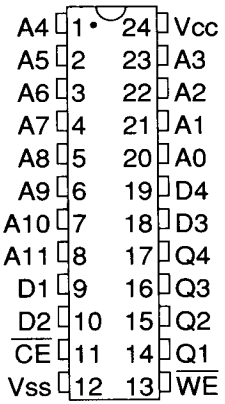
For flexibility in high speed memory applications, Micron offers chip enable ($\overline{CE}$) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design. The x4 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

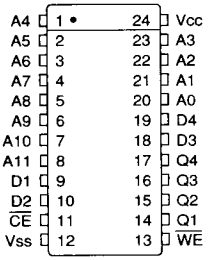
All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

PIN ASSIGNMENT (Top View)

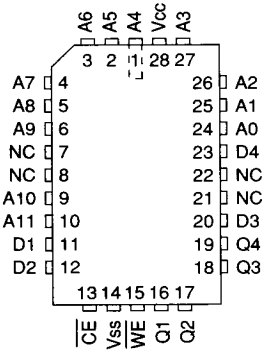
24L/300DIP
(A-7, B-7)



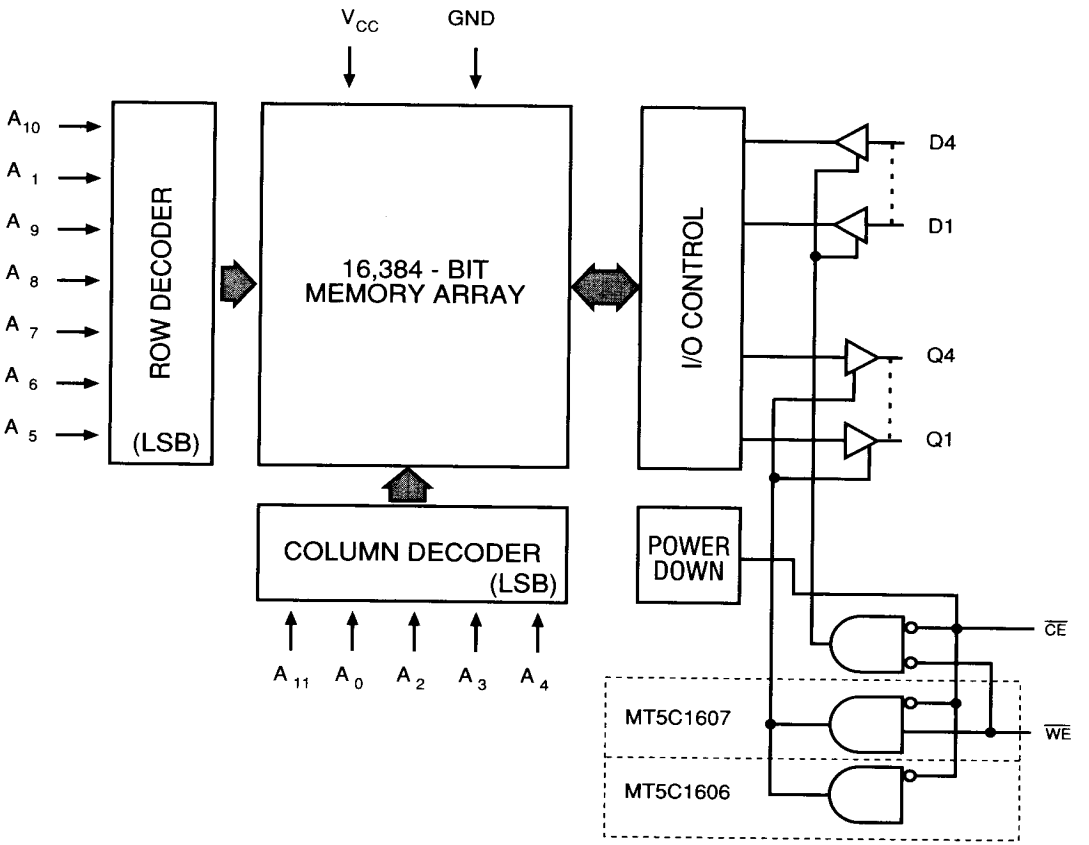
24L/300 SOJ
(E-4)



28L/LCC
(F-4)



FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	H	X	HIGH-Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE (1)	L	L	HIGH-Z	ACTIVE
WRITE (2)	L	L	D	ACTIVE

NOTE: 1. MT5C1607 ONLY
2. MT5C1606 ONLY

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} .....-1.0V to +7.0V
Storage Temperature (Ceramic) .....-65°C to +150°C
Storage Temperature (Plastic) .....-55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

			MAX							
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-30	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{CC}	140	125	110	100	100	100	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC, Outputs Open	I_{SB1}	50	45	40	30	30	30	mA	
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2V; $V_{IH} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	3	3	3	3	3	3	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1MHz	C_I		7	pF	4
Output Capacitance	V_{CC} = 5V	C_O		7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ± 10%)

DESCRIPTION		-12		-15		-20		-25		-30		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle															
READ cycle time	t_{RC}	12		15		20		25		30		35		ns	
Address access time	t_{AA}		12		15		20		25		30		35	ns	
Chip Enable access time	t_{ACE}		11		12		15		20		25		30	ns	
Output hold from address change	t_{OH}	3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	t_{LZCE}	3		3		5		5		5		5		ns	
Chip Disable to output in High-Z	t_{HZCE}		7		7		10		10		15		20	ns	6, 7
Chip Enable to power-up time	t_{PU}	0		0		0		0		0		0		ns	
Chip Disable to power-down time	t_{PD}		12		15		20		25		30		35	ns	
WRITE Cycle															
WRITE cycle time	t_{WC}	12		15		20		25		30		35		ns	
Chip Enable to end of write	t_{CW}	10		12		15		20		25		25		ns	
Address valid to end of write	t_{AW}	12		12		15		20		25		25		ns	
Address setup time	t_{AS}	0		0		0		0		0		0		ns	
Address hold from end of write	t_{AH}	0		0		0		0		0		0		ns	
Write pulse width	t_{WP}	10		12		15		20		25		25		ns	
Data setup time	t_{DS}	7		8		10		10		15		15		ns	
Data hold time	t_{DH}	0		0		0		0		0		0		ns	
Write Disable to output in Low-Z	t_{LZWE}	2		2		2		2		2		2		ns	
Write Enable to output in High-Z	t_{HZWE}		6		6		8		10		12		15	ns	
Write Enable to output valid	t_{AWE}		12		15		20		25		30		35	ns	
Data valid to output valid	t_{ADV}		12		15		20		25		30		35	ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

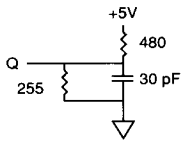


Fig. 1 OUTPUT LOAD EQUIVALENT

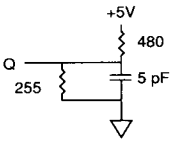


Fig. 2 OUTPUT LOAD EQUIVALENT

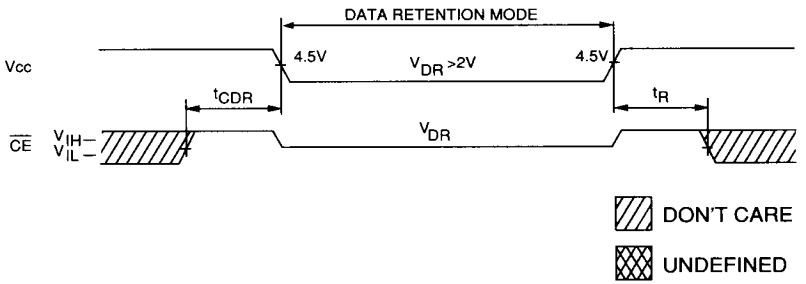
NOTES

1. All voltages referenced to Vss (GND).
2. -3.0V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) can initiate and terminate a WRITE cycle.
13. For automotive, industrial and extended temperature specifications refer to page 4-165.

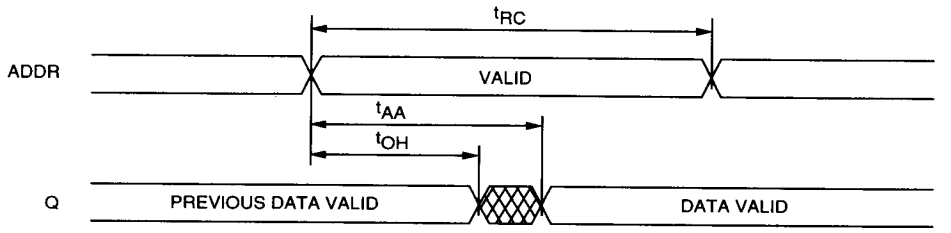
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2v	ICCDR		95	250	µA	
		Vcc = 3v			300	400	µA	
Chip Deselect to Data Retention Time			^{t}CDR	0		—	ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

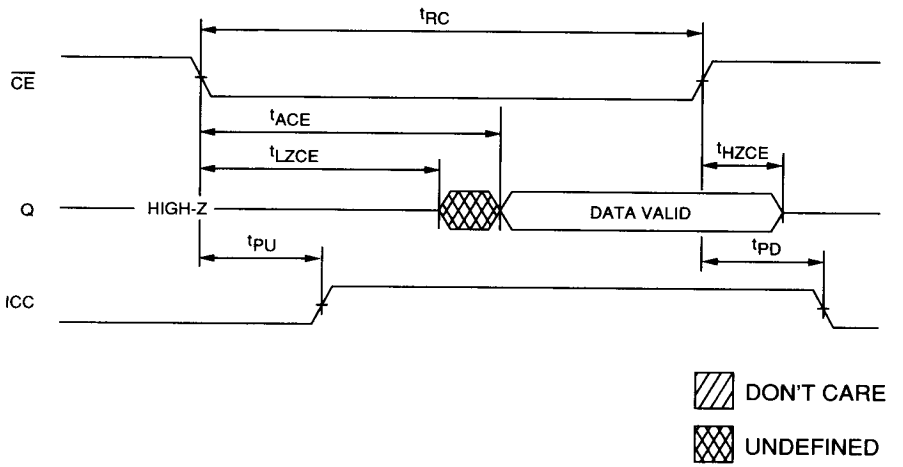
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1 [8, 9]

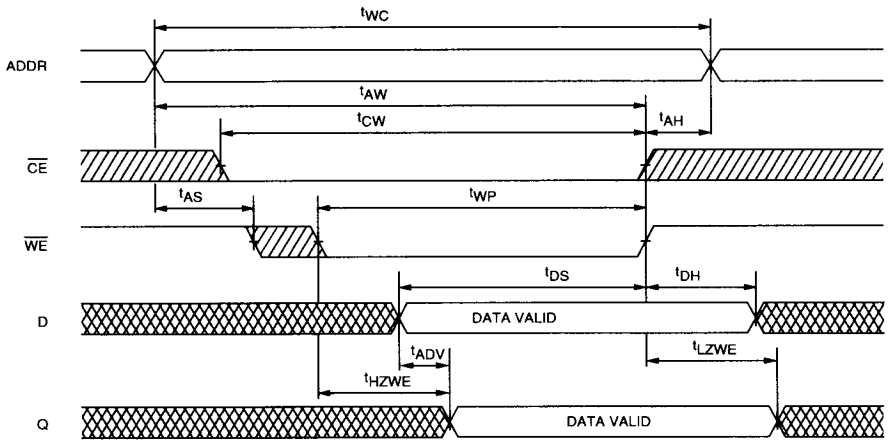


READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1

(Write Enable Controlled) [7, 12]



WRITE CYCLE NO. 2

(Chip Enable Controlled) [12]