MOS RAMs

MM4262/MM5262 2048-bit fully decoded dynamic random access read/write memory

general description

The MM4262/MM5262 is a fully decoded 2048 word by 1 bit dynamic read/write random access memory fabricated using National Semiconductor's proprietary silicon gate low threshold technology. All inputs except the clocks are TTL compatible. The output provides a current pulse allowing a large number of devices to be bussed together without compromising system performance due to capacitive loading. The current pulse output is converted to TTL levels by means of a sense amplifier.

features

	MM4262	MM5262
■ Fast access time	470 ns (max)	365 ns (max)
■ Fast cycle time		
Short Read	565 ns (min)	475 ns (min)
Read/Write	750 ns (min)	635 ns (min)
Write	750 ns (min)	635 ns (min)
■ Refresh cycle	1.0 ms	2.0 ms

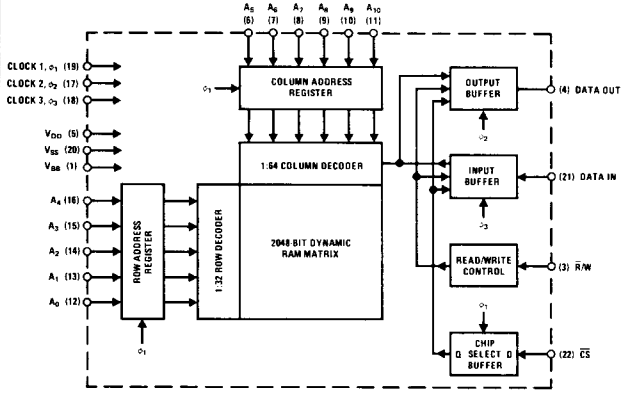
	MM4262	MM5262
■ Low power		
Operating	360 mW (max)	400 mW (max)
Standby	2.5 mW (max)	2.5 mW (max)

- Power supplies +5.0V, +8.5V, −15V
- Low overhead circuits: Fully decoded with internal memory address register
- System oriented design
  - Bipolar compatible except for clocks
  - Current sense output
  - $\overline{\text{Chip Select}}$ for easy memory expansion
- Package 22 pin DIP (Cavity and Molded)
- Device protection: All inputs and outputs protected against static charge

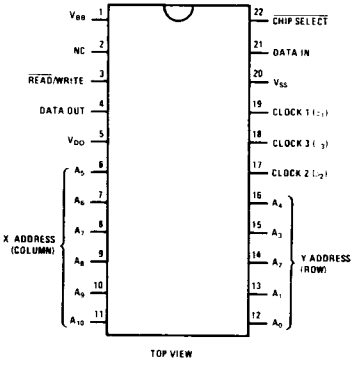
applications

- Core memory replacement
- Mainframe memory
- Buffer storage
- Non-volatile memory using battery back up

block and connection diagrams



Dual-In-Line Package



Order Number MM4262D or MM5262D
See Package 5
Order Number MM5262N
See Package 17

recommended interface circuits

CLOCK DRIVERS:	MH0026 MH8808
SENSE AMPLIFIERS:	LM167 LM168 DM7806/DM8806

absolute maximum ratings (Note 1)

Voltage at Any Pin	V_{BB} + 0.3V to V_{BB} − 27V (Note 16)
Power Dissipation	1.0W
Operating Temperature Range	
MM4262 (T_{CASE})	−55°C to +125°C
MM5262 ($T_{AMBIENT}$)	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics MM4262 ($-55°C \leq T_{CASE} \leq +125°C$, V_{SS} = 5.0V ±0.25V, $V_{BB} - V_{SS}$ = 3.5V ±0.5V, V_{DD} = −15V ±1.0V, unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP (Note 18)	MAX	UNITS
Inputs (Chip Select, Read/Write, Addresses, Data In)	(Notes 14, 15)				
Voltage					
Logical "1" (V_{IH})		V_{SS} 1.5		V_{SS} + 1.0	V
Logical "0" (V_{IL})		V_{SS} 1.0		V_{SS} 4.2	V
Current	$0 \leq V_{IN} \leq V_{SS}$			1.0	μA
Clock Inputs					
Voltage					
Logical "1" ($V_{\phi H}$)		V_{SS} 1.0		V_{SS} + 1.0	V
Logical "0" ($V_{\phi L}$)		V_{DD} 1.0		V_{DD} + 1.0	V
Current	V_{IN} = −16V			50	μA
Outputs	(Note 15)				
Current					
Logical "0" (I_{OL})	V_{OUT} = 0V			100	μA
Logical "1" (I_{OH})	V_{OUT} = 1.2V, $\overline{CS}$ = 0.4V			6.0	mA
	V_{OUT} = 1.8V, $\overline{CS}$ = 0.4V	500			μA
Leakage Current	V_{OUT} = 0V, $\overline{CS}$ = 3.5V			10	μA
Power Supply Current	(Note 17) T_A = 25°C, $V_{BB} - V_{SS}$ = 3.5V, V_{SS} = 5.0V, V_{DD} = −15V, V_{OUT} = 1.2V, Reading 1's at T_{CYCLE} = 750 ns				
(I_{DD})			12	18	mA
(I_{BB})	Operating			150	μA
	Standby (No Clocks)			100	μA

ac electrical characteristics MM4262 (All times measured from 50% points, t_r, $t_f \leq 20$ ns, see ac test circuit and timing diagram, conditions under dc electrical characteristics apply.)

PARAMETER	CONDITIONS	MIN	TYP (Note 18)	MAX	UNITS
ϕ_1 Clock Pulse Width (T_{1PW})	(Note 4)	115	70		ns
ϕ_2 Clock Pulse Width (T_{2PW})	(Note 6)	275	160	400	ns
ϕ_3 Clock Pulse Width (T_{3PW})	(Note 8)	110	60		ns
ϕ_1 Clock to ϕ_2 Clock Delay (T_{12})	(Note 5)	110	60		ns
ϕ_2 Clock to ϕ_3 Clock Delay (T_{23})	(Note 7)	65	10		ns
ϕ_3 Clock to ϕ_1 Clock Delay (T_{31})	(Note 9)	75	40		ns
Chip Select and Address Set Up Time (T_{AS})		100	60		ns
Chip Select and Address Hold Time (T_{AH})		110	50		ns
Read/Write Read Set Up Time (T_{RWS3})		85	30		ns
Read/Write Read Hold Time (T_{RWH3})		65	30		ns
Read/Write Write Set Up Time (T_{RWS1})		95	30		ns
Read/Write Write Hold Time (T_{RWD3})		25	0		ns
Logical "1" Data In Set Up Time (T_{DS1})	(Note 10)	180	60		ns
Logical "0" Data In Set Up Time (T_{DS2})	(Note 10)	75	30		ns
Data In Hold Time (T_{DH1})		70	20		ns
Read Access Time (T_{ACC2})			150	260	ns
Read Access Time (T_{ACC1})	$T_{ACC1} = T_{AS} + T_{12} + T_{ACC2}$		300	470	ns

ac electrical characteristics (con't) MM4262

PARAMETER	CONDITIONS	MIN	TYP (Note 18)	MAX	UNITS
Read Only Cycle ($T_{SHORT/READ}$)	(Note 11)	565			ns
Read, Write, Read Modify Write Cycle (T_{CYCLE})		750			ns
Refresh Time	(Note 12)			1.0	ms
Output Hold Time (T_{OH})	(Note 13)	1000			ns
Chip Select, Address, Read/Write, Data In, Data Out Capacitance (C_X)	(Note 2) $V_{BB} - V_{SS} = 3.5V$, $V_{SS} = 5.0V$ $V_{TEST} = 5.0\ V_{DC}$ With ≤ 15 mV RMS at f = 1 MHz			7.0	pF
ϕ_1 Clock Capacitance (C_1)				50	pF
ϕ_2 Clock Capacitance (C_2)				25	pF
ϕ_3 Clock Capacitance (C_3)				25	pF
Clock Rise/Fall Time				100	ns
Input Rise/Fall Time				50	ns

dc electrical characteristics MM5262 $0°C \leq T_A \leq +70°C$, $V_{SS} = 5.0V \pm 0.25V$, $V_{BB} - V_{SS} = 3.5V \pm 0.5V$, $V_{DD} = -15V \pm 1.0V$, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP (Note 18)	MAX	UNITS
Inputs (Chip Select, Read/Write, Addresses, Data In)	(Notes 14 and 15)				
Voltage					
Logical "1" (V_{IH})		$V_{SS} - 1.5$		$V_{SS} + 1.0$	V
Logical "0" (V_{IL})		$V_{SS} - 10$		$V_{SS} - 4.2$	V
Current	$0V \leq V_{IN} \leq V_{SS}$			1.0	μA
Clock Inputs					
Voltage					
Logical "1" ($V_{\phi H}$)		$V_{SS} - 1.0$		$V_{SS} + 1.0$	V
Logical "0" ($V_{\phi L}$)		$V_{DD} - 1.0$		$V_{DD} + 1.0$	V
Current	$V_{IN} = -16V$			50	μA
Output	(Note 15)				
Current					
Logical "0" (I_{OL})	$V_{OUT} = 0V$			100	μA
Logical "1" (I_{OH})	$V_{OUT} = 1.2V$, $\overline{CS} = 0.4V$			6.0	mA
	$V_{OUT} = 1.8V$, $\overline{CS} = 0.4V$	600			μA
Leakage Current	$V_{OUT} = 0V$, $\overline{CS} = 3.5V$			10	μA
Power Supply Current	(Note 17) $T_A = 25°C$, $V_{BB} - V_{SS} = 3.5V$, $V_{SS} = 5.0V$, $V_{DD} = -15V$, $V_{OUT} = 1.2V$, Reading 1's at $T_{CYCLE} = 635$ ns				
(I_{DD})	Operating		13	20	mA
(I_{BB})	Standby (No Clocks)			150	μA
				100	μA

ac electrical characteristics MM5262 (All times measured from 50% points, t_r, $t_f \leq 20$ ns, see ac test circuit and timing diagram, conditions under dc electrical characteristics apply.)

PARAMETER	CONDITIONS	MIN	TYP (Note 13)	MAX	UNITS
ϕ_1 Clock Pulse Width (T_{1PW})	(Note 4)	95	70		ns
ϕ_2 Clock Pulse Width (T_{2PW})	(Note 6)	240	160	400	ns
ϕ_3 Clock Pulse Width (T_{3PW})	(Note 8)	100	60		ns
ϕ_1 Clock to ϕ_2 Clock Delay (T_{12})	(Note 5)	90	60		ns
ϕ_2 Clock to ϕ_3 Clock Delay (T_{23})	(Note 7)	50	10		ns
ϕ_3 Clock to ϕ_1 Clock Delay (T_{31})	(Note 9)	60	40		ns
Chip Select and Address Set Up Time (T_{AS})		80	60		ns
Chip Select and Address Hold Time (T_{AH})		90	50		ns
Read/Write Read Set Up Time (T_{RWS3})		70	30		ns
Read/Write Read Hold Time (T_{RWH3})		65	30		ns
Read/Write Write Set Up Time (T_{RWS1})		75	30		ns

ac electrical characteristics (con't) MM5262

PARAMETER	CONDITIONS	MIN	TYP (Note 18)	MAX	UNITS
$\overline{\text{Read}}$/Write Write Hold Time (T_{RWO3})		25	0		ns
Logical "1" Data In Set Up Time (T_{DS1})	(Note 10)	120	60		ns
Logical "0" Data In Set Up Time (T_{DS2})	(Note 10)	60	30		ns
Data In Hold Time (T_{DH1})		50	20		ns
Read Access Time (T_{ACC2})			150	195	ns
Read Access Time (T_{ACC1})	$T_{ACC1} = T_{AS} + T_{12} + T_{ACC2}$		300	365	ns
Read Only Cycle ($T_{SHORT/READ}$)	(Note 11)	475			ns
Read, Write, Read Modify Write Cycle (T_{CYCLE})		635			ns
Refresh Time	(Note 12)			2.0	ms
Output Hold Time (T_{OH})	(Note 13)	1000			ns
$\overline{\text{Chip Select}}$, Address, $\overline{\text{Read}}$/Write, Data In, Data Out Capacitance (C_X)	(Note 2) $V_{BB} - V_{SS} = 3.5V$, $V_{SS} = 5.0V$ $V_{TEST} = 5.0\ V_{DC}$ With ≤ 15 mV RMS at f = 1.0 MHz			7.0	pF
ϕ_1 Clock Capacitance (C_1)				50	pF
ϕ_2 Clock Capacitance (C_2)				25	pF
ϕ_3 Clock Capacitance (C_3)				25	pF
Clock Rise/Fall Time				100	ns
Input Rise/Fall Time				50	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: Positive true logic notation is used: Logic "1" = most positive voltage level
Logic "0" = most negative voltage level

Note 4: T_{1PW}, ϕ_1 clock – used to change input logic address and $\overline{\text{chip select}}$.

Note 5: T_{12}, interval between clock 1 and 2 – for decode.

Note 6: T_{2PW}, ϕ_2 clock – cell access.

Note 7: T_{23}, interval between clock 2 and 3 – decision time.

Note 8: T_{3PW}, ϕ_3 clock – write or refresh clock.

Note 9: T_{31}, write recovery time.

Note 10: If a "1" is being written then data in must go high T_{DS1} before the end of ϕ_2 and remain in that state until T_{DH1} after ϕ_3 goes low. If a "0" is being written, data in must go low at least T_{DS2} before ϕ_3, and remain in that state until T_{DH1} after ϕ_3 goes low.

Note 11: For a short read cycle, ϕ_3 may be inhibited and the next cycle may begin T_{23} after ϕ_2.

Note 12: Addresses A_0 through A_4 are the row addresses. To accomplish a refresh, at least one location in each row must be accessed during any 2 ms period for the MM5262 and 1 ms for the MM4262. The row will refresh when reading or writing with the chip disabled or enabled as long as ϕ_3 is applied.

Note 13: During a read cycle the output will remain valid until the next ϕ_1 or T_{OH} whichever is less. During a read modify write or write cycle the output will remain valid until ϕ_3 time.

Note 14: The chip is enabled when $\overline{\text{chip select}}$ is at a logic "0."

Note 15: If a logic "1" (3.5V) is written, when it is read the output will source more than 600μA.

Note 16: Under power turn on conditions care must be taken to insure that V_{BB} is always the most positive potential in the system or large transient currents could result, causing permanent damage.

Note 17: An approximate relationship for I_{DD} is:

$$I_{DD\,max} = A\frac{T_{1PW}}{T_{CYC}} + B\frac{T_{2PW}}{T_{CYC}} + C\frac{1000\text{ ns}}{T_{CYC}}$$

where: A = 20 @ 25°C A = 23 @ 0°C A = 32 @ −55°C
B = 4.5 @ 25°C B = 5.2 @ 0°C B = 7.2 @ −55°C
C = 10 @ 25°C C = 10 @ 0°C C = 12 @ −55°C

Note 18: Typical values for $T_A = 25°C$, $V_{SS} = 5.0V$, $V_{BB} = 8.5V$, and $V_{DD} = -15V$.

timing and operation

The MM4262/MM5262 has four basic modes of operation: (1) read, (2) write, (3) read modify write and (4) refresh. Each, of these modes, is commonly used in memory systems. To make the timing and control considerations perfectly clear each mode will be discussed separately.

READ OPERATION

The read operation consists of reading previously stored data out of randomly selected address locations. The read operation may be performed in one of two ways.

The first method is by use of the $\overline{\text{Read/Write}}$ control. As indicated in Figure 1, if the $\overline{\text{Read/Write}}$ input goes low, for at least the time specified by $T_{RWS3} + T_{RWH3}$, the information will be read out of the selected memory location. The output will remain valid for $T_{OH(max)}$ or until the next ϕ_1 clock pulse, whichever is less.

The second method involves gating the ϕ_3 clock pulse. A write operation can only occur when the ϕ_3 clock is present. Thus by applying a logical "1" to the $\overline{\text{Read/Write}}$ control (write mode) and not applying the ϕ_3 clock, the memory will read out information from the selected location. In other words the memory will be operating in the read mode. There are advantages in gating the ϕ_3 clock. First, since ϕ_3 clock is a high level signal, power will be reduced. Second, since in the read mode ϕ_3 has been eliminated, ϕ_1 may be applied after the T_{23} delay. This will shorten the read cycle by the $T_{3PW} + T_{31}$ interval. The short read cycle is then:

$$T_{SHORT\ READ} = T_{CYCLE} - (T_{3PW} + T_{31})$$
$$= (635 - 160)\ ns = 475\ ns \text{ for MM5262}$$
$$= (750 - 185)\ ns = 565\ ns \text{ for MM4262}$$

WRITE OPERATION

The write operation consists of storing new information into randomly selected address locations. Just as in the case of the read mode, write may be performed by using the $\overline{\text{Read/Write}}$ control or by gating the ϕ_3 clock. The ϕ_3 clock is essential to the write operation and unless it is present, a write will not occur regardless of the state of the $\overline{\text{Read/Write}}$ control.

READ MODIFY WRITE OPERATION

The read modify write operation consists of reading information out of a randomly selected memory location and then writing new information into this same location. The important point to remember in understanding this mode is that information is always read out of the selected address location regardless of the state of the $\overline{\text{Read/Write}}$ control. In this sense, the $\overline{\text{Read/Write}}$ control may be thought of as a write inhibit control.

Then, in the write mode, information will be output T_{ACC2} after the leading edge of the ϕ_2 clock and held until the start of the ϕ_3 clock. The write operation procedes in a normal manner and new information, present on the Data In line, will be written into the selected memory location.

If the Data In and Data Out lines are interfaced to a common data I/O bus, the T_{23} interval must be increased a sufficient amount to transfer the read data onto the common I/O bus and to change the I/O bus to the new information to be written. This, of course, will increase T_{CYC} by the same amount that T_{23} is increased.

REFRESH OPERATION

Because the storage mechanism of a dynamic RAM is charge retention on a capacitor, and leakage paths exist, these capacitors must be recharged or "refreshed" periodically. For the MM5262 the maximum time between refresh intervals must be less than or equal to 2.0 ms. For the MM4262 the maximum refresh interval is 1.0 ms.

The MM4262/MM5262 refreshes on a row basis. That is, when any location within a row is refreshed all locations in that row are refreshed. There are 32 rows in the RAM matrix, corresponding to addresses A_0 through A_4.

Refresh is accomplished within a row whenever the ϕ_3 clock is applied. It does not matter if the memory is in read mode, write mode, selected or not selected. The most common method of refreshing the memory is to place $\overline{CS}$ at V_{IH} and sequence the clocks through a normal read or write cycle with the ϕ_3 clock applied. Note that if, during normal system operation, each row is written into or read out of at an interval of 2.0 ms (1.0 ms for the MM4262) or less, refresh is not required as a separate operation.

Now that the four modes of operation have been defined a step by step description of a write cycle will serve to further clarify the operation of the MM4262/MM5262 RAM.

Any cycle is initiated by the leading edge of the ϕ_1 clock. For a device to be selected it must receive a ϕ_1 clock and $\overline{CS}$ must be at V_{IL} for the interval specified by T_{AS} and T_{AH}. Note that the ϕ_1 clock must be applied to deselect a device also (see block diagram). When a device is not selected, the output buffer assumes a high impedance state and the input buffer inhibits input data.

In addition to gating $\overline{CS}$ information into the device, the ϕ_1 clock also gates in address information (see block diagram). Address inputs, A_0 through A_{10}, must be stable for the interval specified by T_{AS} and T_{AH}.

timing and operation (con't)

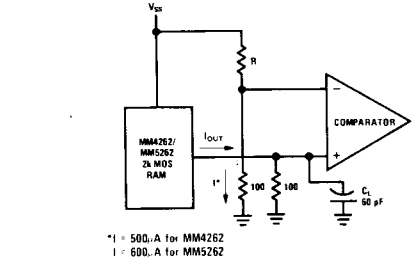
Assuming the read/write operation is to be controlled by the $\overline{\text{Read}}$/Write input, this input must be at V_{IH} for an interval of T_{RWS1} prior to the trailing edge of ϕ_1 clock, and remain at V_{IH} until T_{RWD3} after the trailing edge of the ϕ_3 clock. Note that if the $\overline{\text{Read}}$/Write input is low, during the T_{RWS3} plus T_{RWH3} interval the write operation is internally inhibited, allowing only a refresh to occur.

The ϕ_2 clock gates the information corresponding to the selected address through the output buffer (see block diagram) to the Data Out pin. The delay from leading edge of the ϕ_2 clock to valid data out is T_{ACC2}, Read Access Time. Note that even though the memory is in the write mode, data is being read out. Data out will remain valid only until the start of the ϕ_3 clock, because $\overline{\text{Read}}$/Write is at V_{IH}.

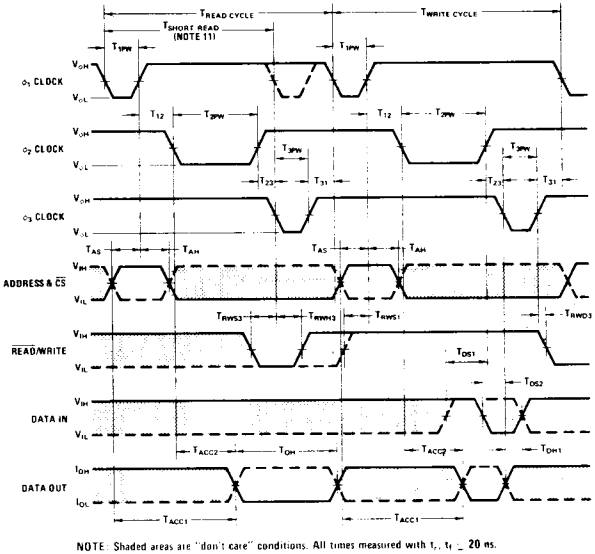
The actual write operation, as stated previously, is controlled by the ϕ_3 clock. The amount of time Data In must be stable is dependent on whether a logical "1" or a logical "0" is to be written. If a logical "1" is to be written, Data In must be stable T_{DS1} prior to the trailing edge of the ϕ_2 clock and remain stable until T_{DH1} after the leading edge of the ϕ_3 clock. If a logical "0" is to be written, Data In must be stable T_{DS2} prior to the leading edge of the ϕ_3 clock and remain stable until T_{DH1} after the leading edge of the ϕ_3 clock.

T_{31} after the trailing edge of the ϕ_3 clock another ϕ_1 clock may be applied to initiate the next cycle. Note that if the next address location is in another device the ϕ_1 clock must still be applied to deselect the current device. This becomes important when clock decoding is used to reduce power consumption in a memory system (see Application Note AN-86).

ac test circuit and switching time waveforms



*I = 500μA for MM4262
I = 600μA for MM5262



NOTE: Shaded areas are "don't care" conditions. All times measured with t_r, t_f = 20 ns.

FIGURE 1.