EM27C010 1-Megabit (128K x 8) UVPROM

Features

- **Functional Compatible to AMD, TI, WSI's 27C010**
- **Fast Read Access Time – 70 ns**
- **Low-Power CMOS Operation**
  - **– 100 µA Max Standby**
  - **– 30 mA Max Active at 5 MHz**
- **JEDEC Standard Packages – 32-lead ceramic DIP**
- **5V ± 10% Supply**
- **Rapid Programming Algorithm – 100 µs/Byte (Typical)**
- **CMOS and TTL Compatible Inputs and Outputs**
- **Integrated Product Identification Code**
- **Industrial, Extended Temperature Ranges and Military Screening**

1. Description

The EM27C010 is fabricated using high-density nonvolatile memory CMOS process and is assembled and tested in EM Semi approved assembly and test facilities. The device is offered in industrial, extended and a version screened to a military test flow.

The EM27C010 is a low-power, high-performance 1,048,576-bit UVPROM organized 128K by 8 bits. It requires only one 5V power supply in normal read mode operation. Any byte can be accessed as fast as 70 ns, eliminating the need for speed reducing WAIT states on high-performance microprocessor systems.

The EM27C010 is available in industry-standard JEDEC-approved ceramic DIP packages. All devices feature two-line control (CE_{NOT}, OE_{NOT}) to give designers the flexibility to prevent bus contention.

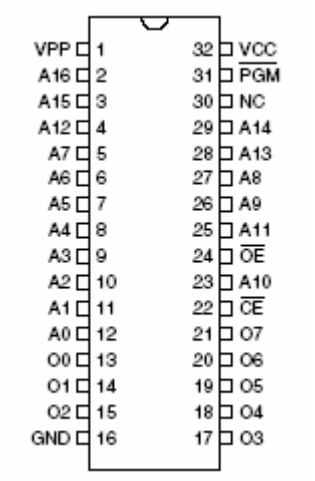
With 128K byte storage capability, the EM27C010 allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

EM27C010 has additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry-standard programming equipment to select the proper programming algorithms and voltages.

2. Pin Configurations

Pin Name	Function
A0 – A16	Addresses
O0 – O7	Outputs
CE_{NOT}	Chip Enable
OE_{NOT}	Output Enable
PGM_{NOT}	Program Strobe
V_{PP}	Program Supply
V_{CC}	Supply Voltage
GND	Ground
NC	Not Connected

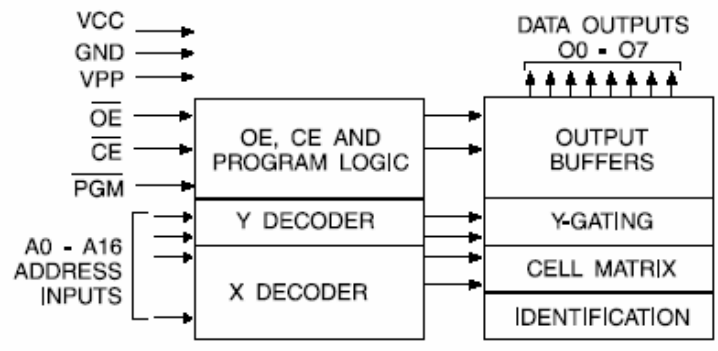
2.1 32-lead Ceramic DIP Top View



3. System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed datasheet limits, resulting in device non-conformance. At a minimum, a 0.1 µF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

4. Block Diagram



5. Absolute Maximum Ratings*

Temperature Under Bias..... -55°C to + 125°C
Storage Temperature ..... -65°C to + 150°C
Supply Voltage…… -2.0V to +7.0V
Voltage on Any Pin with
Respect to Ground .....-2.0V to + 7.0V(1)
Voltage on A9 with
Respect to Ground .....-2.0V to + 13.5V(1)
V_{PP} Supply Voltage with
Respect to Ground .....-2.0V to + 14.0V(1)

* NOTICE:
Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
1. Minimum voltage is -0.5V DC which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.5V DC which may overshoot to +7.0 volts for pulses of less than 20 ns.

6. Operating Modes

Mode/Pin	CE_{NOT}	OE_{NOT}	PGM_{NOT}	A9	Vpp	Outputs
Read	V_{IL}	V_{IL}	X	X	V_{CC} or GND	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X	X	V_{CC} or GND	High Z
Standby	V_{IH}	X	X	X	V_{CC} or GND	High Z
Rapid Program(2)	V_{IL}	V_{IH}	V_{IL}	X	V_{PP}	D_{IN}
PGM Verify	V_{IL}	V_{IL}	V_{IH}	X	V_{PP}	D_{OUT}
PGM Inhibit	V_{IH}	X	X	X	V_{PP}	High Z
Product Identification(4)	V_{IL}	V_{IL}	V_{IH}	V_H	V_{CC}	Identification Code

Notes:
1. X can be V_{IL} or V_{IH}.
2. Refer to Programming Characteristics.
3. V_H = 12.0 ± 0.5V.

7. DC and AC Operating Conditions for Read Operation

		EM27C010
		-70 / -90 / -120
Operating Temp.(Case)	Industrial	-40°C - 85°C
	Extended	-45°C - 115°C
	Military	-55°C - 125°C
V_{CC} Supply		5V ± 10%

8. DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}	Ind.		±10	µA
			Mil.		±10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}	Ind.		±10	µA
			Mil.		±10	µA
$I_{PP(2)}$	V_{PP} Read/Standby Current	Vpp = Vcc			10	µA
I_{SB}	V_{CC} Standby Current	I_{SB1}(CMOS), CE_{NOT} = V_{CC} - 0.2V			100	µA
		I_{SB2}(TTL), CE_{NOT} = V_{IH}			1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT}= 0 mA, CE_{NOT}, OE_{NOT}= V_{IL}			30	mA
V_{IL}	Input Low Voltage			-0.3	0.8	V
V_{IH} (2)	Input High Voltage			2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	V_{OH}(CMOS), I_{OH}= -100 µA		V_{CC} – 0.7		V
		V_{OH}(TTL), I_{OH}= -400 µA		2.4		

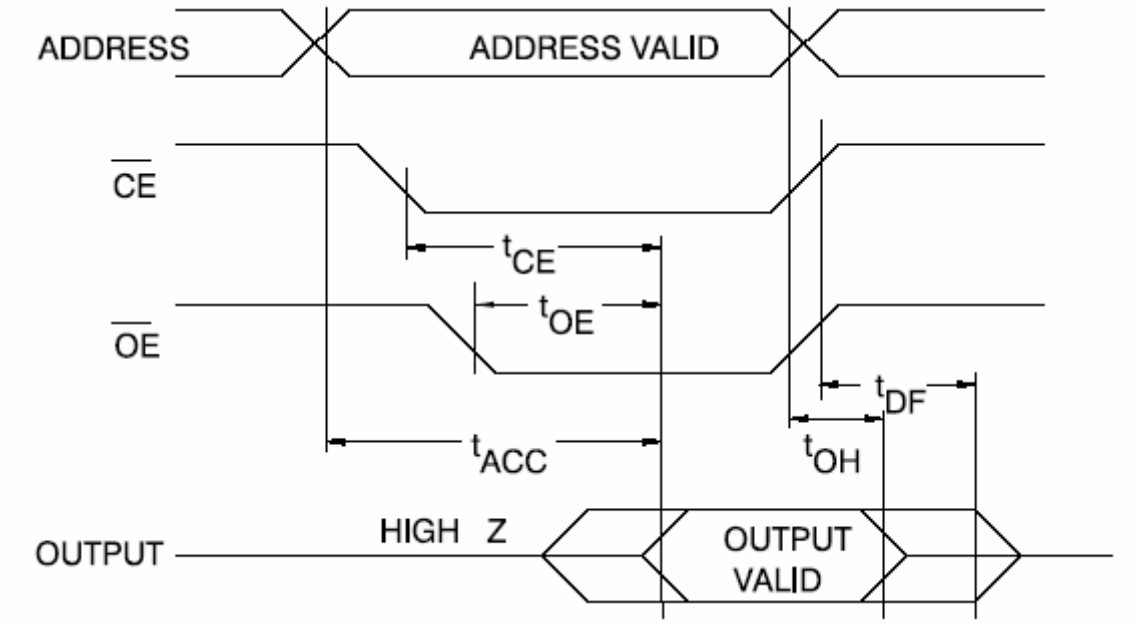
Note:

1. V_{CC} must be applied simultaneously with or before V_{PP}, and removed simultaneously with or after V_{PP}.
2. Maximum DC voltage on Output is V_{CC} + 0.5V.

9. AC Characteristics for Read Operation

Symbol	Parameter	Condition	EM27C010						Units
			-70		-90		-120		
			Min	Max	Min	Max	Min	Max	
t_{ACC}(3)	Address to Output Delay	$CE_{NOT} = OE_{NOT} = V_{IL}$		70		90		120	ns
t_{CE}(2)	CE_{NOT} to Output Delay	$OE_{NOT} = V_{IL}$		70		90		120	ns
t_{OE}(2) (3)	OE_{NOT} to Output Delay	$CE_{NOT} = V_{IL}$		35		45		60	ns
t_{DF}(4) (5)	OE_{NOT} or CE_{NOT} High to Output Float, Whichever Occurred First			30		30		40	ns
t_{OH}	Output Hold from Address, CE_{NOT} or OE_{NOT}, Whichever Occurred First	$CE_{NOT} = OE_{NOT} = V_{IL}$	0		0		0		ns

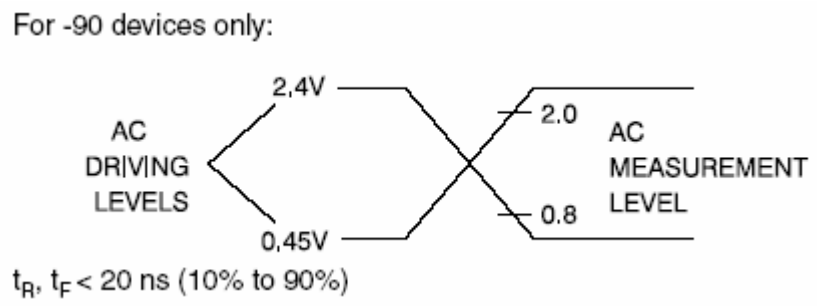
10. AC Waveforms for Read Operation(1)



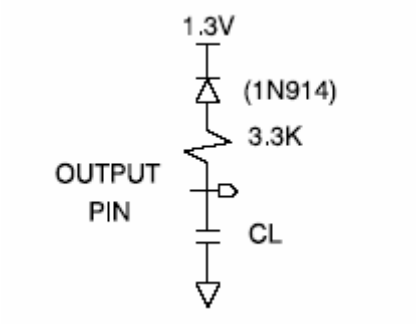
Notes:

1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. OE_{NOT} may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of CE_{NOT} without impact on t_{CE}.
3. OE_{NOT} may be delayed up to $t_{ACC} - t_{OE}$ after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

11. Input Test Waveforms and Measurement Levels



12. Output Test Load



Note:

1. C_L = 100 pF including jig capacitance, except for high speed devices, where C_L = 30 pF.

13. Pin Capacitance

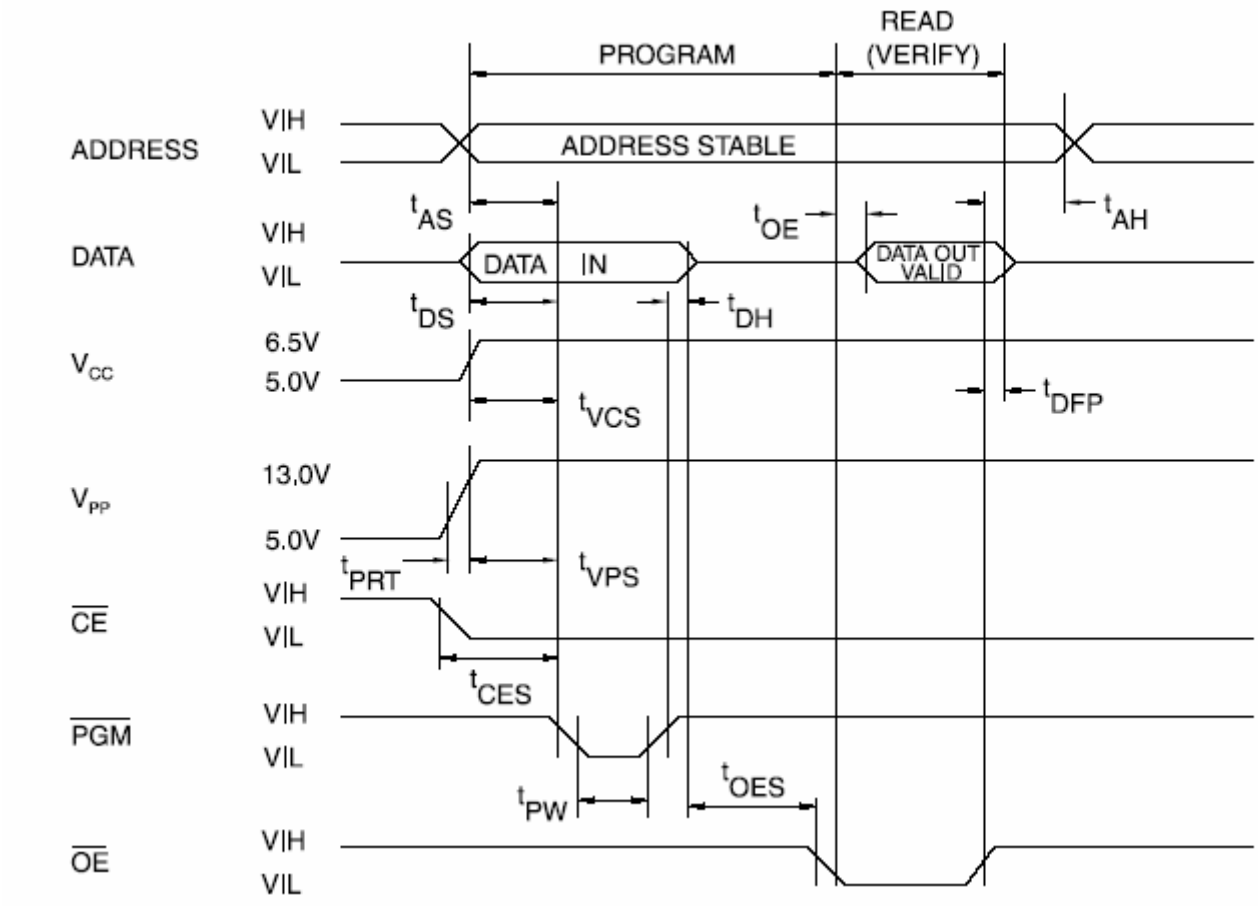
f = 1 MHz, T_A = 25°C (1)

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	V_{IN}= 0V
C_{OUT}	8	12	pF	V_{OUT}= 0V

Note:

1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

14. Programming Waveforms(1)



Notes:

1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.

2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

3. When programming the EM27C010, a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

15. DC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.00 ± 0.25V

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
I_{LI}	Input Load Current	0 <= V_{IN} <= V_{IH}		±10	µA
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			50	mA
I_{PP2}	V_{PP} Supply Current	CE_{NOT} = PGM_{NOT}=V_{IL}		50	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

16. AC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.00 ± 0.25V

Symbol	Parameter	Test Conditions(1)	Limits		Units
			Min	Max	
t_{AS}	Address Setup Time		2		µs
t_{CES}	CE_{NOT} Setup Time		2		µs
t_{OES}	OE_{NOT} Setup Time	Input Rise and Fall Times	2		µs
t_{DS}	Data Setup Time	(10% to 90%) 20 ns	2		µs
t_{AH}	Address Hold Time	Input Pulse Levels	0		µs
t_{DH}	Data Hold Time	0.45V to 2.4V	2		µs
t_{DFP}	OE_{NOT} High to Output Float Delay(2)	Input Timing Reference Level	0	130	ns
t_{VPS}	V_{PP} Setup Time	0.8V to 2.0V	2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	PGM_{NOT} Program Pulse Width(3)	Output Timing Reference Level	95	105	µs
t_{OE}	Data Valid from OE_{NOT}	0.8V to 2.0V		100	ns
t_{PRT}	V_{PP} Pulse Rise Time During Programming		50		ns

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven – see timing diagram.

3. Program Pulse width tolerance is 100 µsec ± 5%.

17. Integrated Product Identification Code

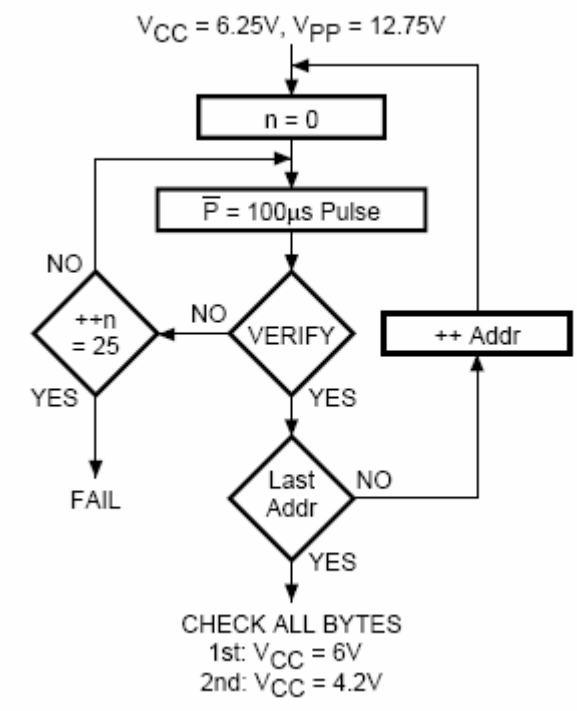
Codes	Pins									Hex Data
	A0	O7	O6	O5	O4	O3	O2	O1	O0	
Manufacturer	V_{IL}	0	0	1	0	0	0	0	0	20
Device Type	V_{IH}	0	0	0	0	0	1	0	1	05

18. Programming Algorithm

When delivered (and after each erasure for UVPROM), all bits of the EM27C010 are in the '1' state. Data is introduced by selectively programming '0's into the desired bit locations. Although only '0's will be programmed, both '1's and '0's can be present in the data word. The only way to change a '0' to a '1' is by die exposure to ultraviolet light (UVPROM). The EM27C010 is in the programming mode when V_{PP} input is at 12.75V, E is at V_{IL} and P is pulsed to V_{IL}. The data to be programmed is applied to 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

Rapid Programming Algorithm

Rapid Programming Algorithm allows the whole array to be programmed with a guaranteed margin, in a typical time of 26.5 seconds. Rapid programming consists of applying a sequence of 100µs program pulses to each byte until a correct verify occurs (see figure). During programming and verify operation, a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in MARGIN MODE provides the necessary margin to each programmed cell.



19. Ordering Information

EM27C010 – XX X X