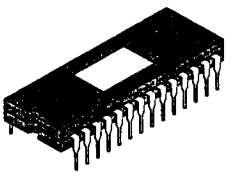
SONY CXK27C512DQ -15/20

65536-word × 8-bit Ultraviolet Erasable CMOS EPROM

Description

The CXK27C512DQ is an electrically programmable, ultraviolet erasable CMOS EPROM. The adoption of CMOS for the peripheral circuits allows for high speed operation and low power consumption. Ideally suited for 8-bit microprocessor systems requiring large program memories, this IC is organized as 65536-word by 8-bit in a 28 pin Frit-Seal package.

28 pin DIP (Ceramic)



Features

- Fast access time : (Access time)
  CXK27C512DQ-15 150ns (Max.)
  CXK27C512DQ-20 200ns (Max.)
- Low current consumption
  at operation current 50mA (Max.)
  at standby 1mA (Max.)
- At read out 5V single supply operation :
  5V ± 10%
- Directly TTL compatible :
  All inputs and outputs
- 3-state output
- High speed program mode
- 600-mil 28 pin ceramic DIP package

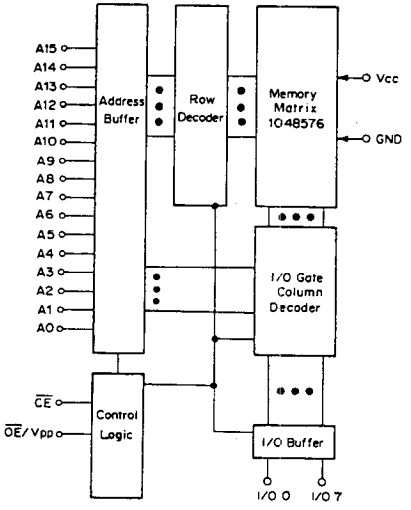
Function

65536-word × 8-bit EPROM

Structure

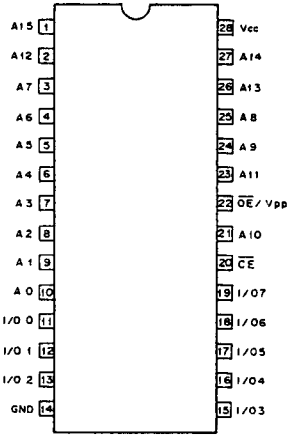
Silicon Stacked-gate CMOS IC

Block Diagram



Pin Configuration

(Top View)



Pin Description

Symbol	Description
A0 to A15	Address input
I/O0 to I/O7	Data I/O
$\overline{CE}$	Chip enable input
$\overline{OE}$/Vpp	Output enable input/Program power supply
Vcc	+5V power supply
GND	GND

E89Y40 – ST

Absolute Maximum Ratings (Ta = 25℃, GND = 0V)

Item	Symbol	Ratings	Unit
Supply voltage	Vcc	− 0.6 to + 7.0	V
	Vpp	− 0.6 to + 14	V
Input voltage	A9	− 0.6 to + 13.5	V
	V_{IN}	− 0.6 to + 6.5	V
Output voltage	$V_{I/O}$	− 0.6 to + 6.5	V
Operating temperature	Topr	− 10 to + 80	℃
Storage temperature	Tstg	− 65 to + 125	℃

Exposure to stress exceeding the Absolute Maximum Ratings may not only adversely affect reliability but at the worst, destroy the device.

Truth Table

$\overline{CE}$	$\overline{OE}$/ Vpp	A9	Mode	I/O pin
L	L	X	Read	Data output
L	H	X	Output disable	High impedance
H	X	X	Standby	High impedance
L	Vpp	X	Program	Data input
H	Vpp	X	Program inhibit	High impedance
L	L	V_H	Electronic signature	Device code output

Set X to either "H" or "L", $V_H = 12V \pm 0.5V$

Read Mode

Recommended Operating Conditions

(Ta = 0 to + 70℃, GND = 0V, Vpp = Vcc*)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.0	—	Vcc + 0.5	V
Input low voltage	V_{IL}	− 0.1	—	0.8	V

* Vpp must be applied simultaneously or after Vcc and removed simultaneously or before Vcc.

Electrical Characteristics

• DC characteristics

(V_{CC} = 5V ± 10%, V_{PP} = V_{CC}, GND = 0V, Ta = 0 to + 70°C)

Item	Symbol	Test conditions	Min.	Typ.*	Max.	Unit
Input leakage current	I_{LI}	V_{IN} = 5.5V	− 10	—	10	μA
Output leakage current	I_{LO}	$V_{I/O}$ = 5.5V	− 10	—	10	μA
Vcc average operating supply current	I_{CC1}	Cycle time 100ns Duty = 100% I_{OUT} = 0mA $\overline{CE}$ = $\overline{OE}$ = V_{IL}	—	—	50	mA
Vcc standby supply current	I_{SB}	$\overline{CE}$ = V_{IH}	—	—	1	mA
Vpp supply current	I_{PP1}		—	—	0.1	mA
Output high voltage	V_{OH}	I_{OH} = − 400 μA	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL} = 2.1mA	—	—	0.45	V

* Vcc = 5V, Ta = 25°C

I/O capacitance

(Ta = 25°C, f = 1MHz)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	4	6	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	8	12	pF

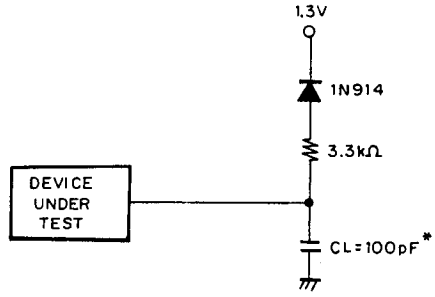
Note) This parameter is sampled and is not 100% tested.

AC characteristics

• AC test conditions

(V_{CC} = 5V ± 10%, V_{PP} = V_{CC}, Ta = 0 to + 70°C)

Item	Conditions
Input pulse high voltage	V_{IH} = 2.4V
Input pulse low voltage	V_{IL} = 0.45V
Input rise time	tr ≦ 20ns
Input fall time	tf ≦ 20ns
I/O reference level	2V/0.8V
Load condition	Right figure

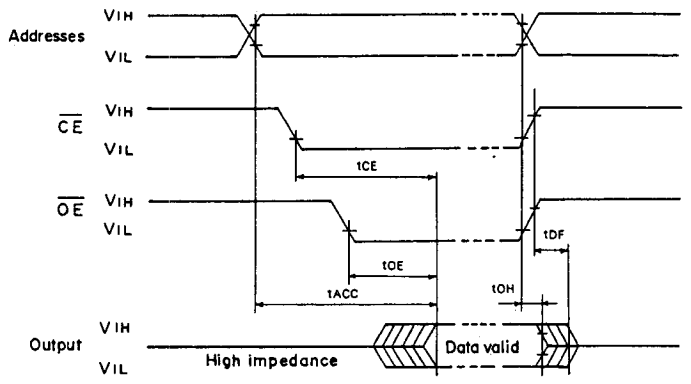


* C_L includes scope and jig capacitances.

Item	Symbol	−15		−20		Unit
		Min.	Max.	Min.	Max.	
Address access time	t_{ACC}	—	150	—	200	ns
Chip enable access time	t_{CE}	—	150	—	200	ns
Output enable access time	t_{OE}	—	60	—	70	ns
Output data hold time	t_{OH}	0	—	0	—	ns
Output disable time	t_{DF} *	0	50	0	60	ns

* t_{DF} is defined by the time required by the output to reach high impedance. It is not determined by the output voltage level. This parameter is only sampled and is not 100% tested.

Timing Waveform (Read cycle)



Programming Operation

Recommended Operating Conditions (Ta = 25 ± 5°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Vcc supply voltage	V_{CC}*1	6.00	6.25	6.50	V
Vpp program supply voltage	V_{PP}*2	12.50	12.75	13.00	V
Input high voltage	V_{IH}	2.0		Vcc + 0.5V	V
Input low voltage	V_{IL}	− 0.1		0.8	V

*1 Vcc must be applied before Vpp and removed after Vpp.
*2 Keep Vpp below 14V including overshoot.
Extraction of the device while 12.75V is applied to Vpp may impair reliability.

Electrical Characteristics

• DC characteristics

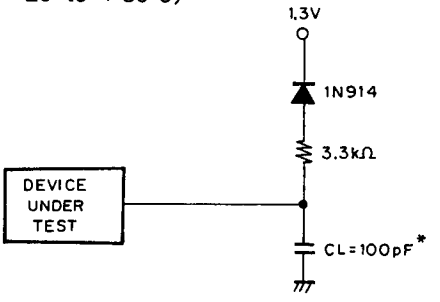
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input leakage current	I_{LI}	$V_{IN} = V_{IL}$ or V_{IH}	− 10	—	10	μA
Vcc supply current	I_{CC2}		—	—	50	mA
Vpp supply current	I_{PP2}	$\overline{CE} = V_{IL}$	—	—	50	mA
Output high voltage (at verify)	V_{OH}	$I_{OH} = -400\,\mu A$	2.4	—	—	V
Output low voltage (at verify)	V_{OL}	$I_{OL} = 2.1\,mA$	—	—	0.45	V
A9 electronic signature	V_{ID}		11.5	12.0	12.5	V

AC Characteristics

• AC test conditions

(Vcc = 6.25 ± 0.25V, Vpp = 12.75 ± 0.25V, Ta = 20 to + 30°C)

Item	Conditions
Input pulse high voltage	V_{IH} = 2.4V
Input pulse low voltage	V_{IL} = 0.45V
Input rise time	tr ≦ 20ns
Input fall time	tf ≦ 20ns
I/O reference level	2V/0.8V
Load conditions	Right figure

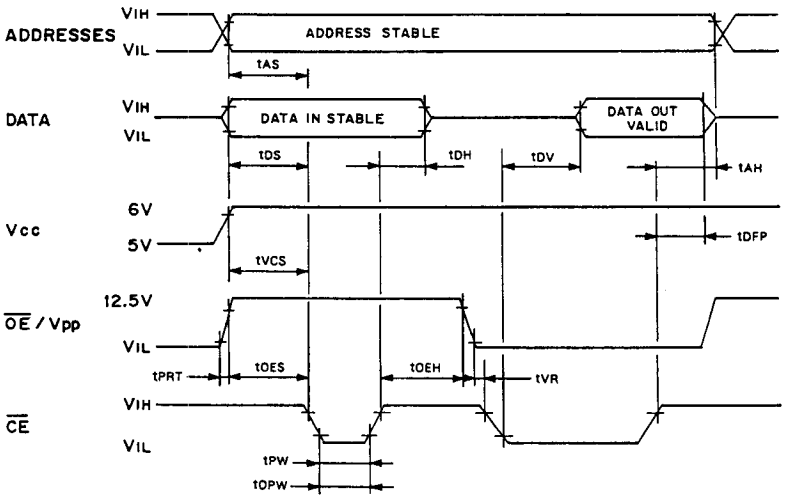


* C_L includes scope and jig capacitances.

Item	Symbol	Min.	Max.	Unit
Address setup time	t_{AS}	2		µs
$\overline{OE}$ setup time	t_{OES}	2		µs
$\overline{OE}$/Vpp hold time	t_{OEH}	2		µs
Data setup time	t_{DS}	2		µs
Address hold time	t_{AH}	0		µs
Data hold time	t_{DH}	2		µs
$\overline{OE}$ high to output float delay	t_{DFP}*	0	130	ns
Vcc setup time	t_{VCS}	0		µs
Program pulse width	t_{PW}	95	105	µs
Data valid from $\overline{CE}$	t_{DV}		1	ns
$\overline{OE}$/Vpp recovery time	t_{VR}	2		µs
$\overline{OE}$/Vpp pulse rise time	t_{PRT}	50		ns

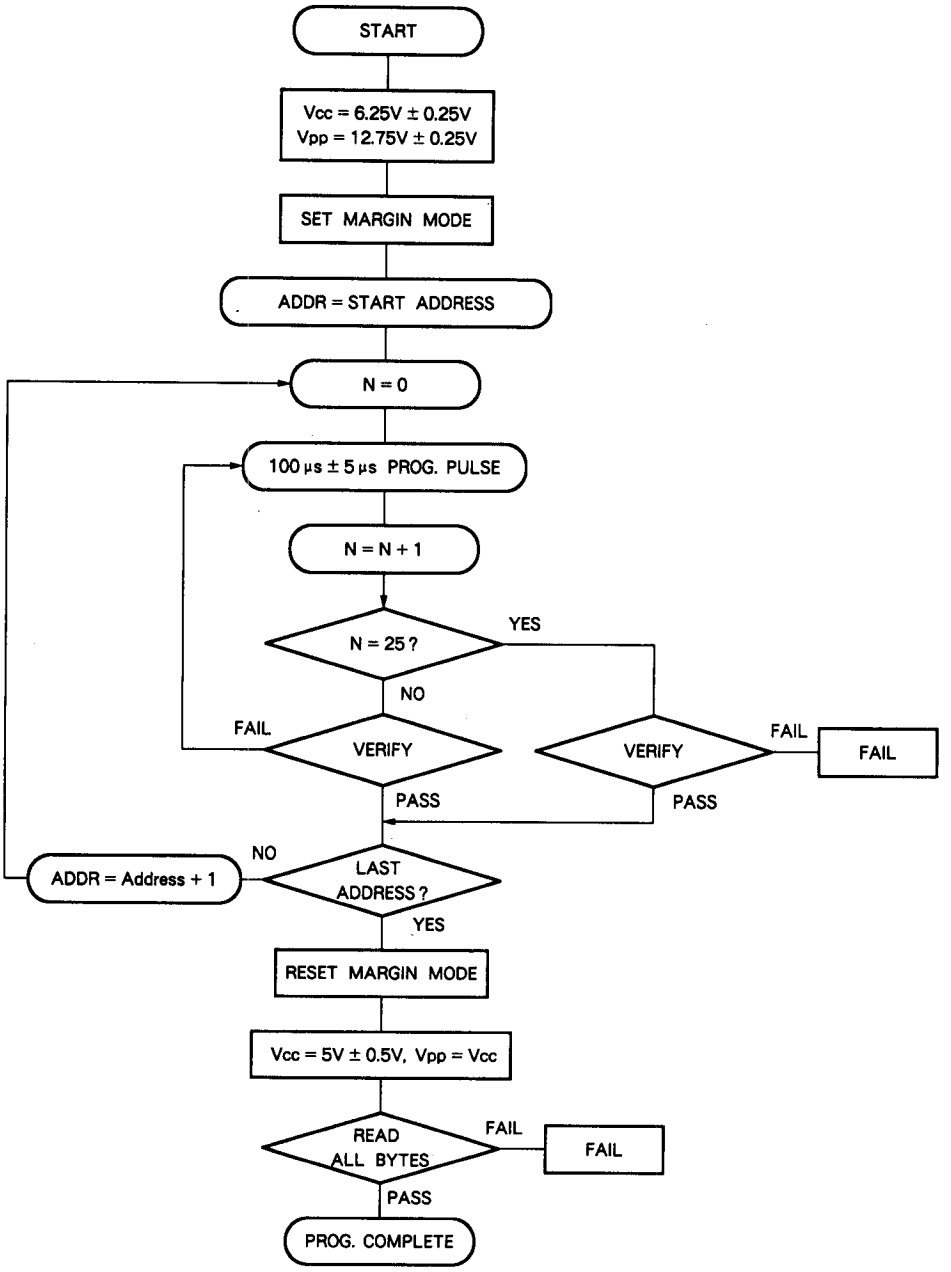
* t_{DFP} is defined by the time required by the output to reach high impedance. It is not determined by the output voltage level. This parameter is only sampled and is not 100% tested.

Timing Waveform (Program)



Note) When programming the CXK27C512DQ a 0.1 µF capacitor is required access $\overline{OE}$/Vpp and GND to suppress switching noise caused by Vpp transient current.

High Speed Programming Method Flow Chart



Erasure Operation

The recommended erasure procedure for the CXK27C512DQ ("0" to "1") is exposure to ultraviolet light of a 2537 Å wavelength through the translucent window. The exposure dose (i.e. UV intensity X exposure time) for erasure should be at a minimum of 15W-sec/cm². The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with an illuminance of 12000 μW/cm² on the package surface placed within 2 to 3cm of the lamp tubes. Moreover, erasure may require larger periods according to the ultraviolet lamp life and the dirt on the quartz window.

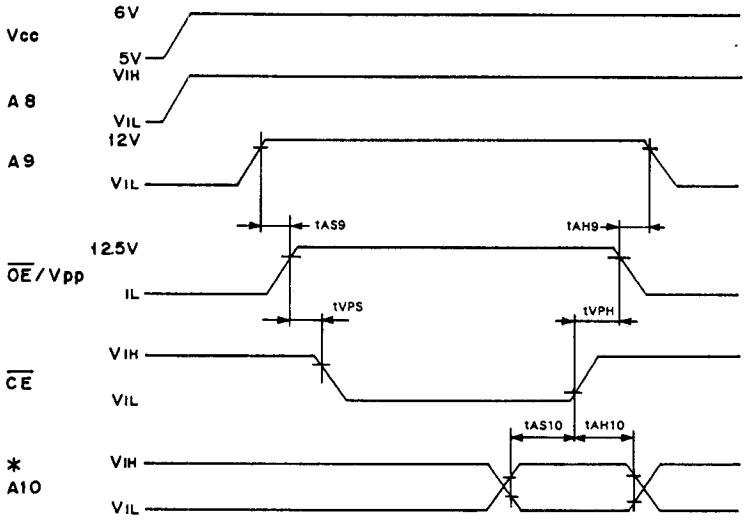
In this IC, erasure of data starts when exposed to light with a wavelength of 4000 Å or less. Considering that sunlight and some fluorescent lighting contain elements of a wavelength between 3000 and 4000 Å, long usage under such type of lighting conditions calls for protection. In such cases, use an opaque seal and the like to cover the glass window and prevent chip exposure to light.

Margin Mode

• AC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
A10 setup time	t_{AS10}	1			μs
A10 hold time	t_{AH10}	1			μs
Vpp hold time	t_{VPH}	2			μs
Vpp setup time	t_{VPS}	2			μs
A9 setup time	t_{AS9}	2			μs
A9 hold time	t_{AH9}	2			μs

Timing Waveform (Margin mode set • reset)



* Set margin mode A10 = V_{IH}, Reset margin mode A10 = V_{IL}.

Operation Modes

Read Mode

This IC features a chip enable ($\overline{CE}$) and an output enable ($\overline{OE}$/Vpp). $\overline{CE}$ selects the device and at the same time controls the power down function. $\overline{OE}$/Vpp controls the output buffer, independently from $\overline{CE}$. By setting the address while $\overline{CE} = \overline{OE}/Vpp = V_{IL}$, data becomes stable after t_{ACC}.

After address has become stable, respective data become stable when after t_{CE}, $\overline{CE}$ is lowered to V_{IL} from V_{IH} in $\overline{OE}/Vpp = V_{IL}$ condition, or $\overline{OE}/Vpp$ is lowered from V_{IH} to V_{IL} in $\overline{CE} = V_{IL}$ condition, after t_{OE}.

Output Disable Mode

By turning $\overline{OE}/Vpp$ to V_{IH}, the output pin turns to high impedance condition irrespectively of other inputs. This function completely prevents bus contention and allows for an easy connection of several devices on a common bus line.

Standby Mode

Turning $\overline{CE}$ to V_{IH} automatically brings in power down condition. Then current consumption Icc is reduced to a maximum 1mA. Also, output turns to high impedance condition irrespectively of $\overline{OE}/Vpp$.

Notes on Operation

Supply current Icc features 3 levels depending on the device operating condition. Standby current level, operating current level and transient peak current level. The transient peak current is the source of switching noise and the cause of high speed IC's misoperation. As the magnitude of the transient peak current heavily depends on the inductance and capacitance of the output load. This can be suppressed through the usage of a decoupling capacitor.

When the system is built, it is recommended to insert a high frequency 1 µF ceramic capacitor between Vcc and GND on every device, and as close to the device as possible.

In addition, a 4.7 µF electrolytic capacitor is recommended for every 8 devices. This should be close to the power supply to overcome voltage drop caused by the PCB wiring inductance.

Program Mode

When delivered, and after each erasure, all bits of the CXK27C512DQ are in the "1" state (Output "H" level). Data is introduced by selectively programming "0s" (output "L" level). To change a "0" to a "1" by ultraviolet light erasure is necessary. (See article on UV Erasure.)

The CXK27C512DQ is set to programming mode when 12.75V is applied to $\overline{OE}/Vpp$ pin and "L" level to $\overline{CE}$.

High Speed Programming Method

During programming and verify operation a circuit that automatically monitors the programming of cells is activated. Thus over program pulse so far in use is not necessary, and programming time is greatly reduced to 6 seconds.

Margin Mode

The CXK27C512DQ has margin mode circuit to guarantee sufficient programming margin. Thus over program pulse so far in use is not necessary. If setting this margin mode at programming, sufficient programming margin can be obtained within less than 6 seconds programming time.

Program Inhibit Mode

By turning $\overline{OE}$/Vpp to 12.75V and $\overline{CE}$ to V_{IH}, programming is inhibited. Using this method allows for programming of multiple devices in parallel with different data. With the exception of $\overline{CE}$ wiring is common. With the input of $\overline{CE} = V_{IL}$ pulse into the device selected for programming, this can be performed independently from other devices.

Program Verify

To verify if programming has been correctly performed at the specified address, memory cells are read out. Data of the selected address is output by turning to $\overline{CE} = \overline{OE}/Vpp = V_{IL}$.

Electronic Signature Mode

Electronic signature serves to identify the manufacturer and the device type of each EPROM. This function is intended for use by the programming equipment to automatically match the device to be programmed with its corresponding programming algorithm.

At read mode, 12V is applied to address A9.

A_1 to A_8, A_{10} to $A_{15} = \overline{OE}/Vpp = \overline{CE} = V_{IL}$ is obtained.

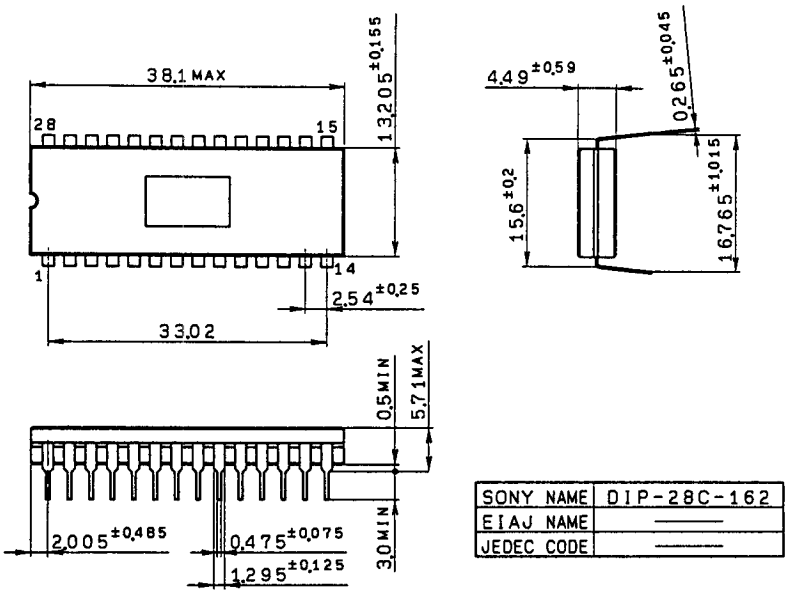
With $A_0 = V_{IL}$ the manufacturer code is output and with $A_0 = V_{IH}$ the device code is output.

The chart below shows the Electronic Signature.

Pins / Signature	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer Code	V_{IL}	0	0	1	0	0	0	0	0	20
Device Code	V_{IH}	0	0	1	1	1	1	0	1	3D

Package Outline Unit : mm

28 pin DIP (Ceramic)



SONY NAME	DIP-28C-162
EIAJ NAME	———
JEDEC CODE	———