

## Description

The μPD27C2001 is a 2,097,152-bit ultraviolet erasable EPROM fabricated with double-polysilicon CMOS technology for a substantial savings in both operating and standby power. The device is organized as 262,144 words by 8 bits and operates from a single +5-volt power supply.

The μPD27C2001 has a single-location programming feature, three-state outputs, and fully TTL-compatible inputs and outputs. It also has a program voltage ( $V_{PP}$ ) of 12.5 volts and is available in a 32-pin cerdip with quartz window.

## Features

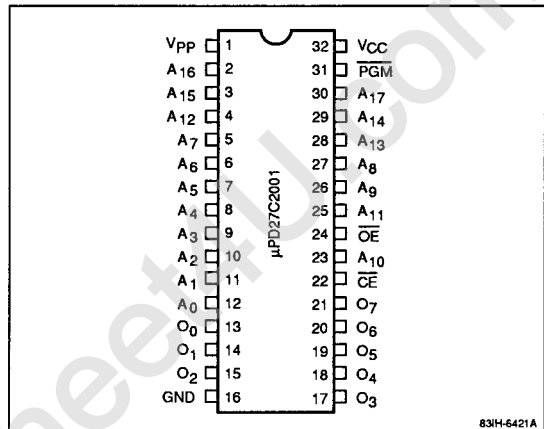
- 262,144 x 8-bit organization
- Ultraviolet erasable and electrically programmable
- High-speed page or byte programming
- Low power dissipation
  - 30 mA max (active)
  - 100 μA max (standby)
- TTL-compatible I/O for reading and programming
- Single +5-volt power supply
- Double-polysilicon CMOS technology
- 32-pin cerdip packaging with quartz window
- JEDEC-compatible pinout

## Ordering Information

Part Number	Access Time (max)	Package
μPD27C2001D-15	150 ns	32-pin cerdip with quartz window
D-17	170 ns	
D-20	200 ns	

## Pin Configuration

### 32-Pin Cerdip



## Pin Identification

Symbol	Function
A <sub>0</sub> - A <sub>17</sub>	Address inputs
O <sub>0</sub> - O <sub>7</sub>	Data outputs
CE	Chip enable
OE	Output enable
PGM	Program
GND	Ground
V <sub>CC</sub>	+5-volt power supply
V <sub>PP</sub>	Program voltage

### Absolute Maximum Ratings

Power supply voltage, $V_{CC}$	-0.6 to +7.0 V
Input voltage, $V_{IN}$	-0.6 to +7.0 V
Input voltage, $A_9$	-0.6 to +13.5 V
Output voltage, $V_{OUT}$	-0.6 to +7.0 V
Operating temperature, $T_{OPR}$	-10 to +80°C
Storage temperature, $T_{STG}$	-65 to +125°C
Program voltage, $V_{PP}$	-0.6 to +13.5 V

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

### Capacitance

$T_A = 25^\circ\text{C}$ ;  $f = 1\text{ MHz}$ ;  $V_{IN}$  and  $V_{OUT} = 0\text{ V}$

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	$C_{IN}$			14	pF
Output capacitance	$C_{OUT}$			16	pF

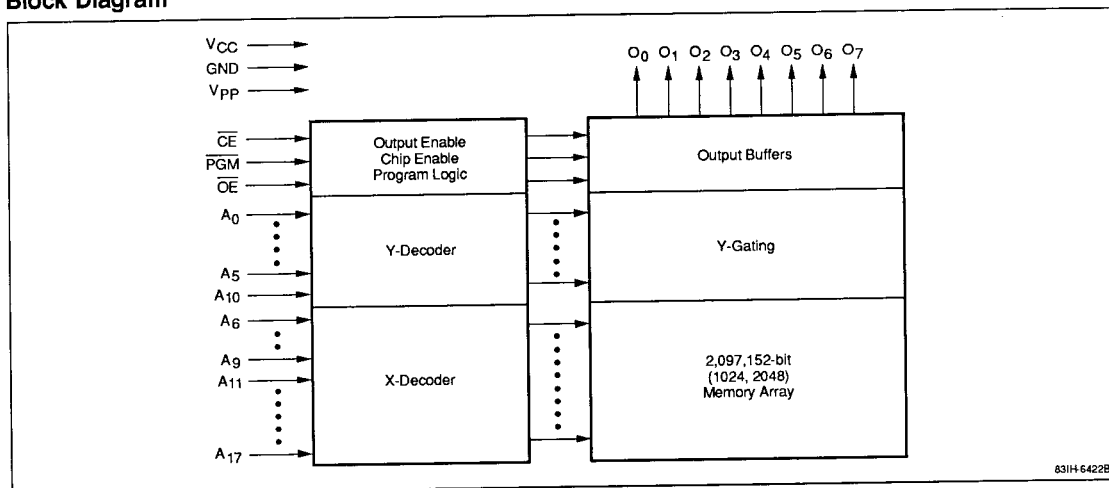
### Truth Table

Function	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	$V_{PP}$	$V_{CC}$	Outputs
Read	$V_{IL}$	$V_{IL}$	$V_{IH}$	5.0 V	5.0 V	$D_{OUT}$
Output disable	$V_{IL}$	$V_{IH}$	X	5.0 V	5.0 V	High-Z
Standby	$V_{IH}$	X	X	5.0 V	5.0 V	High-Z
Page data latch	$V_{IH}$	$V_{IL}$	$V_{IH}$	12.5 V	6.5 V	$D_{IN}$
Page program	$V_{IH}$	$V_{IH}$	$V_{IL}$	12.5 V	6.5 V	High-Z
Byte program	$V_{IL}$	$V_{IH}$	$V_{IL}$	12.5 V	6.5 V	$D_{IN}$
Program verify	$V_{IL}$	$V_{IL}$	$V_{IH}$	12.5 V	6.5 V	$D_{OUT}$
Program inhibit	X	$V_{IL}$	$V_{IL}$	12.5 V	6.5 V	High-Z
	X	$V_{IH}$	$V_{IH}$			

#### Notes:

- (1) X =  $V_{IL}$  or  $V_{IH}$ .
- (2) In read operation,  $\overline{PGM}$  must be set to  $V_{IH}$  at all times, or for at least 2  $\mu\text{s}$  before  $\overline{OE}$  or  $\overline{CE}$  returns to  $V_{IH}$ .

### Block Diagram



831H 6422B

## Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
<b>Read Operation or Standby</b>					
Supply voltage	$V_{CC}$	4.5	5.0	5.5	V
	$V_{PP}$	$V_{CC} - 0.6$	$V_{CC}$	$V_{CC} + 0.6$	V
Input voltage, high	$V_{IH}$	2.0		$V_{CC} + 0.3$	V
Input voltage, low	$V_{IL}$	-0.3		0.8	V
Operating temperature	$T_A$	0		70	°C
<b>Programming Operation</b>					
Supply voltage	$V_{CC}$	6.25	6.5	6.75	V
	$V_{PP}$	12.2	12.5	12.8	V
Input voltage, high	$V_{IH}$	2.4		$V_{CC} + 0.3$	V
Input voltage, low	$V_{IL}$	-0.3		0.8	V
Operating temperature	$T_A$	20	25	30	°C

## DC Characteristics

$T_A = 0$  to  $+70^\circ\text{C}$ ;  $V_{CC} = +5.0\text{ V} \pm 10\%$ ;  $V_{PP} = V_{CC} \pm 0.6\text{ V}$

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
<b>Read Operation</b>						
Output voltage, high	$V_{OH1}$	2.4			V	$I_{OH} = -400\ \mu\text{A}$
	$V_{OH2}$	$V_{CC} - 0.7$			V	$I_{OH} = -100\ \mu\text{A}$
Output voltage, low	$V_{OL}$		0.45		V	$I_{OL} = 2.1\ \text{mA}$
Output leakage current	$I_{LO}$		10		$\mu\text{A}$	$V_{OUT} = 0\text{ V to }V_{CC}$ ; $\overline{\text{OE}} = V_{IH}$
Input leakage current	$I_{LI}$		10		$\mu\text{A}$	$V_{IN} = 0\text{ V to }V_{CC}$
$V_{PP}$ current	$I_{PP}$	1	100		$\mu\text{A}$	$V_{PP} = V_{CC}$
$V_{CC}$ current (active)	$I_{CCA1}$		30		mA	$\overline{\text{CE}} = V_{IL}$ ; $V_{IN} = V_{IH}$
	$I_{CCA2}$		30		mA	$f = 6.7\ \text{MHz}$ ; $I_{OUT} = 0\ \text{mA}$
$V_{CC}$ current (standby)	$I_{CCS1}$		1		mA	$\overline{\text{CE}} = V_{IH}\ \text{min}$
	$I_{CCS2}$		1	100	$\mu\text{A}$	$\overline{\text{CE}} = V_{CC}$ ; $V_{IN} = 0\text{ V to }V_{CC}$

## DC Characteristics (cont)

$T_A = 25 \pm 5^\circ\text{C}$ ;  $V_{CC} = +6.5\text{ V} \pm 0.25$ ;  $V_{PP} = +12.5\text{ V} \pm 0.3$

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
<b>Programming Operation</b>						
Output voltage, high	$V_{OH}$	2.4			V	$I_{OH} = -400\ \mu\text{A}$
Output voltage, low	$V_{OL}$		0.45		V	$I_{OL} = 2.1\ \text{mA}$
Input leakage current	$I_{LI}$		10		$\mu\text{A}$	$V_{IN} = V_{IL}\ \text{or }V_{IH}$
$V_{PP}$ current	$I_{PP}$		50		mA	$\overline{\text{CE}} = \overline{\text{PGM}} = V_{IL}$
$V_{CC}$ current	$I_{CC}$		30		mA	

**AC Characteristics**

$T_A = 0 \text{ to } +70^\circ\text{C}; V_{CC} = +5.0 \text{ V} \pm 10\%; V_{PP} = V_{CC} \pm 0.6 \text{ V}$

Parameter	Symbol	μPD27C2001-15		μPD27C2001-17		μPD27C2001-20		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
<b>Read Operation</b>									
Address to output delay	$t_{ACC}$		150		170		200	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to output delay	$t_{CE}$		150		170		200	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ to output delay	$t_{OE}$		70		70		75	ns	$\overline{CE} = V_{IL}$
$\overline{OE}$ high to output float	$t_{DF}$	0	55	0	55	0	60	ns	$\overline{CE} = V_{IL} \text{ or } \overline{OE} = V_{IL}$
Address to output hold	$t_{OH}$	0		0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

**AC Characteristics (cont)**

$T_A = 25 \pm 5^\circ\text{C}; V_{CC} = +6.5 \text{ V} \pm 0.25; V_{PP} = +12.5 \text{ V} \pm 0.3$

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
<b>Page Programming Operation</b>						
Address setup time	$t_{AS}$	2			μs	
$\overline{CE}$ setup time	$t_{CES}$	2			μs	
Data setup time	$t_{DS}$	2			μs	
Address hold time	$t_{AH}$	2			μs	
	$t_{AHL}$	2			μs	
	$t_{AHV}$	0			μs	
Data hold time	$t_{DH}$	2			μs	
$\overline{OE}$ to output float time	$t_{DF}$	0		130	ns	
$V_{PP}$ setup time	$t_{VPS}$	2			μs	
$V_{CC}$ setup time	$t_{VCS}$	2			μs	
Program pulse width	$t_{PW}$	0.095	0.1	0.105	ms	
$\overline{OE}$ setup time	$t_{OES}$	2			μs	
$\overline{OE}$ to output delay	$t_{OE}$			150	ns	
$\overline{OE}$ pulse width during data latch	$t_{LW}$	1			μs	
PGM setup time	$t_{PGMS}$	2			μs	
$\overline{CE}$ hold time	$t_{CEH}$	2			μs	
OE hold time	$t_{OEH}$	2			μs	

### AC Characteristics (cont)

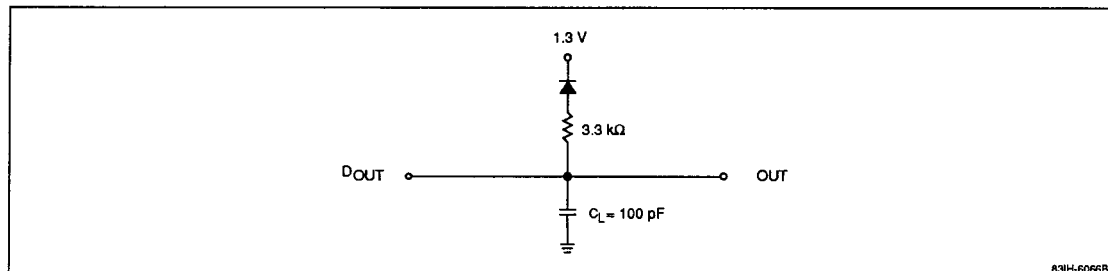
$T_A = 25 \pm 5^\circ\text{C}$ ;  $V_{CC} = +6.5 \text{ V} \pm 0.25$ ;  $V_{PP} = +12.5 \text{ V} \pm 0.3$

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
<b>Byte Programming Operation</b>						
Address setup time	$t_{AS}$	2			μs	
$\overline{OE}$ setup time	$t_{OES}$	2			μs	
Data setup time	$t_{DS}$	2			μs	
Address hold time	$t_{AH}$	2			μs	
Data hold time	$t_{DH}$	2			μs	
$\overline{OE}$ to output float time	$t_{DF}$	0		130	ns	
$V_{PP}$ setup time	$t_{VPS}$	2			μs	
$V_{CC}$ setup time	$t_{VCS}$	2			μs	
Program pulse width	$t_{PW}$	0.095	0.1	0.105	ms	
$\overline{CE}$ setup time	$t_{CES}$	2			μs	
$\overline{OE}$ to output delay	$t_{OE}$			150	ns	

#### Notes:

- (1) Input pulse levels = 0.45 to 2.4 V; input and output timing reference levels = 0.8 and 2.0 V; input rise and fall times  $\leq 20$  ns. See figure 1 for output load.

**Figure 1. Output Load**



83H-6066B

**PROGRAMMING**

Begin programming by erasing all data; this sets all bits high. The μPD27C2001 is originally shipped in this condition. To enter data, program a low-level TTL signal into the chosen location. Address the first byte or page location and apply valid data at the eight output pins. Raise  $V_{CC}$  to  $+6.5\text{ V} \pm 0.25$  and then  $V_{PP}$  to  $+12.5\text{ V} \pm 0.3$ .

**Byte Programming**

$\overline{CE}$  should be set low and  $\overline{OE}$  high to start programming at the initial byte address. Apply a 0.1-ms program pulse to  $\overline{PGM}$ , as shown in the byte programming portion of the timing waveforms. Set  $\overline{OE}$  low to verify the eight bits prior to making a program/no program decision. If the byte is not programmed, apply another 0.1-ms pulse to  $\overline{PGM}$ , up to a maximum of 10 times, and input the next address. If the bits are not programmed in 10 tries, reject the device as a program failure. After all addresses are programmed, lower both  $V_{CC}$  and  $V_{PP}$  to  $+5.0\text{ V} \pm 10\%$  and verify all data again.

**Page Programming**

For page programming,  $\overline{CE}$  and  $\overline{PGM}$  should be set high.  $\overline{OE}$  pulses low four times to latch the addressed four-byte, one-page data. Subsequently,  $\overline{CE}$  and  $\overline{OE}$  should be set high and a 0.1-ms program pulse applied to  $\overline{PGM}$ , as shown in the page programming portion of the timing waveforms. Verify the data prior to making a program/no program decision. If all four bytes of page data are not programmed, apply another 0.1-ms pulse to  $\overline{PGM}$ , up to a maximum of 10 times, and input the next page address. If the page is not programmed in 10 tries, reject the device as a program failure. After all addresses are programmed, lower both  $V_{CC}$  and  $V_{PP}$  to  $+5.0\text{ V} \pm 10\%$  and verify all data again.

**Program Inhibit**

Use the programming inhibit option to program multiple μPD27C2001s connected in parallel. All like inputs except  $\overline{PGM}$  and  $\overline{OE}$  may be common. Program individual devices by applying a low-level TTL pulse to the  $\overline{PGM}$  pin of the device to be programmed. Apply a high-level signal to the  $\overline{PGM}$  pins of the other devices to prevent them from being programmed.

**Program Verification**

To verify that the device is correctly programmed, normal read cycles can be executed with a high logic level applied to the  $\overline{PGM}$  pin and a low logic level applied to  $\overline{CE}$  and  $\overline{OE}$  of the device to be verified. The  $\overline{CE}$  or  $\overline{OE}$  pins of all other devices should be set high.

**Program Erasure**

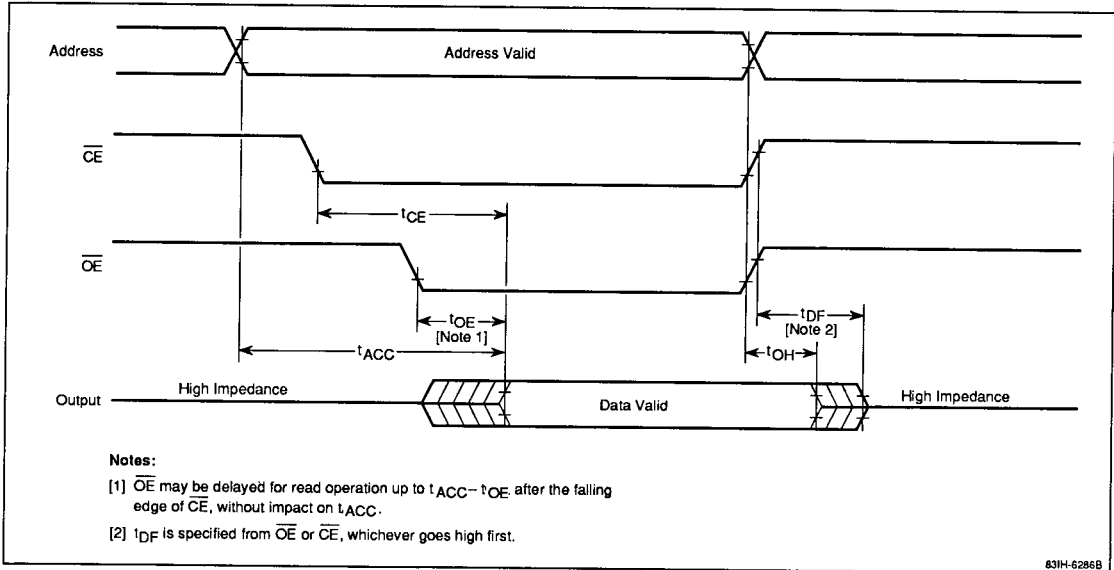
Erase data on the μPD27C2001 by exposing it to light with a wavelength shorter than 400 nm. Since exposure to direct sunlight or room-level fluorescent light could also erase the data, mask the window to prevent unintentional erasure by ultraviolet rays. Opaque labels are supplied with every device.

Data is typically erased by ultraviolet rays with a wavelength of 254 nm. A minimum integrated dose of 15 W-sec/cm<sup>2</sup> (ultraviolet lighting intensity multiplied by exposure time) is required to completely erase written data.

Using an ultraviolet lamp rated at 12,000 μW/cm<sup>2</sup>, it takes approximately 15 to 20 minutes to complete erasure. Place the μPD27C2001 within 2.5 cm of the lamp tubes and remove any filter on the lamp.

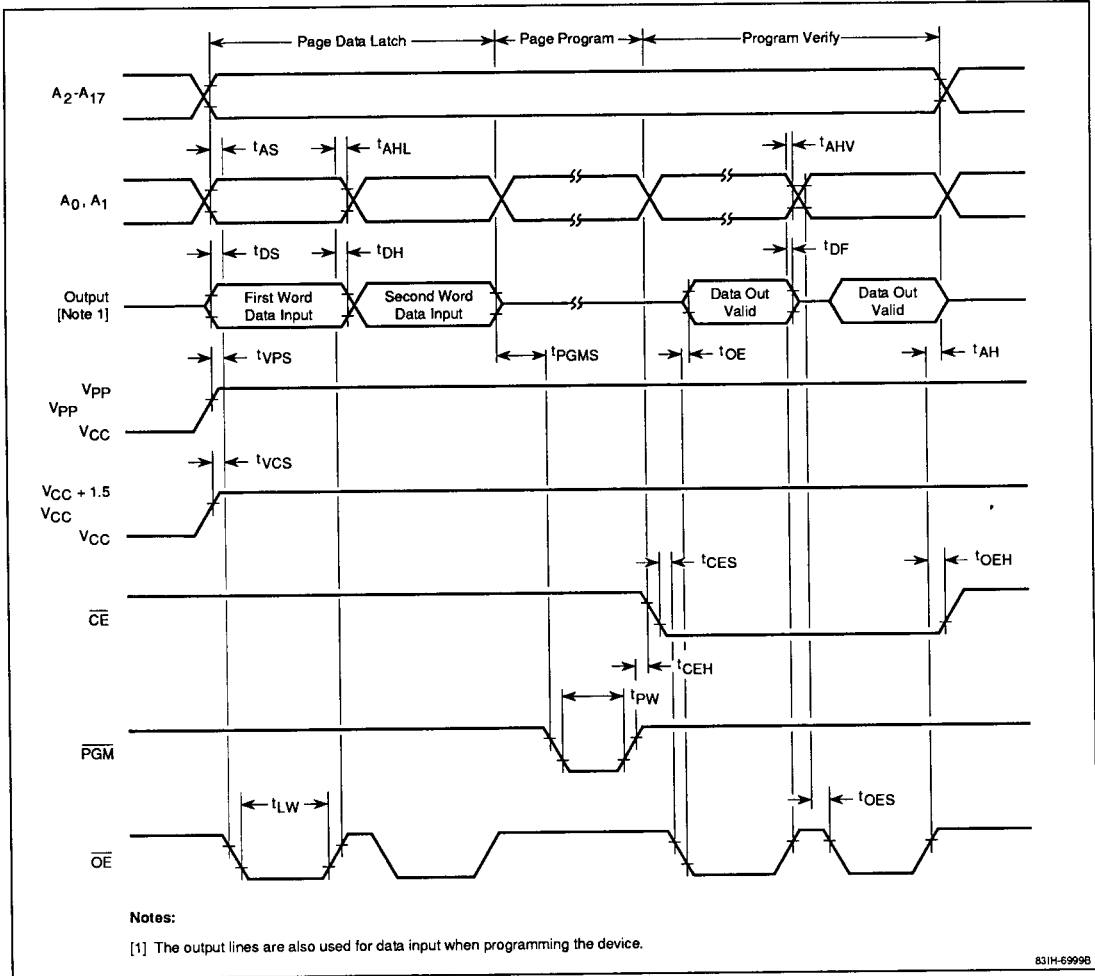
### Timing Waveforms

#### Read Cycle



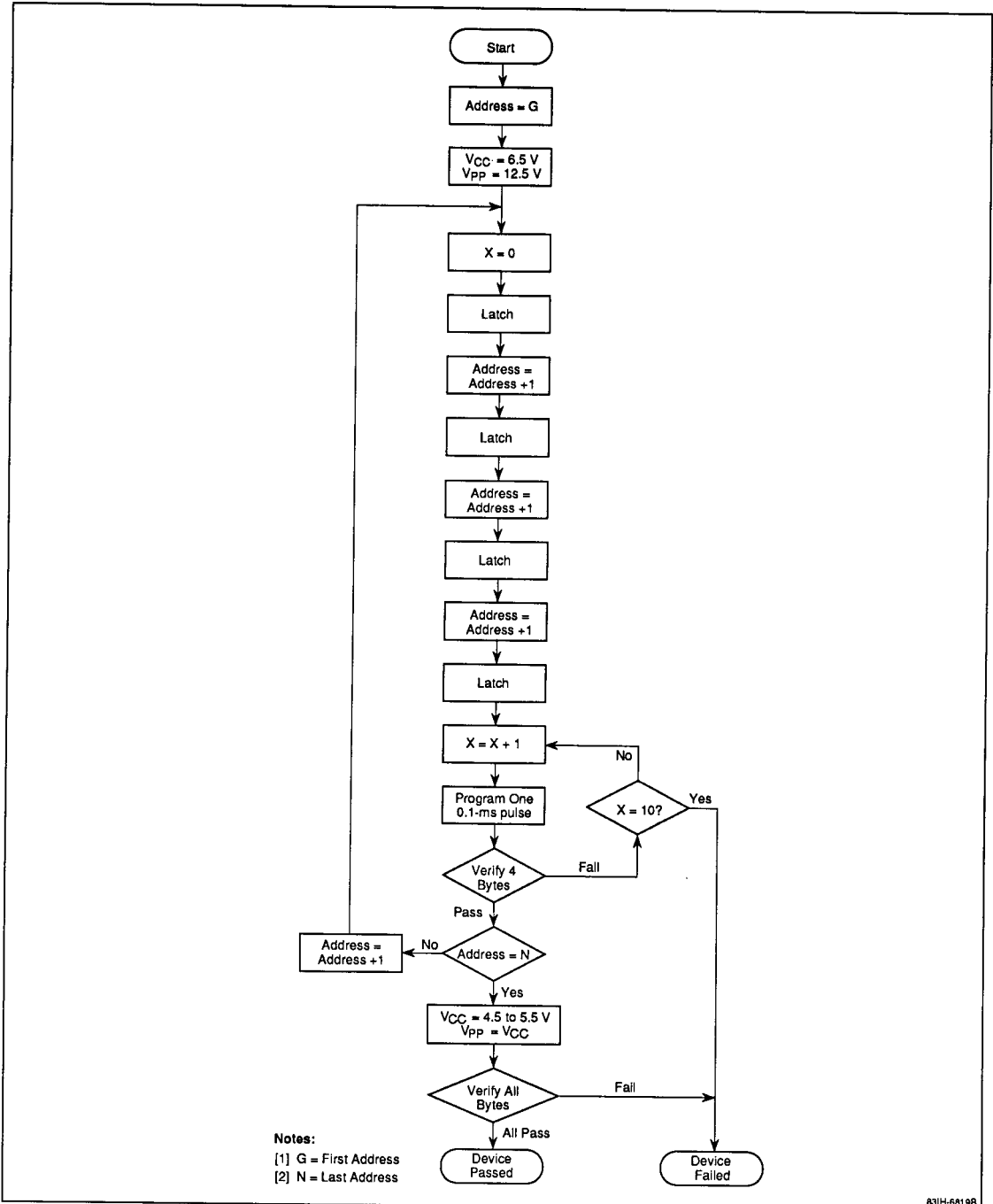
Timing Waveforms (cont)

Page Programming





**Figure 2. Page Programming Flowchart**



Timing Waveforms (cont)

Byte Programming Cycle

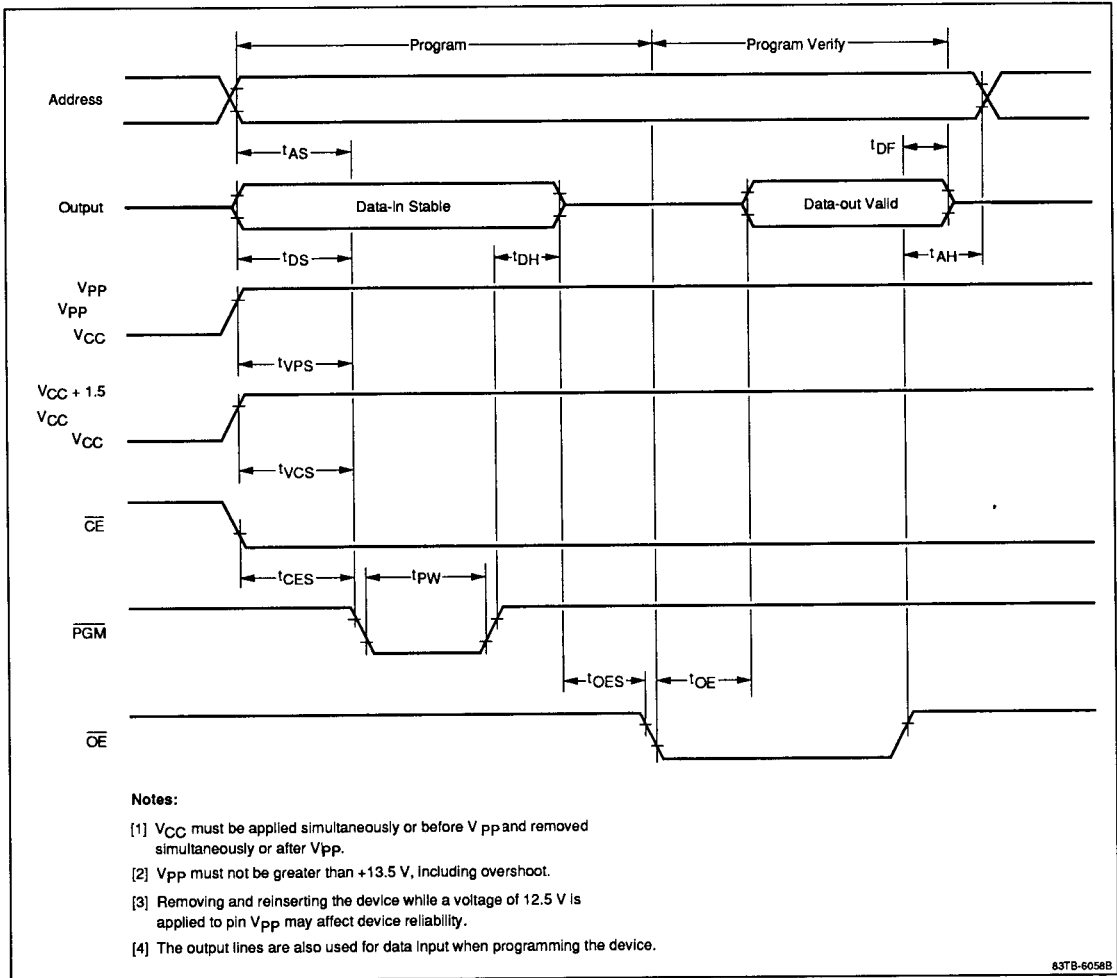


Figure 3. Byte Programming Flowchart

