Features

- Dynamic random access memory 65536 x 4 bits manufactured using a CMOS technology
- $\overline{RAS}$ access times 70 ns/80 ns
- TTL-compatible
- Three-state outputs bidirectional
- 256 refresh cycles 4 ms refresh cycle time
- FAST PAGE MODE
- Operating modes: Read, Write, Read - Write, $\overline{RAS}$ only Refresh, Hidden Refresh with address transfer
- Low power dissipation
- Power supply voltage 5 V
- Package PDIP18 (300 mil)
- Operating temperature range 0 to 70 °C
- Quality assessment according to CECC 90000, CECC 90100 and CECC 90112

Description

Addressing

The UD61464 is a dynamic random access memory organized 65536 words by 4 bits.

FPM facilitates faster data operation with predefined row address. Via 8 address inputs the 16 address bits are transmitted into the internal address memories in a time-multiplex operation. The falling $\overline{RAS}$-edge takes over the row address. After the row address hold time the column address can be applied. The bit pattern that is available at the address outputs during the set-up time and after the falling edge of $\overline{CAS}$ is interpreted as row address. During Write the column address is taken over with the falling edge of the control signal $\overline{CAS}$, or $\overline{W}$, whichever becomes active as the last. The selection of one or more memory circuits can be made via the $\overline{RAS}$ input.

Read-Write-Control

The choice between Read or Write cycle is made at the $\overline{W}$ input. HIGH at the $\overline{W}$ input causes a Read cycle, meanwhile LOW leads to a Write cycle.

Both $\overline{CAS}$-controlled and $\overline{W}$-controlled Write cycles are possible with activated $\overline{RAS}$ signal.

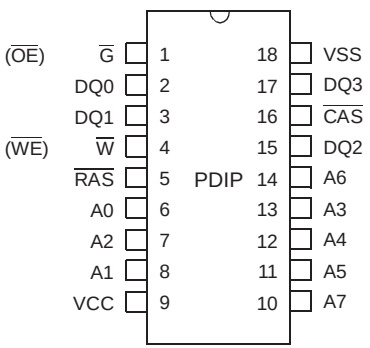
Data Output Control

The usual state of the data output is the High-Z state. Whenever $\overline{CAS}$ is inactive (HIGH), Q will float (High-Z). Thus, $\overline{CAS}$ functions as data output control.

After access time, in case of a Read cycle, the output is activated, and it contains the logic „0“ or „1“.

If the memory cycle is a Read, Read-Write or a Write cycle ($\overline{W}$-controlled), Q changes from High-Z state to the active state („0“ or „1“). After access time, the contents of the selected cell will be available, with the exception of the Write cycle. The output remains active until $\overline{CAS}$ becomes inactive, irrespective of $\overline{RAS}$ becoming inactive or not. The memory cycle being a Write cycle ($\overline{CAS}$-controlled), the data output keeps its High-Z state throughout the whole cycle. This configuration makes Q fully controllable by the user merely through the timing of $\overline{W}$. Through storaging the data on output, they remain valid from the end of access time until the start of another cycle.

Pin Configuration

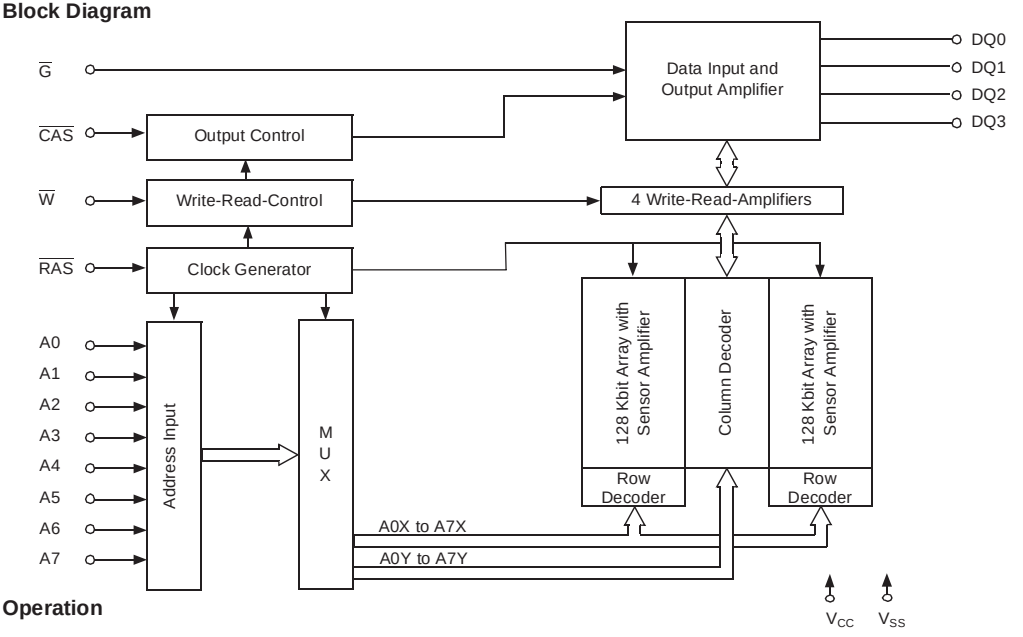


Top View

Pin Description

Signal Name	Signal Description
A0 - A7	Address Inputs
DQ0 - DQ3	Data In/Out
$\overline{W}$	Read, Write Control
$\overline{RAS}$	Row Address Strobe
$\overline{G}$	Output Enable
VCC	Power Supply Voltage
VSS	Ground
$\overline{CAS}$	Column Address Strobe

Block Diagram



Operation

Function		$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	Address		$\overline{G}$	Data
					R	C		
Stand-by		H	X	X	X	X	X	High-Z
Read		L	L	H	Row	Column	L	Output Data
Write		L	L	L	Row	Column	X	Input Data
Read-Write		L	L	H → L	Row	Column	L → H	Output Data/Input Data
FPM Read	1st cycle	L	H → L	H	Row	Column	L	Output Data
	2nd cycle	L	H → L	H		Column	L	Output Data
FPM Write	1st cycle	L	H → L	L	Row	Column	X	Input Data
	2nd cycle	L	H → L	L		Column	X	Input Data
FPM Read-Write	1st cycle	L	H → L	H → L	Row	Column	L → H	Output Data/Input Data
	2nd cycle	L	H → L	H → L		Column	L → H	Output Data/Input Data
$\overline{RAS}$ only Refresh		L	H	X	Row		X	High-Z
HIDDEN Refresh*)	Read	L → H → L	L	H	Row	Column	L	Output Data
	Write	L → H → L	L	L	Row	Column	X	Input Data

*) Transfer of Refresh Address required

Characteristics

All voltages are referenced to V_{SS} = 0 V (ground).
All characteristics are valid in the power supply voltage range and operating temperature range indicated below.

Absolute Maximum Ratings		Symbol	Min.	Max.	Unit
Power Supply Voltage		V_{CC}	-0.5	7.0	V
Input Voltage	1)	V_I	-1.0	7.0	V
Output Voltage	1)	V_O	-1.0	7.0	V
Output Current	1a)	I_O	-50	50	mA
Power Dissipation		P_D		1	W
Operating Temperature		T_a	0	70	°C
Storage Temperature		T_{stg}	-55	125	°C

Remarks: see page 7

Recommended Operating Conditions		Symbol	Min.	Max.	Unit
Power Supply Voltage		V_{CC}	4.5	5.5	V
Input Low Voltage	1)	V_{IL}	-1.0	0.8	V
Input High Voltage		V_{IH}	2.4	5.5	V

Remark: see page 7

Capacitances	Conditions	Symbol	Min.	Max.	Unit
Input Capacitance A0 to A7	V_{CC} = 5.0 V V_I = V_{SS} f = 1 MHz T_a = 25 °C	C_{I1}		6	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$ and $\overline{G}$		C_{I2}		7	pF
Output Capacitance DQ0 to DQ3		C_O		7	pF

All pins not under test must be connected with ground by capacitors.

Static Characteristics	Conditions	Symbol	Min.		Max.		Unit
			DC07	DC08	DC07	DC08	
Power Supply Current [2] (average value of $\overline{RAS}$-$\overline{CAS}$ cycles)	$t_{cW} = t_{cWmin}$ $t_{cR} = t_{cRmin}$	I_{CC1}			70	60	mA
Refresh Current [2] (average value of $\overline{RAS}$ cycles)	$\overline{CAS} = V_{IH}$ $t_{cW} = t_{cWmin}$ $t_{cR} = t_{cRmin}$	I_{CC2}			70	60	mA
FPM Current [2] (average value of FPM cycles)	$\overline{RAS} = V_{IL}$ $t_{cPG} = t_{cPGmin}$	I_{CC3}			50	40	mA
Stand-by Current (TTL Level)	$\overline{RAS} = \overline{CAS} = V_{IH}$	I_{CC4}			2	2	mA
Stand-by Current (CMOS Level)	$\overline{RAS} = V_{CC} - 0.2$ V $\overline{CAS} = V_{CC} - 0.2$ V	I_{CC5}			1	1	mA
Output High Voltage	$I_{OH} = -5$ mA	V_{OH}	2.4	2.4			V
Output Low Voltage	$I_{OL} = 4.2$ mA	V_{OL}			0.4	0.4	V
Input Leakage Current at any input, all other pins = 0 V	$V_I = 0$ V to 5.5 V	I_I	-10	-10	10	10	µA
Output Leakage Current Q = High-Z	$V_O = 0$ V to 5.5 V $\overline{RAS} = \overline{CAS} = V_{IH}$	I_O	-10	-10	10	10	µA

Remarks: see page 7

Dynamic Characteristics 3)	Symbol		Min.		Max.		Unit
	Alt.	IEC	DC07	DC08	DC07	DC08	
❒ ALL CYCLES							
Transition Time (Rise and Fall) 4)	t_T	t_t	3	3	50	50	ns
$\overline{RAS}$ Precharge Time	t_{RP}	$t_{w(RASH)}$	50	60			ns
$\overline{CAS}$ Precharge Time	t_{CP}	$t_{w(CASH)}$	10	10			ns
Row Address Set-up Time	t_{ASR}	$t_{su(RA-RAS)}$	0	0			ns
Column Address Set-up Time	t_{ASC}	$t_{su(CA-CAS)}$	0	0			ns
Row Address Hold Time	t_{RAH}	$t_{h(RAS-RA)}$	10	10			ns
Column Address Hold Time ref. to $\overline{RAS}$	t_{AR}	$t_{h(RAS-CA)}$	55	60			ns
Column Address Hold Time	t_{CAH}	$t_{h(CAS-CA)}$	15	15			ns
Output Buffer Turn-off Delay Time 5)	t_{OFF}	$t_{v(CAS)}$	0	0	20	20	ns
Output Buffer Turn-off Delay Time from $\overline{G}$ 5)	t_{OEZ}	$t_{v(G)}$	0	0	20	20	ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	$t_{CASH-RASL}$	5	5			ns
$\overline{RAS}$ to Column Address Delay Time 6)	t_{RAD}	t_{RAS-CA}	15	15	35	40	ns
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	$t_{CA-RASH}$	35	40			ns
$\overline{CAS}$ to Output in Low-Z	t_{CLZ}	$t_{CASL-QX}$	0	0			ns
Refresh Period	t_{REF}	t_{rf}			4	4	ms
❒ READ							
Random Read Cycle Time 7)	t_{RC}	t_{cR}	130	150			ns
Access Time from $\overline{RAS}$ 8)	t_{RAC}	$t_{a(RAS)}$			70	80	ns
Access Time from Column Address 8)	t_{AA}	$t_{a(CA)}$			35	40	ns
Access Time from $\overline{CAS}$ 8)	t_{CAC}	$t_{a(CAS)}$			20	20	ns
$\overline{G}$ Access Time 8)	t_{OEA}	$t_{a(G)}$			20	20	ns
$\overline{RAS}$ Pulse Width	t_{RAS}	$t_{w(RASL)}$	70	80	10000	10000	ns
$\overline{CAS}$ Pulse Width	t_{CAS}	$t_{w(CASL)}$	20	20	10000	10000	ns
Read Command Set-up Time	t_{RCS}	$t_{su(R-CAS)}$	0	0			ns
Read Command Hold Time ref. to $\overline{RAS}$ 9)	t_{RRH}	$t_{h(RAS-R)}$	0	0			ns
Read Command Hold Time 9)	t_{RCH}	$t_{h(CAS-R)}$	0	0			ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time 6)	t_{RCD}	$t_{RASL-CASL}$	20	20	50	60	ns
$\overline{CAS}$ Hold Time	t_{CSH}	$t_{RASL-CASH}$	70	80			ns
$\overline{RAS}$ Hold Time	t_{RSH}	$t_{CASL-RASH}$	20	20			ns
$\overline{RAS}$ Hold Time referenced to $\overline{G}$	t_{ROH}	$t_{GL-RASH}$	10	10			ns

Remarks: see page 7

Dynamic Characteristics	3)	Symbol		Min.		Max.		Unit
		Alt.	IEC	DC07	DC08	DC07	DC08	
❒ WRITE								
Random Write Cycle Time	7)	t_{RC}	t_{cW}	130	150			ns
$\overline{RAS}$ Pulse Width		t_{RAS}	$t_{w(RASL)}$	70	80	10000	10000	ns
$\overline{CAS}$ Pulse Width		t_{CAS}	$t_{w(CASL)}$	20	20	10000	10000	ns
Write Command Pulse Width		t_{WP}	$t_{w(W)}$	15	15			ns
Write Command Set-up Time	14)	t_{WCS}	$t_{su(W-CAS)}$	0	0			ns
Data Set-up Time ref. to $\overline{CAS}$	12)	t_{DS}	$t_{su(D-CAS)}$	0	0			ns
Data Set-up Time ref. to $\overline{W}$	12)	t_{DS}	$t_{su(D-W)}$	0	0			ns
Write Command Hold Time		t_{WCH}	$t_{h(CAS-W)}$	15	15			ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	$t_{h(W-RAS)}$	20	20			ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	$t_{h(W-CAS)}$	20	20			ns
Data Hold Time ref. to $\overline{CAS}$	12)	t_{DH}	$t_{h(CAS-D)}$	15	15			ns
Data Hold Time ref. to $\overline{W}$		t_{DH}	$t_{h(W-D)}$	15	15			ns
$\overline{G}$ Command Hold Time		t_{OEH}	$t_{h(W-GL)}$	20	20			ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	6)	t_{RCD}	$t_{RASL-CASL}$	20	20	50	60	ns
$\overline{CAS}$ Hold Time		t_{CSH}	$t_{RASL-CASH}$	70	80			ns
$\overline{RAS}$ Hold Time		t_{RSH}	$t_{CASL-RASH}$	20	20			ns
❒ READ-WRITE								
Read-Write Cycle Time	7)	t_{RWC}	t_{cRW}	185	205			ns
$\overline{RAS}$ Pulse Width		t_{RAS}	$t_{w(RASL)RW}$	125	135	10000	10000	ns
$\overline{CAS}$ Pulse Width		t_{CAS}	$t_{w(CASL)RW}$	75	75	10000	10000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	$t_{(RASL-CASH)RW}$	125	135			ns
$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	14)	t_{RWD}	t_{RAS-W}	100	110			ns
$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	14)	t_{CWD}	t_{CAS-W}	50	50			ns
Column to $\overline{WRITE}$ Delay Time	14)	t_{AWD}	$t_{(CA-W)RW}$	65	70			ns
❒ FPM Read								
Fast Page Mode Cycle Time		t_{PC}	t_{cPG}	50	50			ns
$\overline{RAS}$ Pulse Width		t_{RASP}	$t_{w(RASL)}$	70	80	100000	100000	ns
Access Time from $\overline{CAS}$ Precharge		t_{CPA}	$t_{a(CASH)}$	35	40			ns
❒ FPM Write								
Fast Page Mode Cycle Time		t_{PC}	t_{cPG}	50	50			ns

Remarks: see page 7

Dynamic Characteristics 3)	Symbol		Min.		Max.		Unit
	Alt.	IEC	DC07	DC08	DC07	DC08	
❒ FPM Read-Write							
FPM Cycle Time	t_{PC}	$t_{c(PG)RW}$	95	100			ns
Access Time from $\overline{CAS}$ Precharge	t_{CPA}	$t_{a(CASH)}$	35	40			ns
❒ HIDDEN REFRESH							
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	t_{CHR}	$t_{RASL-CASH}$	15	15			ns

Remark: see below

Remarks:

1) The Input Low Voltage must not drop below -0.3 V for more than 40 ns.

1a) The total sum of the absolute values of output currents must not exceed 100 mA in case of static application.

2) The current is inversely proportional to the cycle time; the max. current is measured in the shortest cycle time.

3) For test conditions see test configuration for functional test and clock timing.

4) V_{IHmin} and V_{ILmax} are reference levels for time measurement of the input signals; transition times are measured between V_{IH} and V_{IL}.

5) $t_{v(CAS)}$ and $t_{v(G)}$ define the time at which the data output goes to High-Z; this time is not related to any level.

6) $t_{RASL-CASLmax}$ and $t_{v(G)}$ are given as reference points only; they do not represent restrictive conditions.

7) The values of t_{cWmin}, t_{cRmin} and t_{cRWmin} are used for indication of the particular cycle time in which full function is guaranteed in the temperature range from 0 to 70 °C. Values below the one shown above may cause permanent damage to the component.

8) Measured with a load equivalent to 2 TTL loads, 100 pF.

9) In Read cycle either $t_{h(RAS-R)}$ or $t_{h(CAS-R)}$ must be kept.

10) $t_{h(RASH-CA)}$ is only required if the valid data are to be held beyond the rising edge of $\overline{RAS}$.

11) $t_{su(W-CAS)}$, t_{RAS-W}, t_{CAS-W} and $t_{(CA-W)RW}$ do not represent restrictive parameters:

- if $t_{su(W-CAS)} \geq t_{su(W-CAS)min}$ and $t_{h(CASH-W)} \geq t_{h(CASH-W)min}$, the cycle is a Write cycle ($\overline{CAS}$-controlled), and the data output remains in High-Z throughout the whole $\overline{CAS}$ cycle,

- if $t_{CAS-W} > t_{CAS-Wmin}$, $t_{RAS-W} > t_{RAS-Wmin}$ and $t_{(CA-W)RW} > t_{(CA-W)RWmin}$, the cycle is a Read-Write cycle, and the content of the cell is available at the data output,

- if none of these conditions is satisfied, the condition of the data output (at access time) is indeterminate, since a Write cycle ($\overline{W}$-controlled) is carried out.

12) These parameters refer to $\overline{CAS}$ during Write ($\overline{CAS}$-controlled), and to $\overline{W}$ ($\overline{W}$-controlled) or to $\overline{W}$ during Read-Write.

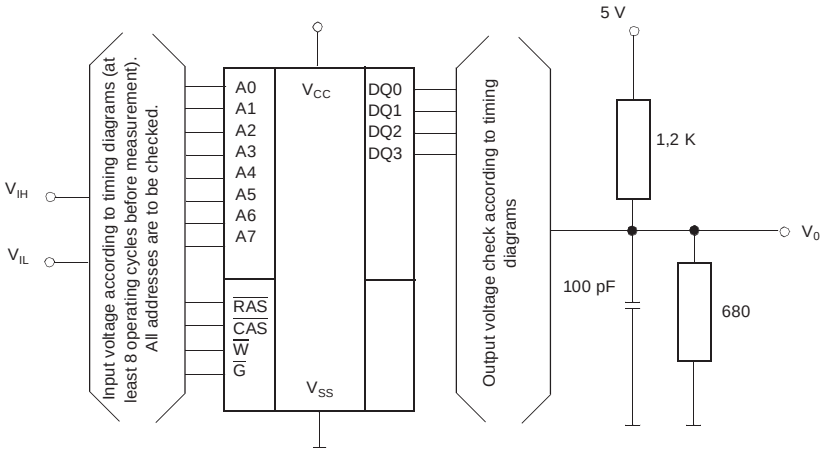
14) $t_{su(W-CAS)}$, t_{RAS-W}, t_{CAS-W} and $t_{(CA-W)RW}$ do not represent restrictive parameters:

- if $t_{su(W-CAS)} \geq t_{su(W-CAS)min}$ the cycle is a Write cycle ($\overline{CAS}$-controlled) and the data output remains in High-Z throughout the whole $\overline{CAS}$ cycle,

- if $t_{CAS-W} > t_{CAS-Wmin}$, $t_{RAS-W} > t_{RAS-Wmin}$ and $t_{(CA-W)RW} > t_{(CA-W)RWmin}$, the cycle is a Read-Write cycle, and the content of the cell is available at the data output,

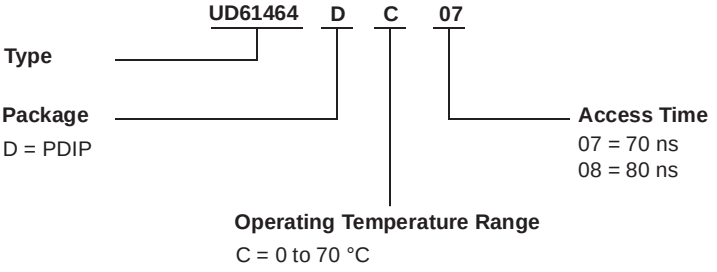
- if none of these conditions is satisfied, the condition of the data output (at access time) is indeterminate, since a Write cycle ($\overline{W}$-controlled) is carried out.

Test Configuration for Functional Check



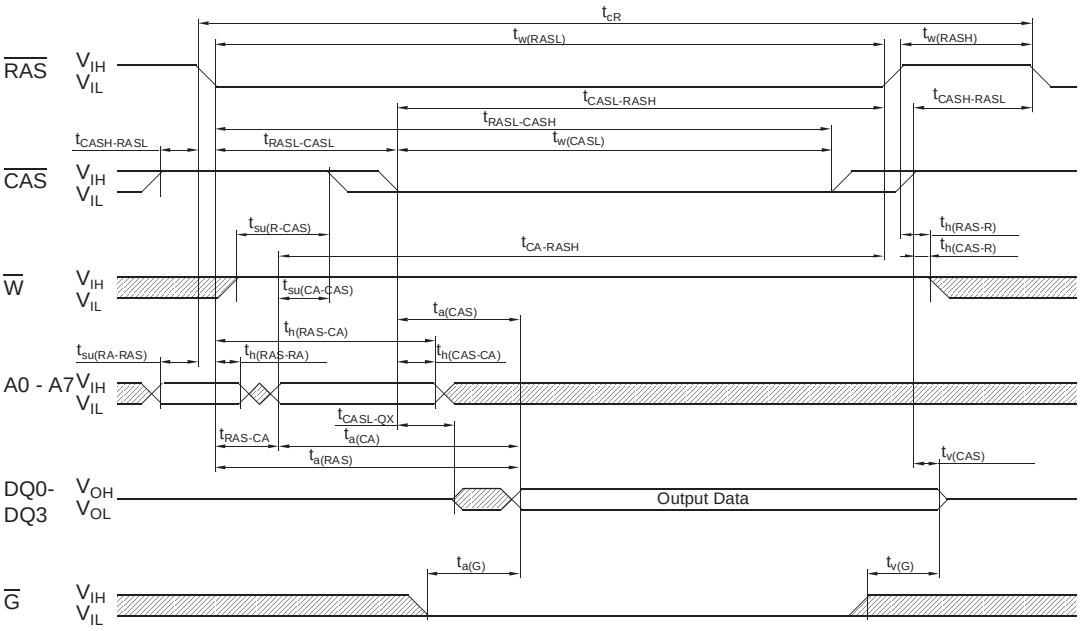
IC Code Numbers

Example

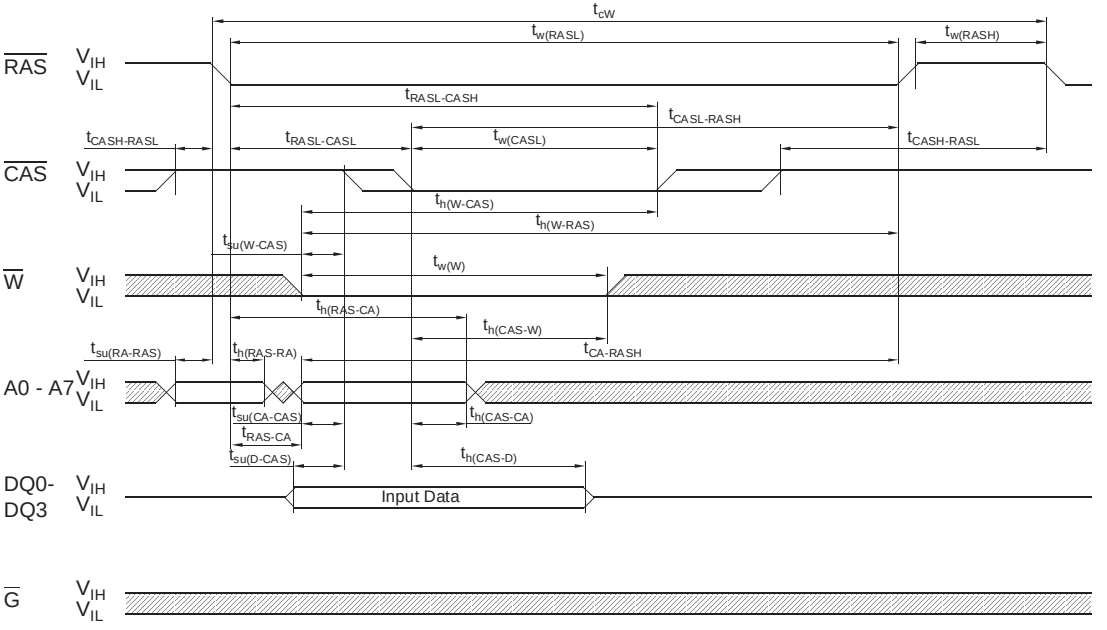


The date of manufacture is given by the 4 last digits of the mark, the 2 first digits indicating the year, and the last 2 digits the calendar week.

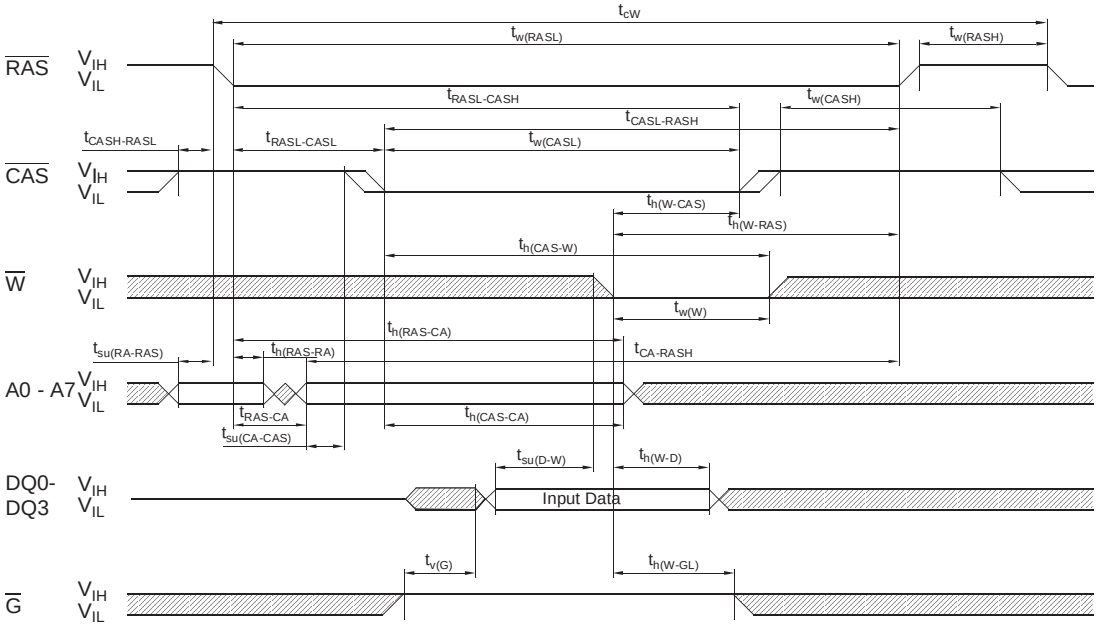
Read



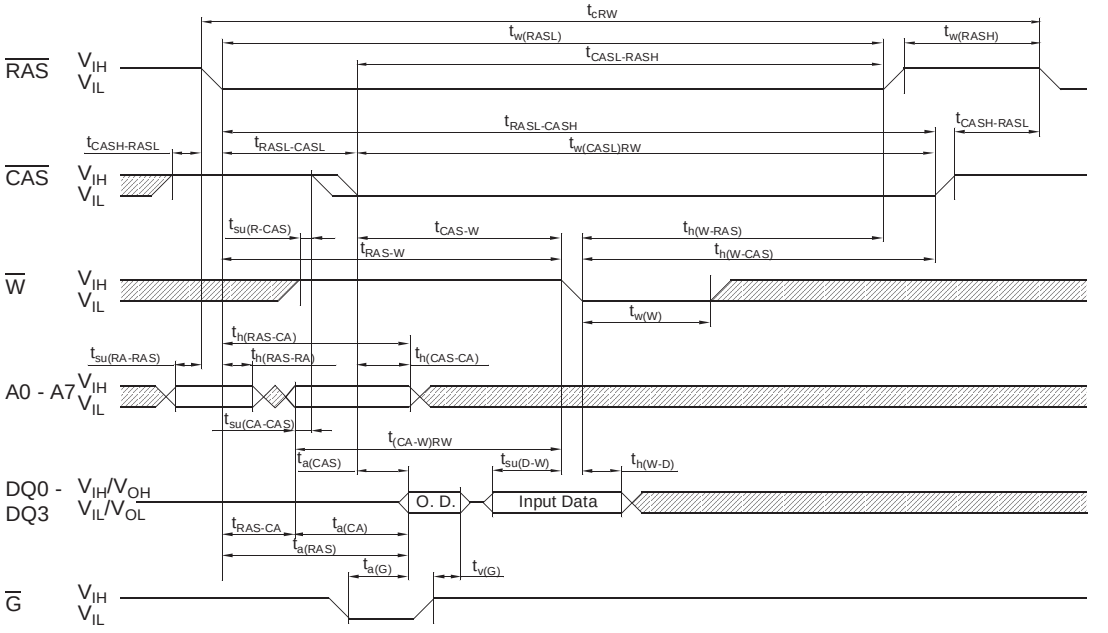
Write ($\overline{CAS}$-controlled)



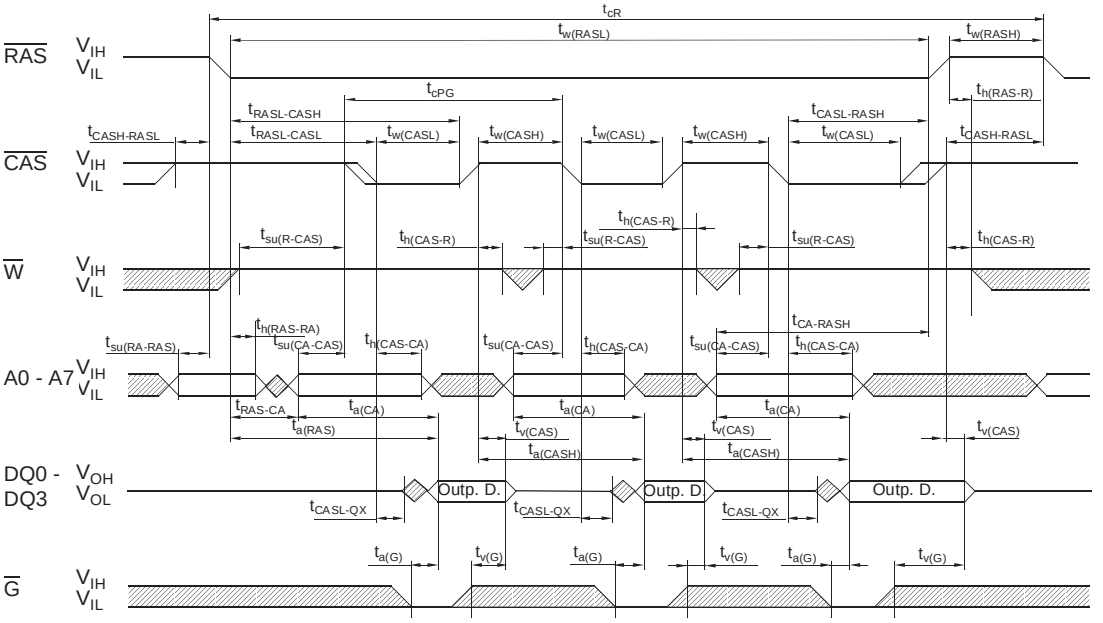
Write ($\overline{W}$-controlled)



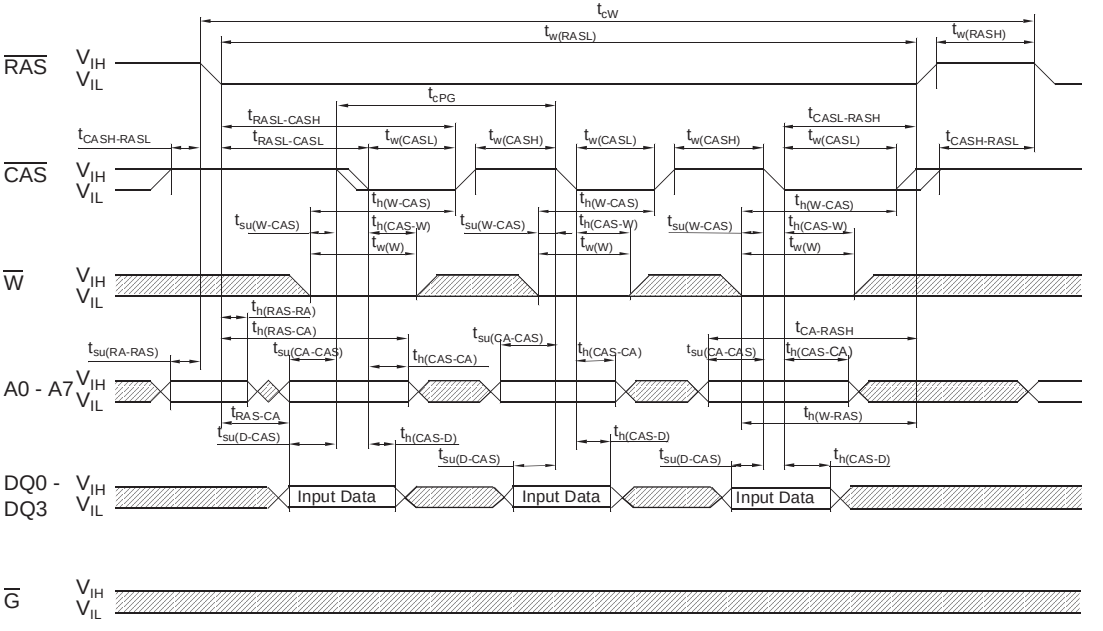
Read-Write



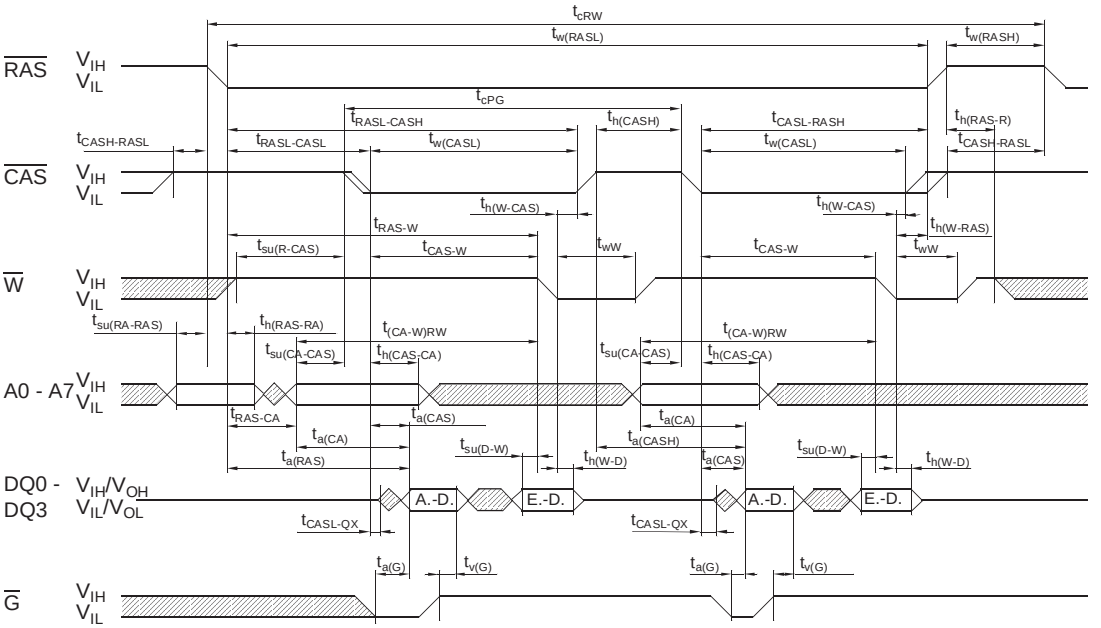
FPM Read



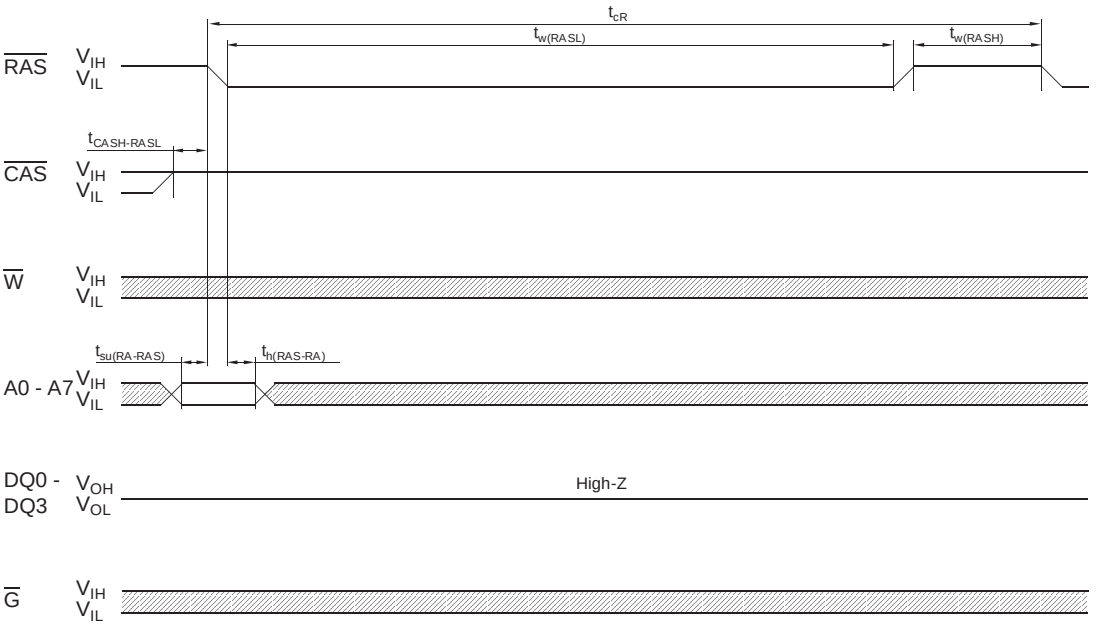
FPM Write (CAS-controlled)



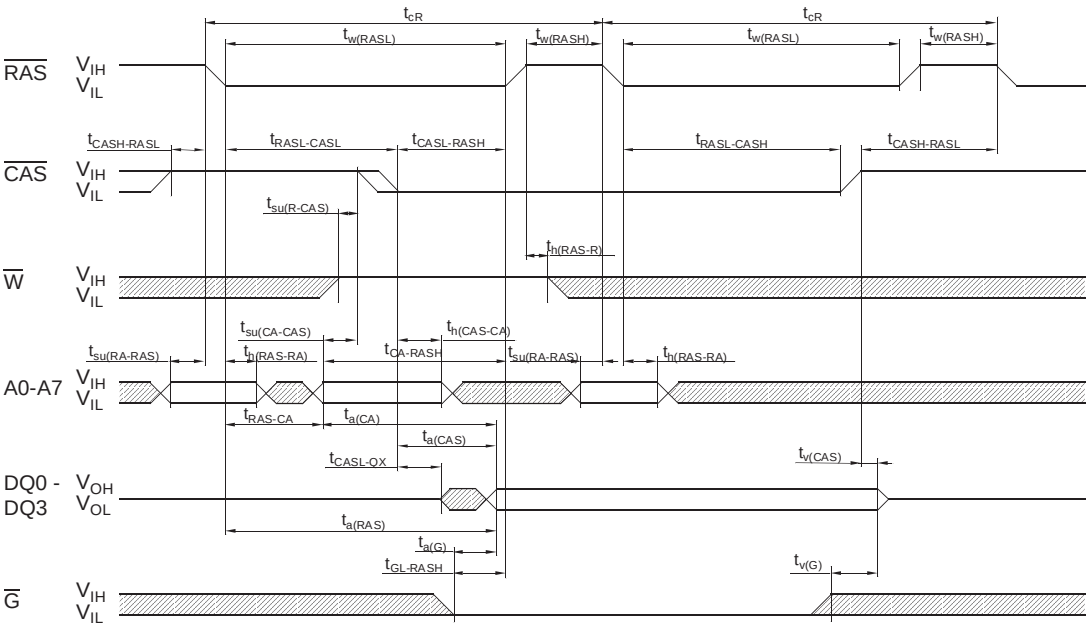
FPM Read-Write



$\overline{\text{RAS}}$ only Refresh



HIDDEN-Refresh with address transfer



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