MOS
LSI

TMS 4036 JL, NL; TMS 4036-1 JL, NL; TMS 4036-2 JL, NL
64-WORD BY 8-BIT STATIC RANDOM-ACCESS MEMORIES

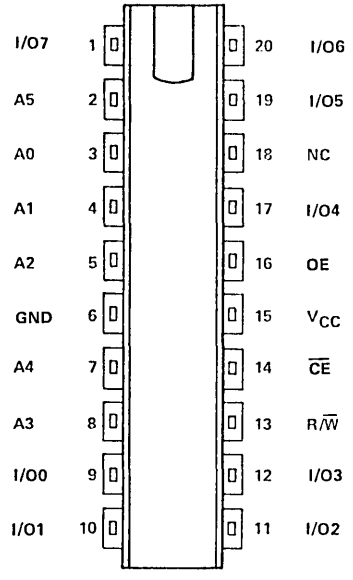
BULLETIN NO. DL-S 7512277, MAY 1975

- 64 x 8 Organization
- Static Operation (No Clocks, No Refresh)
- Compact 20-Pin 300-Mil Dual-in-Line Package
- 3 Performance Ranges:

	ACCESS TIME (MAX)	READ OR WRITE CYCLE (MIN)
TMS 4036	1000 ns	1000 ns
TMS 4036-1	650 ns	650 ns
TMS 4036-2	450 ns	450 ns

- Multiplexed Common Bus I/O
- Input Interface
  - Fully Decoded
  - TTL Compatible
  - Static Charge Protection
- Output Interface
  - 3-State
  - Fan-Out 1 Series 74 TTL Load
  - OR-Tie Capability
- Power Dissipation . . . 450 mW Maximum
- N-Channel Silicon-Gate Technology
- 8-Bit Word Length Ideal for Microprocessor-Based Systems

20-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



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description

This series of static random-access memories is organized as 64 words of 8 bits. Data inputs and outputs are multiplexed on an 8-bit, bidirectional bus controlled by the combination of chip enable and output enable. Static design results in reduced overhead costs by elimination of refresh-clocking circuitry and by simplification of the timing requirements. In addition, all inputs and outputs are fully compatible with Series 74 TTL, including the single 5-volt power supply. The TMS 4036 series is manufactured using TI's reliable N-channel silicon-gate technology to optimize the cost/performance relationship. Readout is nondestructive and the output data polarity is not inverted from data-in.

The TMS 4036 is offered in compact 20-pin ceramic (JL suffix) and plastic (NL suffix) dual-in-line packages designed for insertion in mounting-hole rows on 300-mil centers. The series is guaranteed for operation from 0°C to 70°C.

operation

addresses (A0-A5)

The 6-bit address selects one of 64 8-bit words. The address-valid time determines cycle time during both the read and write cycles. The address inputs can be driven directly from standard Series 54/74 TTL with no external pull-up resistors required.

PRELIMINARY DATA SHEET:
Supplementary data may be published at a later date.

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operation (continued)

chip enable ($\overline{CE}$)

The $\overline{CE}$ terminal is used to enable a specific memory device. If $\overline{CE}$ is low, the device is enabled for either a read or write cycle, depending on the state of the read/write and output-enable terminals. When $\overline{CE}$ is high, the I/O buffers are in the high-impedance state. $\overline{CE}$ may be driven from Series 74 TTL. For a more complete understanding of $\overline{CE}$, see the section on output enable.

read/write (R/$\overline{W}$)

The R/$\overline{W}$ input must be high during read and low during write operations. Prior to an address change, R/$\overline{W}$ must be in the read state and must remain in that state for a minimum period to eliminate the possibility of data being written into an unwanted position. The R/$\overline{W}$ input is TTL-compatible and does not require external resistors.

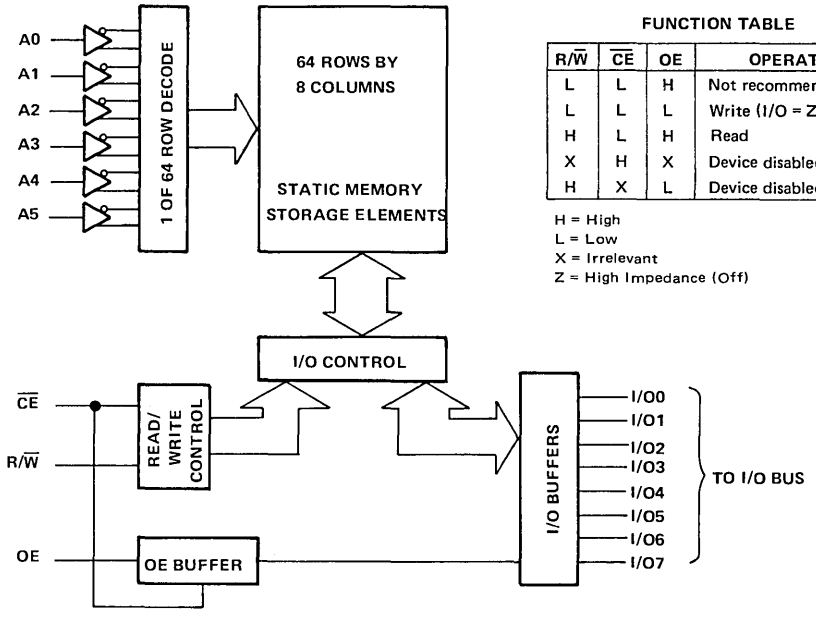
output enable (OE)

The output enable terminal controls the I/O buffer and determines whether the bus is in an input or output mode. When OE is low, the I/O terminals are in the input configuration; when OE is high, the I/O terminals are in the output configuration. The read cycle and write cycle timing diagrams show in detail the relation between $\overline{CE}$, OE, and the other signals (refer to the function table). This input is also compatible with Series 74 TTL circuits.

input/output buffer (I/O0-I/O7)

Each of these terminals interface directly with the external data bus and have the capability of being both an input and an output buffer. These buffers are controlled by a combination of $\overline{CE}$ and OE as described in the output enable section. Each buffer is three-state and fully TTL compatible, both as an input and an output.

functional block diagram



FUNCTION TABLE

R/$\overline{W}$	$\overline{CE}$	OE	OPERATION
L	L	H	Not recommended
L	L	L	Write (I/O = Z)
H	L	H	Read
X	H	X	Device disabled (I/O = Z)
H	X	L	Device disabled (I/O = Z)

H = High
L = Low
X = Irrelevant
Z = High Impedance (Off)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Notes 1 and 2)	−0.5 to 7 V
Input voltage (any input) (see Notes 1 and 2)	−0.5 to 7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTES:
1. Voltage values are with respect to the ground terminal.
2. For all combinations of inputs, the I/O lines may be shorted to V_{SS} or V_{CC} for a period not to exceed five milliseconds.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER	TMS 4036			TMS 4036-1			TMS 4036-2			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	V
Supply voltage, V_{SS}		0			0			0		V
High-level input voltage, V_{IH}	2.2		V_{CC}	2.2		V_{CC}	2.2		V_{CC}	V
Low-level input voltage, V_{IL} (see Note 3)	−0.3		0.8	−0.3		0.8	−0.3		0.8	V
Read cycle time, $t_{c(rd)}$	1000			650			450			ns
Write cycle time, $t_{c(wr)}$	1000			650			450			ns
Write pulse width, $t_{w(wr)}$	500			300			200			ns
Address setup time, $t_{su(ad)}$	450			300			200			ns
Chip-enable setup time, $t_{su(\overline{CE})}$	700			500			400			ns
Data setup time, $t_{su(da)}$	600			400			300			ns
Address hold time, $t_{h(ad)}$	50			50			50			ns
Data hold time, $t_{h(da)}$	50			50			50			ns
Operating free-air temperature, T_A	0		70	0		70	0		70	°C

NOTE 3: The albegraic convention where the most negative limit is designated as minimum is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

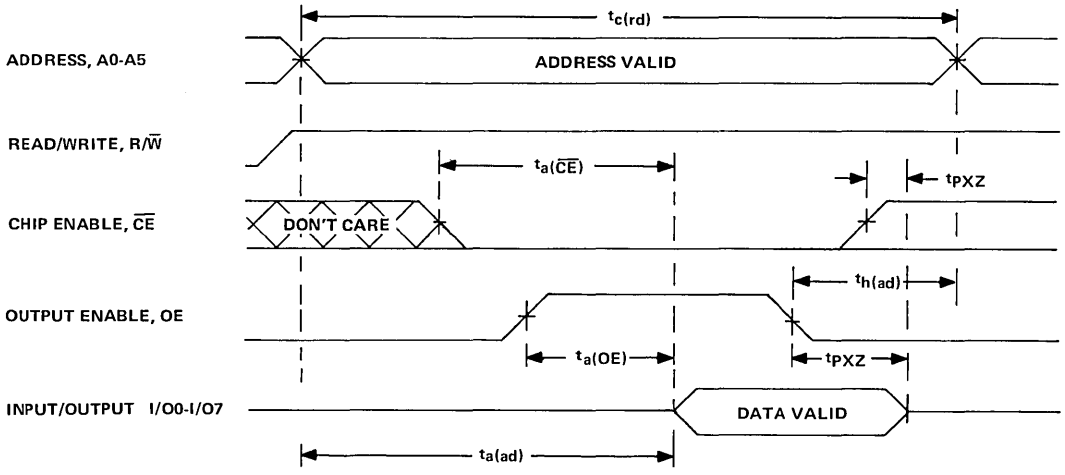
PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −100 μA,	V_{CC} = 4.75 V	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 1.9 mA,	V_{CC} = 4.75 V		0.4	V
I_{IH}	High-level input current into address, R/$\overline{W}$, $\overline{CE}$, or OE	V_I = 5.25 V			10	μA
I_{OZH}	Off-state output current, high-level voltage applied at I/O terminal	V_O = 5.25 V, $\overline{CE}$ at 5.25 V	OE at 0 V,		10	μA
		V_O = 5.25 V, $\overline{CE}$ at 2.2 V	OE at 5.25 V,		10	
		V_O = 5.25 V, $\overline{CE}$ at 0 V	OE at 0.8 V,		10	
I_{OZL}	Off-state output current, low-level voltage applied at I/O terminal	V_O = 0 V, $\overline{CE}$ at 2.2 V	OE at 5.25 V,		−100	μA
		V_O = 0 V, $\overline{CE}$ at 0 V	OE at 0.8 V,		−100	
I_{CC}	Supply current from V_{CC}				85	mA
C_i	Input capacitance	f = 1 MHz,	T_A = 25°C		10	pF
$C_{i/o}$	I/O terminal capacitance	f = 1 MHz,	T_A = 25°C		20	pF

switching characteristics over recommended supply voltage ranges, T_A = 0°C to 70°C

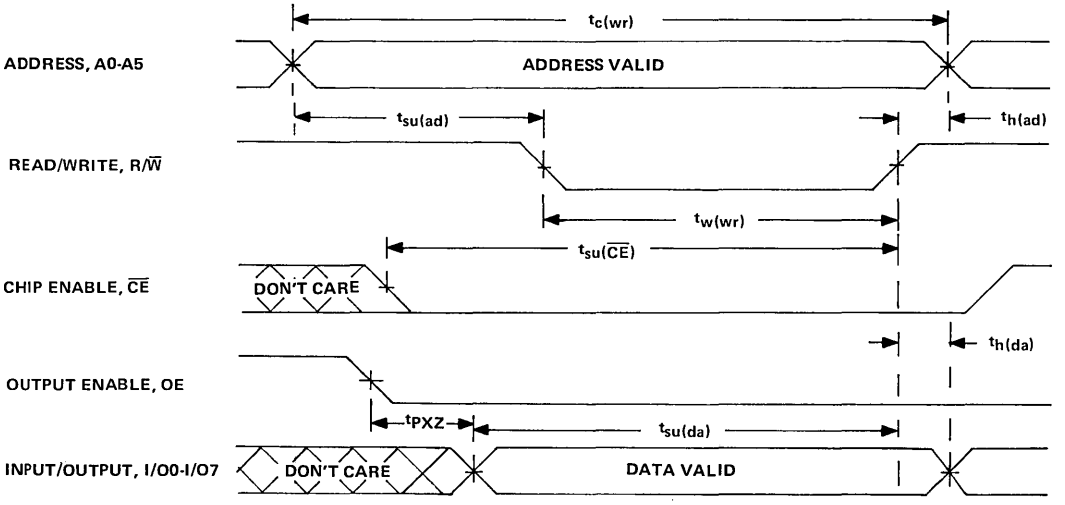
PARAMETER		TMS 4036			TMS 4036-1			TMS 4036-2			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{a(ad)}$	Access time from address			1000			650			450	ns
$t_{a(\overline{CE})}$	Access time from chip enable			200			190			180	ns
$t_{a(OE)}$	Access time from output enable			200			190			180	ns
t_{PXZ}	Output disable time from chip enable	0	60	200	0	60	200	0	60	200	ns
t_{PXZ}	Output disable time from output enable (see Note 4)	0	60	200	0	60	200	0	60	200	ns

NOTE 4: This parameter defines the delay for the I/O bus to enter the input mode.
†All typical values are at T_A = 25°C.

read cycle timing



write cycle timing



NOTE: For measuring timing requirements and characteristics, V_{IH} = 2.2 V, V_{IL} = 0.65 V, $t_r = t_f$ = 20 ns and all timing points are 50% points.