2108-2 AND 2108-4
8192 X 1 BIT DYNAMIC RAM

	2108-2	2108-4
	S1572,S1573	S1626,S1627
Max. Access Time (ns)	200	300
Read, Write Cycle (ns)	350	425
Read-Modify-Write Cycle (ns)	400	595

- **8K RAM in Industry Standard 16 Pin Package**
- **Low Standby Power**
- **All Inputs Including Clocks TTL Compatible**
- **Standard Power Supplies +12V, +5V, -5V**
- **Only 64 Refresh Cycles Required Every 2 ms**
- **On-Chip Input Latches**
- **Output is Three-State, TTL Compatible; Data is Latched and Valid into Next Cycle**
- **Fully Compatible with 4K and 16K Dynamic RAMs**

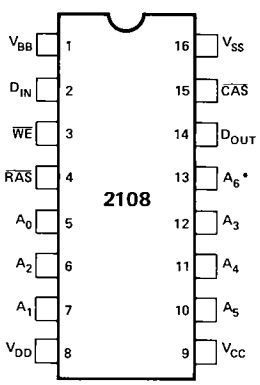
The Intel®2108 is a 8K Dynamic MOS RAM organized as 8192 words by 1 bit. The 2108 employs the same masks and highly reliable, production-proven two layer polysilicon N-MOS technology as the Intel® 2116 16K RAM. As shown in the block diagram below, the 2116 is organized as two 8K RAMs on a single silicon die. Each of these 8K RAMs contains its own row decoders, sense amplifiers, and storage cells. The 2108 is fully tested to insure that one 8K RAM meets all AC and DC specifications.

The 2108 is available as either the upper or lower half of the 2116. Address A_6 selects the operating half. For S1572 or S1627, A_6 should be high (V_{IH}) during row address strobe (RAS). For S1573 or S1626, A_6 should be low (V_{IL}) during RAS. The use of the Intel® 3242 Address Multiplexer/Refresh Counter with a 2108 is described on page 2-66. The 2108 is packaged in the industry standard 16-pin DIP which is compatible with widely available automated handling equipment and facilitates easy upgrading from 2104A-type 4K RAM Systems and up to 2116-type 16K RAM Systems.

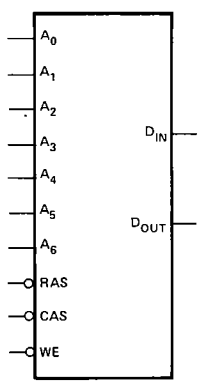
As in the 2104A-type 4K RAM and 2116-type 16K RAM, the 2108 has non-critical clock timing requirements which allow use of addressing multiplexing while maintaining high performance. Three methods of refreshing are permissable; they are described in the applications section of this data sheet.

The 2108 will provide the same reliable operation in its system usage as any Intel product. Information on the details of reliability tests performed on the 2108 and field data on the use of partial devices are available from Intel Corporation.

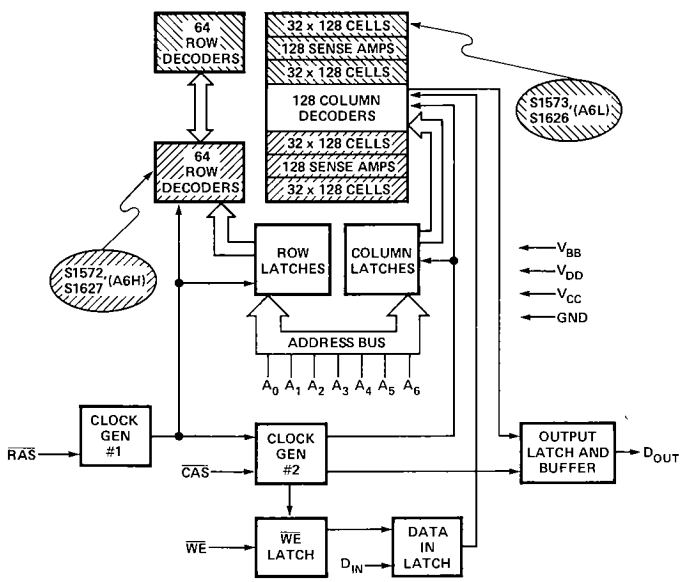
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_6	ADDRESS INPUTS	$\overline{WE}$	WRITE ENABLE
$\overline{CAS}$	COLUMN ADDRESS STROBE	V_{BB}	POWER (-5V)
D_{IN}	DATA IN	V_{CC}	POWER (+5V)
D_{OUT}	DATA OUT	V_{DD}	POWER (+12V)
$\overline{RAS}$	ROW ADDRESS STROBE	V_{SS}	GROUND

*S1572 & S1627: A_6 SHOULD BE AT V_{IH} DURING $\overline{RAS}$
S1573 & S1626: A_6 SHOULD BE AT V_{IL} DURING $\overline{RAS}$

Absolute Maximum Ratings*

Ambient Temperature Under Bias	-10°C to +80°C
Storage Temperature	-65°C to +150°C
Voltage on any Pin Relative to V_{BB} (V_{SS} - V_{BB} ≥ 4V)	-0.3V to +20V
Power Dissipation	1.25W

*COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics [1],[2]

T_A = 0°C to 70°C, V_{DD} = +12V ±10%, V_{CC} = +5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Limits			Unit	Conditions	
		Min.	Typ.[3]	Max.			
I_{LI}	Input Load Current (any input)			.10	µA	V_{IN} = $V_{IL\ MIN}$ to $V_{IH\ MAX}$	
$\|I_{LO}\|$	Output Leakage Current for high impedance state		0.1	10	µA	Chip deselected: $\overline{RAS}$ and $\overline{CAS}$ at V_{IH} V_{OUT} = 0 to 5.5V	
I_{DD1}	V_{DD} Supply Current		1.2	2	mA	$\overline{CAS}$ and $\overline{RAS}$ at V_{IH} or $\overline{CAS}$-only cycle. Chip deselected prior to measurement. See Note 5.	
I_{BB1}	V_{BB} Supply Current		1	50	µA		
I_{DD2}[4]	Operating V_{DD} Current		53	69	mA	2108-2 t_{CYC} = 350 ns	T_A = 25°C Device selected. See Note 6.
			49	65	mA	2108-4 t_{CYC} = 425 ns	
I_{BB2}	Operating V_{BB} Current		120	400	µA	Device selected	
I_{CC1}[7]	V_{CC} Supply Current when deselected			10	µA		
V_{IL}	Input Low Voltage (any input)	-1.0		0.8	V		
V_{IH}	Input High Voltage (any input)	2.4		V_{CC}+1	V		
V_{OL}	Output Low Voltage	0.0		0.4	V	I_{OL} = 4.1 mA (Read Cycle Only)	
V_{OH}	Output High Voltage	2.4		V_{CC}	V	I_{OH} = -5 mA (Read Cycle Only)	

Capacitance [8]

T_A = 25°C, V_{DD} = 12V ±10%, V_{CC} = 5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{I1}	Address, Data In & $\overline{WE}$ Capacitance	4	7	pF	V_{IN} = V_{SS}
C_{I2}	$\overline{RAS}$ Capacitance	3	5	pF	V_{IN} = V_{SS}
C_{I3}	$\overline{CAS}$ Capacitance	6	10	pF	V_{IN} = V_{SS}
C_O	Data Output Capacitance	3	7	pF	V_{OUT} = 0V

Notes:
1. All voltages referenced to V_{SS}. No power supply sequencing is required but V_{DD}, V_{CC}, and V_{SS} should never be 0.3V or more negative than V_{BB}.
2. To avoid self-clocking, $\overline{RAS}$ should not be allowed to float.
3. Typical values are for T_A = 25°C and nominal power supply voltages.
4. For $\overline{RAS}$-only refresh I_{DD} = 0.78 I_{DD2}. For $\overline{CAS}$-before-$\overline{RAS}$ (64 cycle refresh) I_{DD} = 0.96 I_{DD2}.
5. The chip is deselected (i.e., output is brought to high impedance state) by $\overline{CAS}$-only cycle or by $\overline{CAS}$-before-$\overline{RAS}$ cycle. The current flowing in a selected (i.e., output on) chip with $\overline{RAS}$ and $\overline{CAS}$ at V_{IH} is approximately twice I_{DD1}.
6. See Page 2-62 for typical I_{DD} characteristics under other conditions.
7. When chip is selected V_{CC} supply current is dependent on output loading; V_{CC} is connected to output buffer only.
8. Capacitance measured with Boonton Meter.

TYPICAL CHARACTERISTICS

I_{BB2} AND I_{DD2} VS. TEMPERATURE

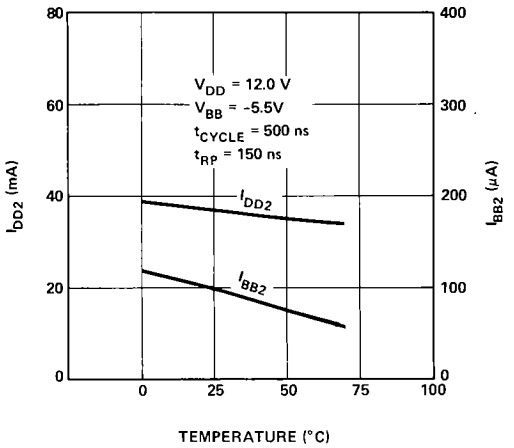


Figure 1.

I_{DD2} VS. CYCLE TIME

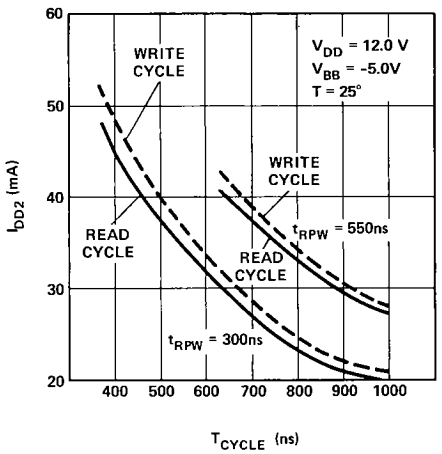


Figure 2.

Standby Power Calculations:

$$P_{REF} = P_{OP}\left(N\frac{t_{CYC}}{t_{REF}}\right) + P_{SB}\left(1 - N\frac{t_{CYC}}{t_{REF}}\right)$$ where

P_{OP} = Power dissipation — continuous operation = V_{DD} x I_{DD2}.

N = Number of refresh cycles (64).

t_{CYC} = Cycle time for a refresh cycle.

t_{REF} = Time between refreshes

P_{SB} = Standby power dissipation = V_{DD} x I_{DD1} + $|V_{BB}|$ x I_{BB}

Note that I_{DD2} depends upon refresh as follows:

1. For ($\overline{RAS}$ before $\overline{CAS}$) use I_{DD2} from Figures 1 and 2.
2. For ($\overline{CAS}$ before $\overline{RAS}$) multiply I_{DD2} determined in (1) by 0.96.
3. For ($\overline{RAS}$ only) multiply I_{DD2} determined in (1) by 0.78.

Examples of typical calculations for V_{BB} = -5.0V, V_{DD} = 12.0V, T_A = 25°C, t_{CYC} = 0.425 μs, t_{RAS} = 0.3 μs. t_{REF} = 2000 μs:

1. 128 cycle ($\overline{RAS}$ before $\overline{CAS}$): P_{OP} = 12.0V x 43 mA = 516 mW

   $$P_{REF} = 516\left(128\ \frac{0.425}{2000}\right) + (12x1.2+5x0.001)\left(1-128\ \frac{0.425}{2000}\right)$$

   P_{REF} = 28.0 mW

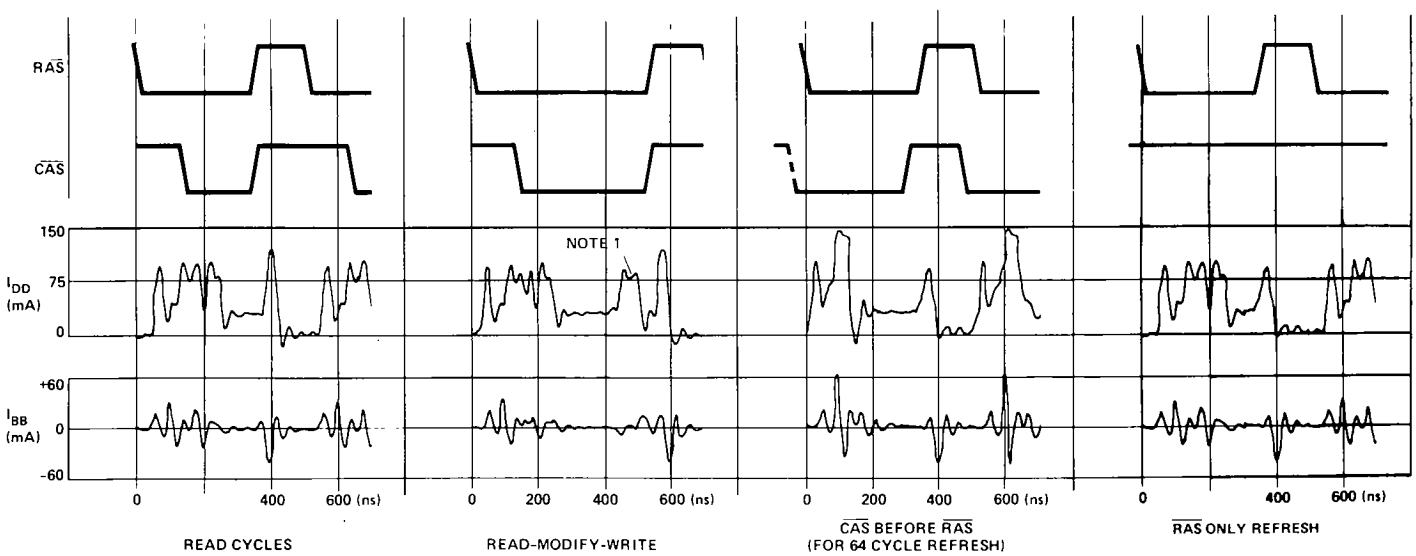
2. 64 cycle ($\overline{CAS}$ before $\overline{RAS}$); P_{OP} = 12.0V x 43 (0.96) mA = 495 mW.

   $$P_{REF} = 495\left(64\ \frac{0.425}{2000}\right) + (12x1.2+5x0.001)\left(1-64\ \frac{0.425}{2000}\right) =$$

   P_{REF} = 20.9 mW

3. 128 cycle ($\overline{RAS}$ only): P_{OP} = 12.0V x 43 (0.78) mA = 402 mW

   P_{REF} = 25.0 mW



Note 1: Increase in current due to $\overline{WE}$ going low. Width of this current pulse is independent of $\overline{WE}$ pulse width.

Figure 3. Supply Current Waveforms.

A.C. Characteristics[1]

T_A=0°C to 70°C, V_{DD}=12V ±10%, V_{CC}=5V ±10%, V_{BB}=-5V ±10%, V_{SS}=0V, unless otherwise noted.

READ, WRITE, READ-MODIFY-WRITE AND REFRESH CYCLES

Symbol	Parameter	2108-2 Min.	2108-2 Max.	2108-4 Min.	2108-4 Max.	Unit
t_{REF}	Time Between Refresh		2		2	ms
t_{RP}	$\overline{RAS}$ Precharge Time	75		95		ns
t_{CP}	$\overline{CAS}$ Precharge Time	100		125		ns
t_{RCL}[2]	$\overline{RAS}$ to $\overline{CAS}$ Leading Edge Lead Time	45	75	60	110	ns
t_{CRP}[3]	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	0		0		ns
t_{RSH}	$\overline{RAS}$ Hold Time	160		220		ns
t_{CSH}	$\overline{CAS}$ Hold Time	200		300		ns
t_{ASR}	Row Address Set-Up Time	0		0		ns
t_{ASC}	Column Address Set-Up Time	-10		-10		ns
t_{AH}	Address Hold Time	45		60		ns
t_T	Transition Time (Rise and Fall)		50		50	ns
t_{OFF}	Output Buffer Turn Off Delay	0	60	0	80	ns
t_{CAC}[4]	Access Time From $\overline{CAS}$		125		190	ns
t_{RAC}[4]	Access Time From $\overline{RAS}$		200		300	ns

READ AND REFRESH CYCLES

Symbol	Parameter	2108-2 Min.	2108-2 Max.	2108-4 Min.	2108-4 Max.	Unit
t_{CYC}[5]	Random Read Cycle Time	350		425		ns
t_{RAS}	$\overline{RAS}$ Pulse Width	275	32000	330	32000	ns
t_{CAS}	$\overline{CAS}$ Pulse Width	125	3000	190	3000	ns
t_{CH}	$\overline{CAS}$ Hold Time for $\overline{RAS}$-Only Refresh	30		30		ns
t_{CPR}	$\overline{CAS}$ Precharge for 64 Cycle Refresh	30		30		ns
t_{RCH}	Read Command Hold Time	20		20		ns
t_{RCS}	Read Command Set-Up Time	0		0		ns
t_{DOH}	Data-Out Hold Time	32		32		μs

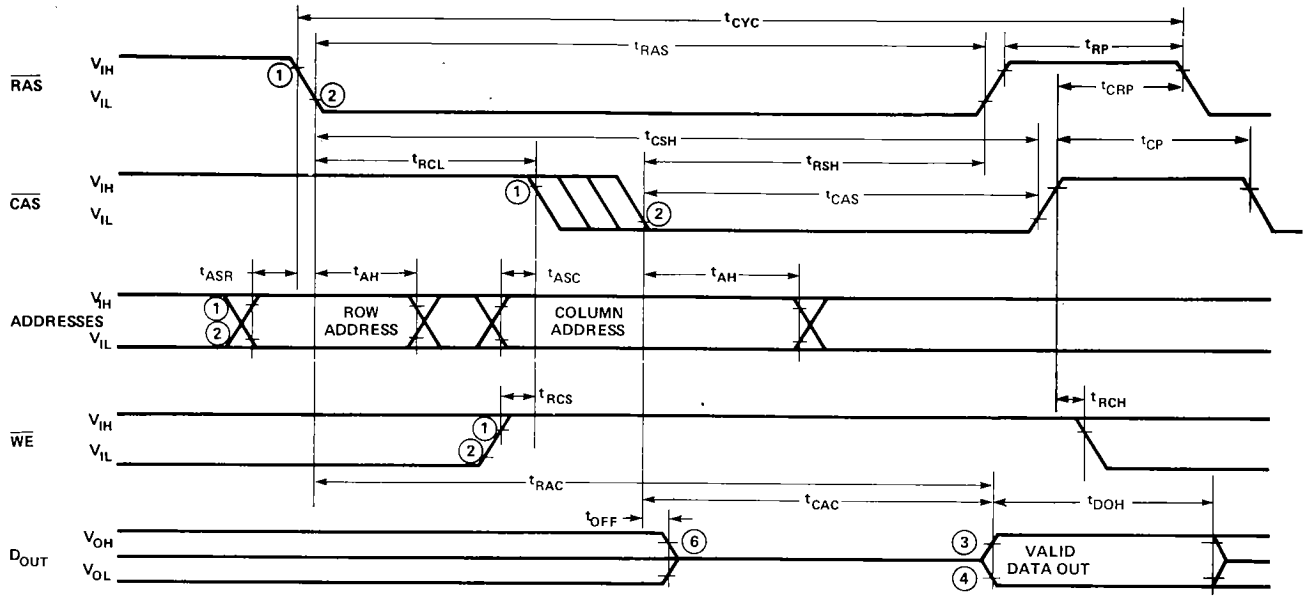
WRITE CYCLE

Symbol	Parameter	2108-2 Min.	2108-2 Max.	2108-4 Min.	2108-4 Max.	Unit
t_{CYC}[5]	Random Write Cycle Time	350		425		ns
t_{RAS}	$\overline{RAS}$ Pulse Width	275	32000	330	32000	ns
t_{CAS}	$\overline{CAS}$ Pulse Width	125	10000	190	10000	ns
t_{WCH}	Write Command Hold Time	75		100		ns
t_{WP}	Write Command Pulse Width	50		100		ns
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	125		200		ns
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	100		160		ns
t_{DS}[6]	Data-In Set-Up Time	0		0		ns
t_{DH}[6]	Data-In Hold Time	100		125		ns

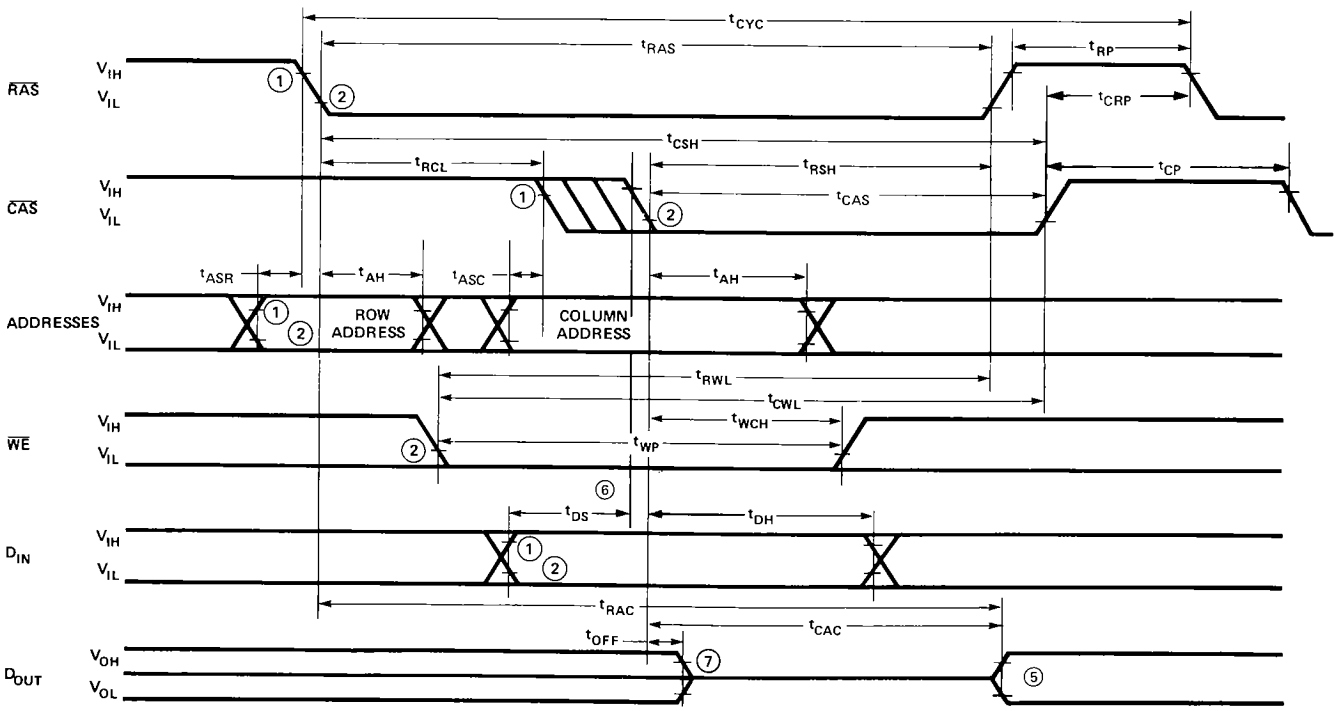
Notes: 1. All voltages referenced to V_{SS}.
2. $\overline{CAS}$ must remain at V_{IH} a minimum of $t_{RCL\ MIN}$ after $\overline{RAS}$ switches to V_{IL}. To achieve the minimum guaranteed access time (t_{RAC}), $\overline{CAS}$ must switch to V_{IL} at or before $t_{RCL\ (MAX)} = t_{RAC} - t_{CAC}$. Device operation is not guaranteed for $t_{RCL} > 2$ μs.
3. The t_{CRP} specification is less restrictive than the t_{CRL} range which was specified in the 2108 preliminary data sheet.
4. Load = 1 TTL and 50 pF.
5. The minimum cycle timing does not allow for t_T or skews.
6. Referenced to $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.

Waveforms

READ CYCLE



WRITE CYCLE



Notes:
1,2. V_{IH} MIN and V_{IL} MAX are reference levels for measuring timing of input signals.
3,4. V_{OH} MIN and V_{OL} MAX are reference levels for measuring timing of D_{OUT}.
5. D_{OUT} follows D_{IN} when writing, with $\overline{WE}$ before $\overline{CAS}$.
6. Referenced to $\overline{CAS}$ or $\overline{WE}$, whichever occurs last.
7. t_{OFF} is measured to $|I_{OUT}| \leq |I_{LO}|$.

A.C. Characteristics

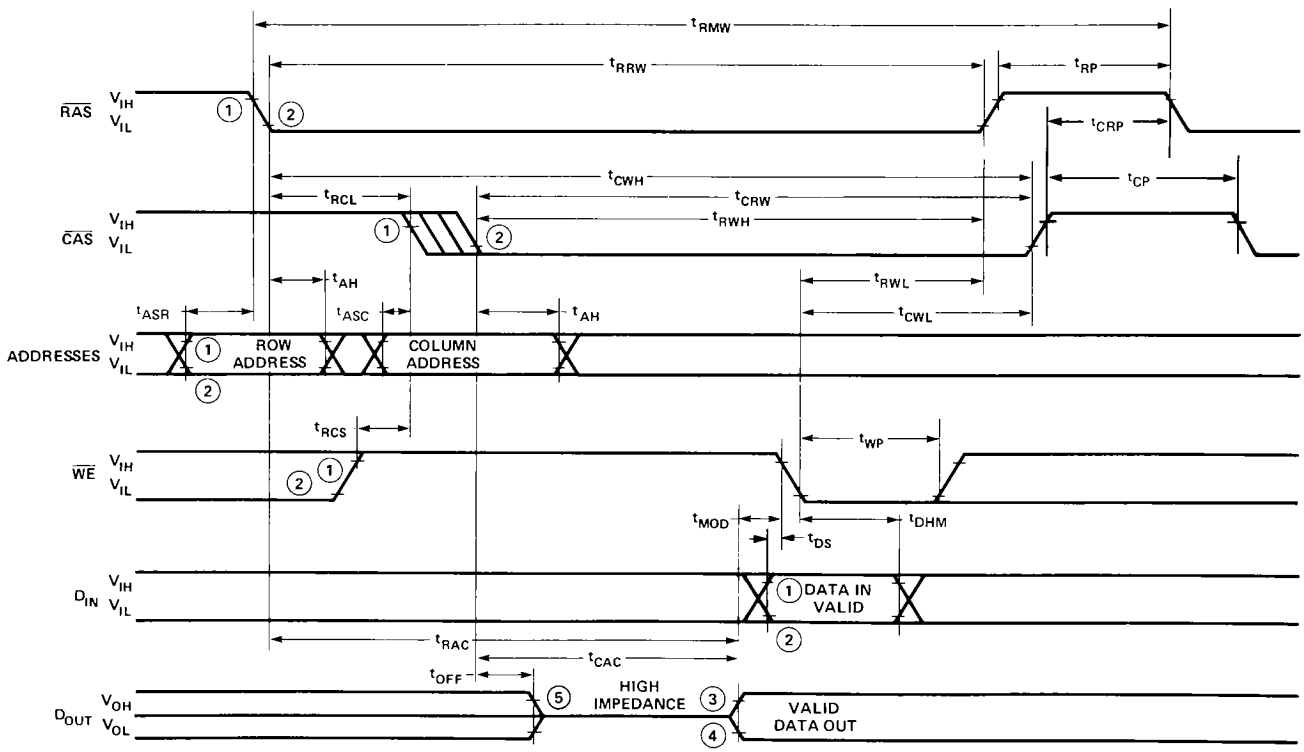
T_A = 0°C to 70°C, V_{DD} = 12V ±10%, V_{CC} = 5V ±10%, V_{BB} = −5V ±10%, V_{SS} = 0V, unless otherwise noted.

READ-MODIFY-WRITE CYCLE

Symbol	Parameter	2108-2 Min.	2108-2 Max.	2108-4 Min.	2108-4 Max.	Unit
t_{RMW}	Read-Modify-Write Cycle Time	400		595		ns
t_{CRW}	RMW Cycle $\overline{CAS}$ Width	225	3000	350	3000	ns
t_{RRW}	RMW Cycle $\overline{RAS}$ Width	325	32000	500	32000	ns
t_{RWH}	RMW Cycle $\overline{RAS}$ Hold Time	250		390		ns
t_{CWH}	RMW Cycle $\overline{CAS}$ Hold Time	300		460		ns
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	125		200		ns
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	100		160		ns
t_{WP}	Write Command Pulse Width	50		100		ns
t_{RCS}	Read Command Set-Up Time	0		0		ns
t_{MOD}	Modify Time	0	10	0	10	μs
t_{DS}	Data-In Set-Up Time	0		0		ns
t_{DHM}	Data-In Hold Time (RMW Cycle)	50		125		ns

Waveforms

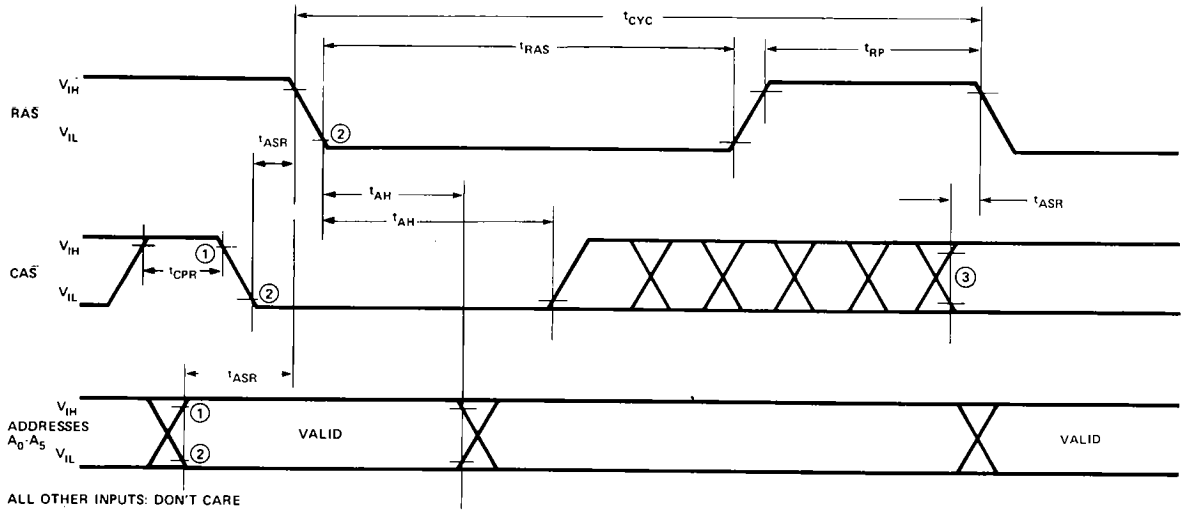
READ MODIFY WRITE CYCLE



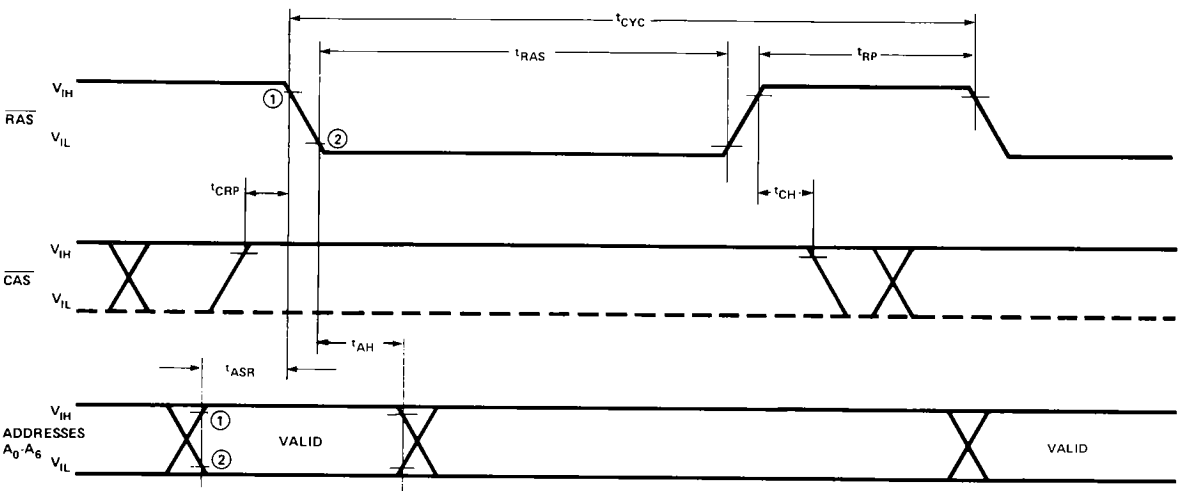
Notes: 1,2. V_{IHMIN} and V_{ILMAX} are reference levels for measuring timing of input signals.
3,4. V_{OHMIN} and V_{OLMAX} are reference levels for measuring timing of D_{OUT}.
5. t_{OFF} is measured to $I_{OUT} \leq |I_{LO}|$.

Refresh Cycle Waveforms

$\overline{CAS}$ BEFORE $\overline{RAS}$ CYCLES. (64 CYCLE REFRESH)



$\overline{RAS}$ ONLY CYCLES (128 CYCLE REFRESH)



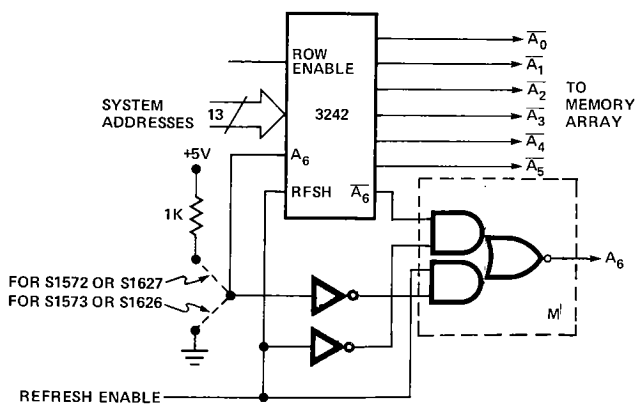
Notes: 1,2. V_{IHMIN} and V_{ILMAX} are reference levels for measuring timing of input signals.
.3. $\overline{CAS}$ must be high or low as appropriate for the next cycle.

Applications Information

The 2108 may be refreshed in any of three modes: read cycles with $\overline{RAS}$ before $\overline{CAS}$ timing as shown on page 5, $\overline{RAS}$ only cycles (page 7), or $\overline{CAS}$ before $\overline{RAS}$ cycles (page 7). In all three modes A_6 must be held high for the S1572 and S1627 or low for the S1573 and S1626. The row addressed by A_0 through A_5 is refreshed. Therefore, 64 cycles are required to refresh the stored data.

The $\overline{CAS}$-before-$\overline{RAS}$ mode is useful in the 2116 as a technique for increasing memory availability and minimizing standby power dissipation by requiring only 64 refresh cycles every 2 ms. Systems employing the 2108 in a $\overline{CAS}$-before-$\overline{RAS}$ refresh mode can be easily upgraded to the most efficient 16K RAM capability.

Since the 2108 input pin A_6 supplies two system addresses (A_6 and A_{13}) to the internal memory array, it is not possible to simply tie this input high or low. The 2108 input A_6 must be tied to the appropriate level only during row address strobe ($\overline{RAS}$) and then used to supply the high order system address A_{13} during column address strobe ($\overline{CAS}$). Control of A_6 in a system may be implemented. as shown at right. In this circuit the output A_6 of multiplexer M supplies the appropriate high or low level (determined by S1572, S1627, S1573, or S1626) during $\overline{RAS}$ for both a memory cycle and refresh cycle. During $\overline{CAS}$, system address A_{13} is multiplexed on A_6 as shown. See the 2116 section for additional applications information.



Power Supply Decoupling/ Distribution

Power supply current waveforms for the 2108 are shown in Figure 3. The V_{DD} supply provides virtually all of the operating current for the 2108. The V_{DD} supply current, I_{DD}, has two components: transient current peaks when the clocks change state and a DC component while the clocks are active (low). When selecting the decoupling capacitors for the V_{DD} supply, the characteristics of capacitors as well as the current waveform must be considered. Suppression of transient or pulse currents require capacitors with small physical size and low inherent inductance. Monolithic and other ceramic capacitors exhibit these desirable characteristics. When the current waveform indicates a DC component, bulk capacity must be located near the current load to supply the load power. Inductive effects of PC board traces and bus bars preclude supplying the DC component from bulk capacitors at the periphery of a memory matrix without voltage droop during the active portion of a memory cycle. This means that some bulk capacity in the form of electrolytic or large ceramic capacitors should be distributed around or within the memory matrix.

The V_{BB} supply current, I_{BB}, has high transient current peaks, with essentially no DC component (less than 400 microamperes). The V_{BB} capacitors should be selected for transient suppression characteristics. The following capacitance values and locations are recommended for the 2108:

1. A 0.33 μF ceramic capacitor between V_{DD} and V_{SS} (ground) at every other device.
2. A 0.1 μF ceramic capacitor between V_{BB} and V_{SS} at every other device (preferably alternate devices to the V_{DD} decoupling above).
3. A 4.7 μF electrolytic capacitor between V_{DD} and V_{SS} for each eight devices and located adjacent to the devices.

The V_{CC} supply is connected only to the 2108 output buffer and is not used internally. The load current from the V_{CC} supply is dependent only upon the output loading and is usually only the input high level current to a TTL gate and the output leakage currents of any OR-tied 2108 (typically 100 μA or less total). Intel recommends that a 0.1 or 0.01 μF ceramic capacitor be connected between V_{CC} and V_{SS} for every eight devices to preclude coupled noise from affecting the TTL devices in the system.

Intel recommends a power supply distribution system such that each power supply is grided both horizontally and vertically at each memory device. This technique minimizes the power distribution system impedance and enhances the effect of the decoupling capacitors.

Output Data Latch

The 2108 contains an output data latch eliminating the need for an external system data latch and the timing circuitry required to strobe an external latch. The output latch operates identically to the 16-pin 4K RAM (Intel 2104) output latch enhancing the system compatibility of the 16K and 4K devices.

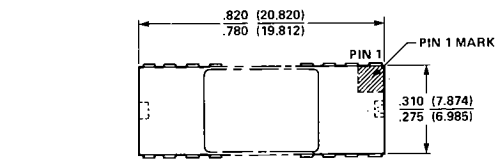
Operation of the output latch is controlled by $\overline{CAS}$. The data output will go to the high-impedance state immediately following the $\overline{CAS}$ leading edge during each data cycle and will either go to valid data at access time on selected devices (devices receiving both $\overline{RAS}$ and $\overline{CAS}$) or will remain in the high impedance state on unselected devices (devices receiving only $\overline{CAS}$). During $\overline{RAS}$-only refresh cycles, the data output remains in the state it was prior to the $\overline{RAS}$-only cycle. This unique feature of latched output RAMs allows a refresh cycle to be hidden among data cycles without impacting data availability. For instance, a $\overline{RAS}$-only refresh cycle could follow each data cycle in a microprocessor system but the accessed data would remain at the device output and the microprocessor could take the data at any time within the cycle. Non-latched output devices do not provide this type of hidden refresh capability since their data output would go to the high impedance state at the end of the data cycle.

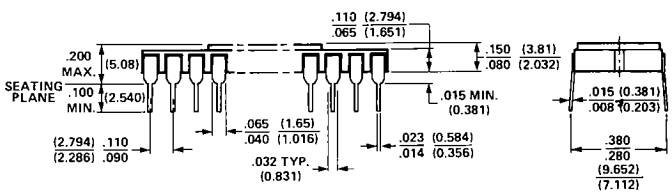
Page Mode Operation

The 2108 is designed for page mode operation and is presently being characterized for that mode. Specifications will be available at a later date.

Packaging Information

16-LEAD HERMETIC DUAL IN-LINE PACKAGE





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