TTL ISOPLANAR MEMORY 93L421

256×1—BIT FULLY DECODED RANDOM ACCESS MEMORY

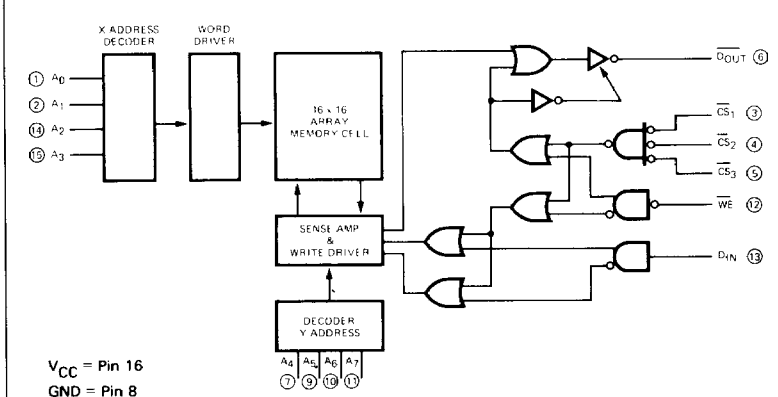
DESCRIPTION – The 93L421 is a low power 256-bit Read/Write Random Access Memory organized 256 words by one bit. It is designed for scratchpad, buffer and distributed main memory applications requiring low power. The device has three Chip Select lines to simplfy its use in larger memory systems. Address input locations are specifically chosen to permit maximum packaging density and for ease of PC board layout. A 3-state output is provided to drive bus organized systems and/or highly capacitive loads.

- **3-STATE OUTPUT**
- **ORGANIZATION – 256 WORDS X 1 BIT**
- **THREE HIGH-SPEED CHIP SELECT INPUTS**
- **TYPICAL READ ACCESS TIME – 45 ns**
- **ON-CHIP DECODING**
- **POWER DISSIPATION – 275 mW TYPICAL**
- **POWER DISSIPATION DECREASES WITH TEMPERATURE**
- **INVERTED DATA OUTPUT**

PIN NAMES		LOADING (Notes a, b)
$\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$	Chip Select Inputs	0.5 U.L.
$A_0 - A_7$	Address Inputs	0.5 U.L.
D_{IN}	Data Input	0.5 U.L.
$\overline{D_{OUT}}$	Data Output	10 U.L.
$\overline{WE}$	Write Enable	0.5 U.L.

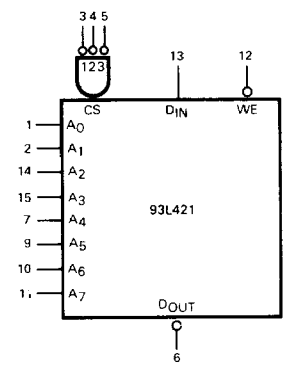
NOTES:
a. 1 Unit Load (U.L.) = 40 μA HIGH / 1.6 mA LOW
b. 10 U.L. is the output LOW drive factor. This output will sink a maximum of 16 mA at V_{OUT} = 0.45 V, and will source a minimum of 10 mA at 2.4 V

LOGIC DIAGRAM



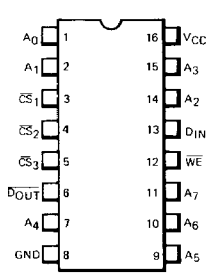
V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The 93L421 is a fully decoded 256-bit Random Access Memory organized 256 words by one bit. Word selection is achieved by means of an 8-bit address, A_0 through A_7.

Three Chip Select inputs are provided for logic flexibility. For larger memories, the fast chip select access time permits the decoding of Chip Select, $\overline{CS}$, from the address without increasing address access time.

The read and write operations are controlled by the state of the active LOW Write Enable ($\overline{WE}$, pin 12). With $\overline{WE}$ held LOW and the chip selected, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH and the chip selected. Data in the specified location is presented at $\overline{D_{OUT}}$.

The 3-state output provides drive capability for higher speeds with high capacitive load systems The third state (high impedance) allows bus organized systems where multiple outputs are connected to a common bus.

During writing, the output is held in the high impedance state.

TABLE I – TRUTH TABLE

INPUTS					OUTPUT	
$\overline{CS}_1$	$\overline{CS}_2$	$\overline{CS}_3$	$\overline{WE}$	D_{IN}	$\overline{D_{OUT}}$	MODE
H	X	X	X	X	HIGH Z	Not Selected
X	H	X	X	X	HIGH Z	Not Selected
X	X	H	X	X	HIGH Z	Not Selected
L	L	L	L	L	HIGH Z	Write "0"
L	L	L	L	H	HIGH Z	Write "1"
L	L	L	H	X	$\overline{D_{OUT}}$	Read inverted data from addressed location

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care (HIGH or LOW)
HIGH Z = High Impedance

TABLE 2 – FUNCTION TABLE

FUNCTION	INPUTS		OUTPUT
	CHIP SELECT	WRITE ENABLE	
Write	L	L	HIGH Z
Read	L	H	Stored Data
Not Selected	H	X	HIGH Z

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−12 mA to +5.0 mA
**Voltage Applied to Outputs (output HIGH)	−0.5 V to +5.50 V
Output Current (dc) (output LOW)	+20 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.
**Output Current Limit Required.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE Note 4
	MIN	TYP	MAX	
93L421XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93L421XM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS: Over Operating Temperature Ranges. Notes 1, 2 and 4

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP (Note 3)	LIMITS MAX	UNITS	CONDITIONS
V_{OL}	Output LOW Voltage			0.3	0.45	V	V_{CC} = MIN, I_{OL} = 16 mA
V_{IH}	Input HIGH Voltage		2.0	1.6		V	Guaranteed Input Logical HIGH Voltage for all Inputs
V_{IL}	Input LOW Voltage			1.5	0.85	V	Guaranteed Input Logical LOW Voltage for all Inputs
I_{IL}	Input LOW Current			−530	−800	μA	V_{CC} = MAX, V_{IN} = 0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 4.5 V
I_{OFF}	Output Current (HIGH Z)				50 −50	μA	V_{CC} = MAX, V_{OUT} = 2.4 V V_{CC} = MAX, V_{OUT} = 0.5 V
V_{CD}	Input Clamp Diode Voltage			−1.0	−1.5	V	V_{CC} = MAX, I_{IN} = −10 mA
I_{CC}	Power Supply Current	93L421XC		55	70	mA	T_A = 0°C to +75°C; V_{CC} = MAX, WE Grounded, all other inputs @ 4.5 V, see Power Supply vs Temp. Curve
		93L421XM		55	70		T_A = −55°C to +125°C
V_{OH}	Output HIGH Voltage	93L421XC	2.4			V	I_{OH} = −10.3 mA
		93L421XM	2.4			V	I_{OH} = −5.2 mA
I_{OS}	Output Current Short Circuit to Ground				−100	mA	V_{CC} = MAX, Note 7

AC CHARACTERISTICS: Over Guaranteed Operating Ranges. Notes 1, 2, 4, 5, 6

SYMBOL	CHARACTERISTIC	93L421XC MIN	93L421XC TYP (Note 3)	93L421XC MAX	93L421XM MIN	93L421XM TYP (Note 3)	93L421XM MAX	UNITS	CONDITIONS
READ MODE	DELAY TIMES								
t_{ACS}	Chip Select Access Time		30	40		35	50		See Test Circuit
t_{ZRCS}	Chip Select to HIGH Z		30	40		30	50	ns	and Waveforms
t_{AA}	Address Access Time		45	90		45	100		Note 5
WRITE MODE	DELAY TIMES								
t_{ZWS}	Write Disable to HIGH Z		30	45		30	55	ns	
t_{WR}	Write Recovery Time		50	60		65	70		
	INPUT TIMING REQUIREMENTS								
t_W	Minimum Write Pulse Width	60	20		70	20			See Test Circuit
t_{WSD}	Data Set-Up Time Prior to Write	5	0		5	0			and Waveforms
t_{WHD}	Data Hold Time After Write	5	0		5	0			Note 6
t_{WSA}	Address Set-Up Time	10	0		15	0		ns	
t_{WHA}	Address Hold Time	10	0		10	0			
t_{WSCS}	Chip Select Set-Up Time	0	0		0	0			
t_{WHCS}	Chip Select Hold Time	0	0		0	0			
C_{IN}	Input Capacitance		2.5	3.5		2.5	3.5	pF	Measured with a
C_{OUT}	Output Capacitance		5	7		5	7		pulse technique

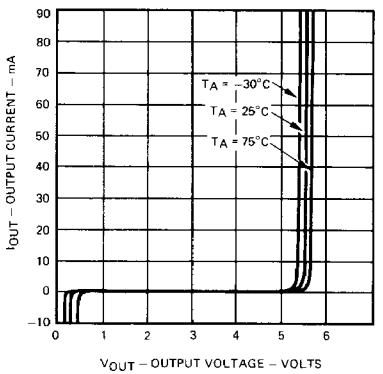
NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represents the "worst case" value for the parameters. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values are at V_{CC} = 5.0 V, T_A = +25°C, and MAX loading.
4. The Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute. For military range an additional requirement of a two minute warm-up. Temperature range of operation refers to case temperature for Flatpaks and ambient temperature for all other packages. Typical thermal resistance values of the package at maximum temperature are:

   θ_{JA} (Junction to Ambient) (at 400 fpm air flow) = 50°C/Watt, Ceramic DIP; 65°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JA} (Junction to Ambient) (still air) = 90°C/Watt, Ceramic DIP; 110°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JC} (Junction to Case) = 25°C/Watt, Ceramic DIP; 25°C/Watt, Plastic DIP; 10°C/Watt, Flatpak.

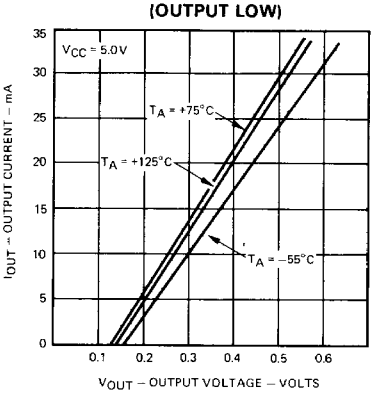
5. The MAX address access time is guaranteed to be the "worst case" bit in the memory using a pseudo random testing pattern.
6. t_W measured at t_{WSA} = MIN, t_{WSA} measured at t_W = MIN.
7. Duration of short circuit should not exceed one second.

TYPICAL ELECTRICAL CHARACTERISTICS

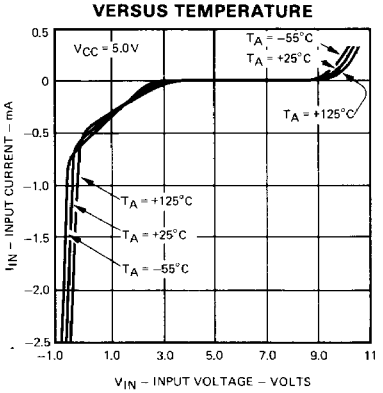
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH Z STATE)



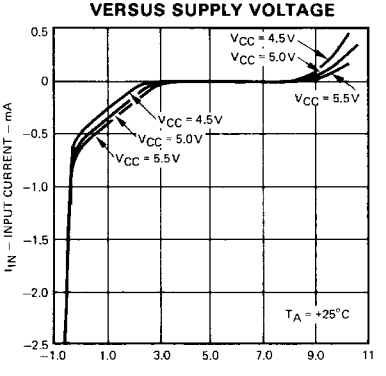
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



INPUT CURRENT VERSUS INPUT VOLTAGE VERSUS TEMPERATURE



INPUT CURRENT VERSUS INPUT VOLTAGE VERSUS SUPPLY VOLTAGE



AC Test Load and Waveforms same as 93L420, see page 7-93, 7-94 & 7-95.