M27C256/E27C256
256K CMOS EPROM

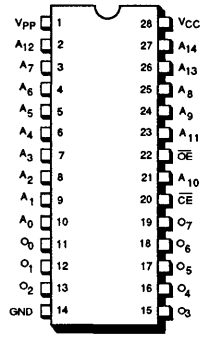
November 1989

Features

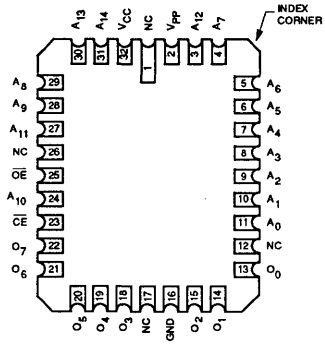
- **256K (32K x 8) CMOS EPROM**
- **Military and Extended Temperature Range**
  - **–55°C to +125°C: M27C256**
  - **–40°C to +85°C: E27C256**
- **Ultra Low Power**
  - **150 µA Max. V_{CC} Standby Current**
  - **50 mA Max. Active Current**
- **Programmed Using Intelligent Algorithm**
  - **12.5 V V_{PP}**
- **200 ns Access Times**
- **5 V± 10% V_{CC}**
- **JEDEC Approved Bytewide Pin Configuration**
- **Silicon Signature®**

Pin Configuration

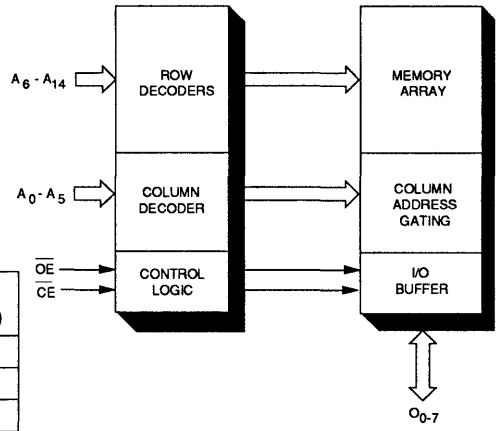
DUAL-IN-LINE



LEADLESS CHIP CARRIER
BOTTOM VIEW



Block Diagram



Description

SEEQ's 27C256 is the industry's first 256K CMOS EPROM. It has a 32K x 8 organization and has very low power dissipation. Its active current is less than one half the active power of n-channel EPROMs. In addition the standby current is orders of magnitude lower than those

Mode Selection

PINS / MODE	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	Outputs (11-13, 15-19)
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IH}	V_{IL}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	V_{CC}	High Z
Silicon Signature*	V_{IL}	V_{IL}	V_{CC}	V_{CC}	Encoded Data

X can be either V_{IL} or V_{IH}
*For Silicon Signature: A_0 is toggled, A_9 = 12V, and all other addresses are at a TTL low.

Silicon Signature is a registered trademark of SEEQ Technology, Inc.

Pin Names

$A_0 - A_5$	ADDRESSES – COLUMN (LSB)
$A_6 - A_{14}$	ADDRESSES – ROW
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$O_0 - O_7$	OUTPUTS
NC	NO CONNECT

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same EPROMs. Consequently, system memory sizes can be substantially increased at a very small increase in power. Low active and standby power is important in applications which require portability, low cooling cost, high memory bit density, and long term reliability.

The 27C256 is specified over both the extended and military temperature ranges at 5 V± 10% V_{CC}. The access time is specified at 200 ns, making the 27C256 compatible with most of today's microprocessors. Its inputs and outputs are completely TTL compatible.

Absolute Maximum Ratings

Temperature
Storage ..... −65°C to +150°C
M27C256 Under Bias ..... −65°C to +135°C
E27C256 Under Bias ..... −50°C to +95°C
All Inputs or Outputs
with Respect to Ground ..... +7 V to −0.6 V
V_{PP} with Respect to Ground ..... +14.0 V to −0.6 V
Voltage on A_9
with Respect to Ground ..... +14.0 V to −0.6 V

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions

	M27C256-20, M27C256-25 M27C256-30	E27C256-20, E27C256-25 E27C256-30
V_{CC} Supply Voltage[1]	5V ± 10%	5V ± 10%
Temperature Range (Read Mode)	(Case) −55°C to +125°C	(Ambient) −40°C to +85°C
V_{PP} During Read[2]	V_{CC}	V_{CC}
V_{PP} During Programming[3]	12.5 ± 0.3V	12.5 ± 0.3V

DC Operating Characteristics During Read or Programming

Symbol	Parameter	Limits Min.	Limits Max.	Units	Test Condition
I_{IN}[4]	Input Leakage		1	µA	$V_{IN} = V_{CC}$ Max.
I_O[5]	Output Leakage		10	µA	$V_{OUT} = V_{CC}$ Max.
I_{PP}	V_{PP} Current Standby Mode Read Mode Programming Mode		 150 1 30	 µA mA mA	 $\overline{CE} = V_{CC} - 1$ v. min. F = 5 MHz, $\overline{CE} = V_{IL}$ $V_{PP} = 12.5$ v.
I_{CC_1}	V_{CC} Standby Current		150	µA	$\overline{CE} \geq V_{CC} - 1$ v.
I_{CC_2}	V_{CC} Standby Current		2	mA	$\overline{CE} = V_{IH}$
I_{CC_3}	V_{CC} Active Current		50	mA	$\overline{CE} = \overline{OE} = V_{IL}$, $O_{0-7} = 0$, F = 5 MHz.
V_{IL}	Input Low Voltage	−0.1	0.8	V	
V_{IH}	Input High Voltage	2.0	$V_{CC} + 1$	V	
V_{OL}	Output Low Voltage		0.45	V	$I_{OL} = 2.1$ ma
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -400$ µA.

NOTES:
1. V_{CC} must be appied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} cannot be left floating and should be connected to V_{CC} during read.
3. 0.1 µF ceramic capacitor on V_{PP} is required during programming only, to suppress voltage transients.
4. Inputs only. Does not include I/O.
5. For I/O only.

AC Operating Characteristics During Read

Symbol	Parameter	Limits (nsec)						Test Conditions
		M27C256-20 E27C256-20		M27C256-25 E27C256-25		M27C256-30 E27C256-30		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address Access Time		200		250		300	$\overline{CE}=\overline{OE}=V_{IL}$
t_{CE}	Chip Enable to Data Valid		200		250		300	$\overline{OE}=V_{IL}$
t_{OE} [2]	Output Enable to Data Valid		75		100		120	$\overline{CE}=V_{IL}$
t_{DF} [3]	Output Enable or Chip Enable to Output Float		60		60		105	$\overline{CE}=V_{IL}$
t_{OH}	Output Hold from Chip Enable, Addresses, or Output Enable whichever occured first	0		0		0		$\overline{CE}=\overline{OE}=V_{IL}$

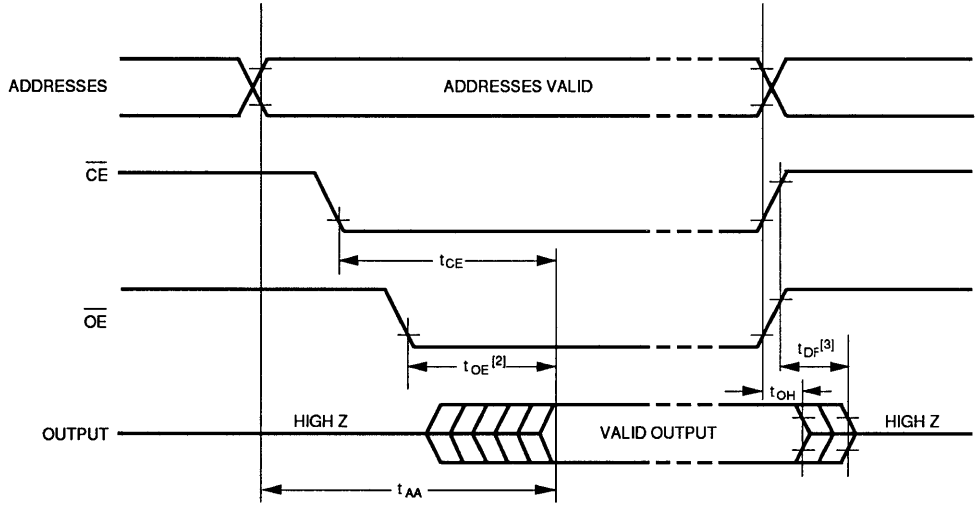
Capacitance [1]

Symbol	Parameter	Typ.	Max	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	V_{IN} = 0 V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0 V

Equivalent A.C. Test Conditions [4]

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤ 20 ns
Input Pulse Levels: 0.45V to 2.4V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

A.C. Waveforms



NOTES:
1. This parameter is sampled and is not 100% tested.
2. $\overline{OE}$ may be delayed to $t_{AA} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{AA}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
4. These are equivalent test conditions and actual test conditions are dependent on the tester.

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Initially and after erasure, all bits are in the "1" state. An intelligent algorithm is used to program the 27C256 typically in four minutes. Data is programmed using a 12.5V V_{PP} and an initial chip enable pulse of 1.0 ms.

Incorporated on the 27C256 is Silicon Signature. Silicon Signature contains encoded data which identifies SEEQ as the EPROM manufacturer and gives the product code. This data is encoded in ROM to prevent erasure by ultraviolet light.

Erasure Characteristics

The 27C256 is erased using ultraviolet light which has a wavelength of 2537 Angstroms. The integrated dose, i.e., intensity x exposure time, for erasure is a minimum of 15 watt-seconds/cm². The EPROM should be placed within one inch of the lamp tube during erasure. Table 1 shows the typical EPROM erasure time for various light intensities.

Table 1. Typical EPROM Erasure Time

Light Intensity (Micro-Watts/cm²)	Erasure Time (Minutes)
15,000	20
10,000	30
5,000	55

Silicon Signature

Incorporated in SEEQ's EPROMs is a row of mask programmed read only memory (ROM) cells which is outside of the normal memory cell array. The ROM contains the EPROM's Silicon Signature. Silicon Signature contains data which identifies SEEQ as the manufacturer and gives the product code. This data allows programmers to match the programming specification against the product which is to be programmed. If there is verification, then the programmer proceeds to program.

Silicon Signature is activated by raising address A_9 to 12V ± 0.5V, bringing chip enable and output enable to a TTL low, having all addresses except A_0 at a TTL low. The Silicon Signature data is then accessed by toggling A_0. The data appears on outputs O_0 to O_6, with O_7 used as an odd parity bit (see Table 2).

Table 2. Silicon Signature Bytes

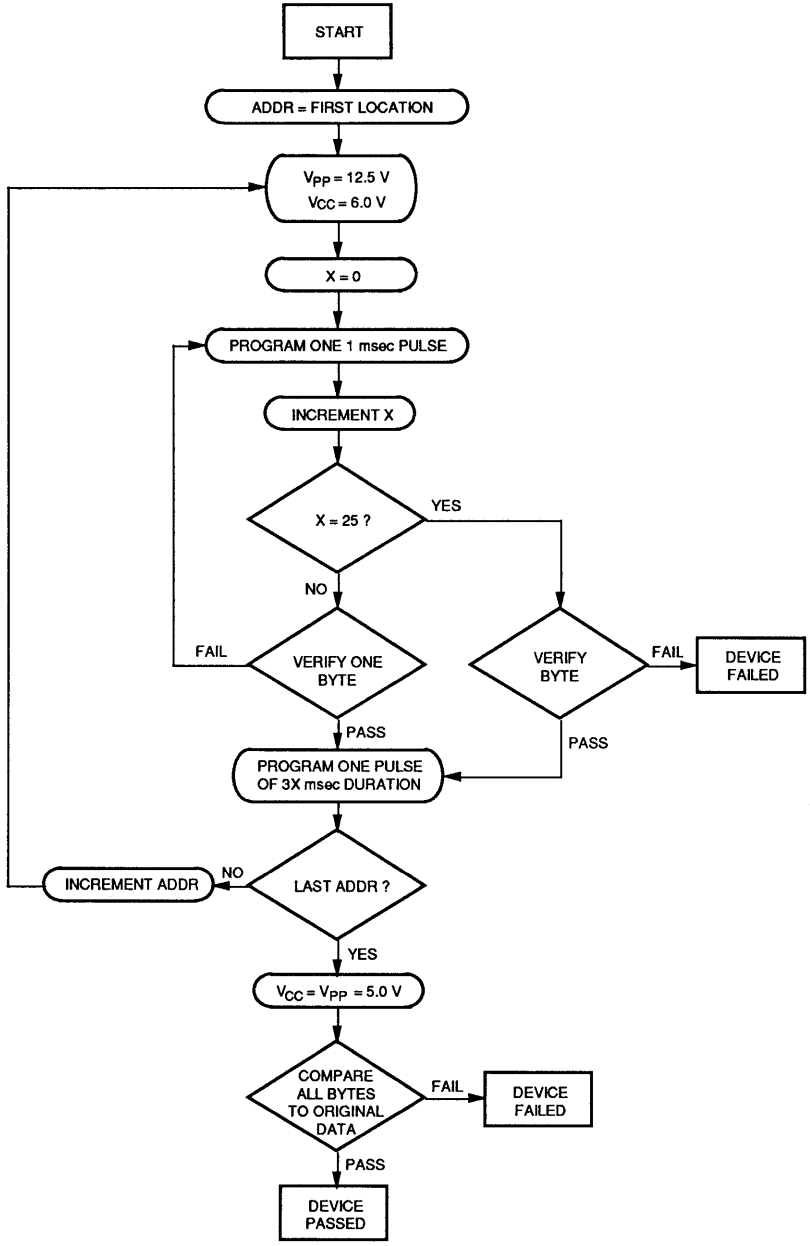
	A_0	Data (Hex)
SEEQ Code (Byte 0)	V_{IL}	94
Product Code (Byte 1)	V_{IH}	C2

Programming

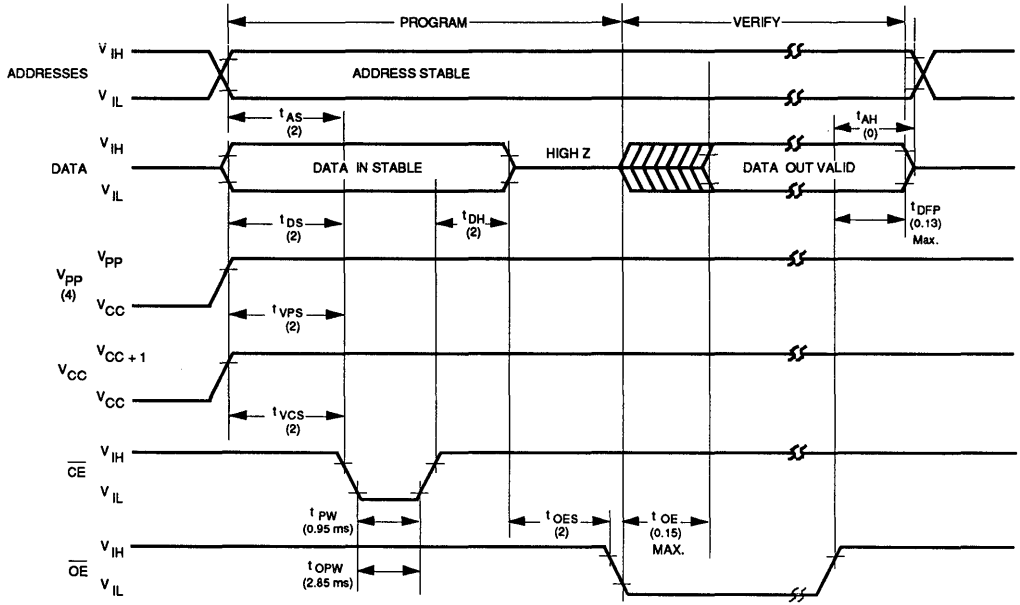
The 27C256 is programmed using the industry standard intelligent algorithm.

The intelligent algorithm requires V_{CC} = 6 V and V_{PP} = 12.5 V during byte programming. The initial program pulse width is 1.0 millisecond, followed by a sequence of 1.0 millisecond pulses. A byte is verified after each pulse. A single program pulse, with a time duration equal to 3 times the number of 1.0 millisecond pulses applied, is additionally given to the address after it is verified as being correctly programmed. A minimum of one to a maximum of 25 1-ms pulses, plus one 3X overpulse, may be applied to each byte. When the intelligent algorithm cycle has been completed, all bytes must be read at V_{CC} = V_{PP} = 5 V.

Intelligent Algorithm Flowchart



Intelligent Algorithm



NOTES:
1. All times shown in ( ) are minimum and in µsec unless otherwise specified.
2. The input timing reference level is 0.8 V for a V_{IL} and 2 V for a V_{IH}.
3. t_{OE} and t_{DFP} are characteristics of the device but must be accomodated by the programmer.
4. 0.1 µF ceramic capacitor on V_{PP} is required during programming only, to suppress voltage transients.

Intelligent Algorithm

AC Programming Charateristics T_A =25° ± 5°C, V_{CC}[1] = 6.0 V ± 0.25 V, V_{PP} = 12.5 V

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{AS}	Address Setup Time	2			µs
t_{OES}	$\overline{OE}$ Setup Time	2			µs
t_{DS}	Data Setup Time	2			µs
t_{AH}	Address Hold Time	0			µs
t_{DH}	Data Hold Time	2			µs
t_{DFP}	Output Enable to Output Float Delay	0		130	ns
t_{VPS}	V_{PP} Setup Time	2			µs
t_{VCS}	V_{CC} Setup Time	2			µs
t_{PW}	$\overline{CE}$ Initial Program Pulse Width	0.95	1.0	1.05	ms
t_{OPW}[3]	$\overline{CE}$ Overprogram Pulse Width	2.85		78.75	ms
t_{OE}	Data Valid from $\overline{OE}$			150	ns

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The length of the overprogram pulse will vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X.

AC Conditions of Test

Input Rise and Fall Times (10% to 90%) ..... 20 ns
Input Pulse Levels ..... 0.45 V to 2.4 V
Input Timing Reference Level ..... 0.8 V and 2.0 V
Output Timing Reference Level ..... 0.8 V and 2.0 V

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Ordering Information