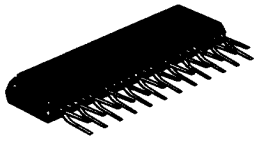
M5M4C264L-10,-12,-15

262144-BIT DUAL-PORT DYNAMIC RAM



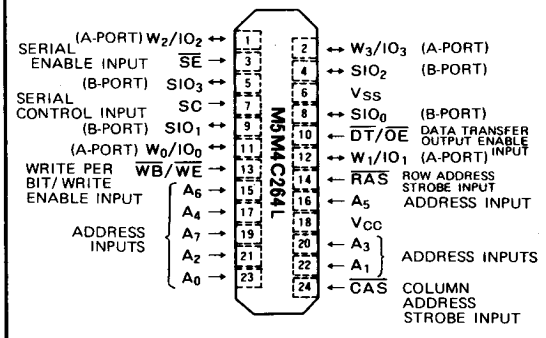
DESCRIPTION

The Mitsubishi M5M4C264L is a high speed 262,144-bit Dual Port Dynamic Memory equipped with a 64K x 4 Dynamic RAM Port and a 256 x 4 Serial Read/Write Port. The use of N-well CMOS Process combined with silicide technology and a single transistor dynamic storage cell provide high circuit density and low power dissipation.

The Serial Read/Write Port is connected to an internal 1024 bit Data Register through a 256 x 4 Serial Input/Output Control and is serially read out or written in with a clock rate of up to 25MHz.

All reads and writes are done relative to the RAM Array, thus Data transfer from the RAM array to the Data Register is referred to as Read Transfer, while Data Transfer from the Data Register to the RAM array is referred to as Write Transfer.

PIN CONFIGURATION (TOP VIEW)



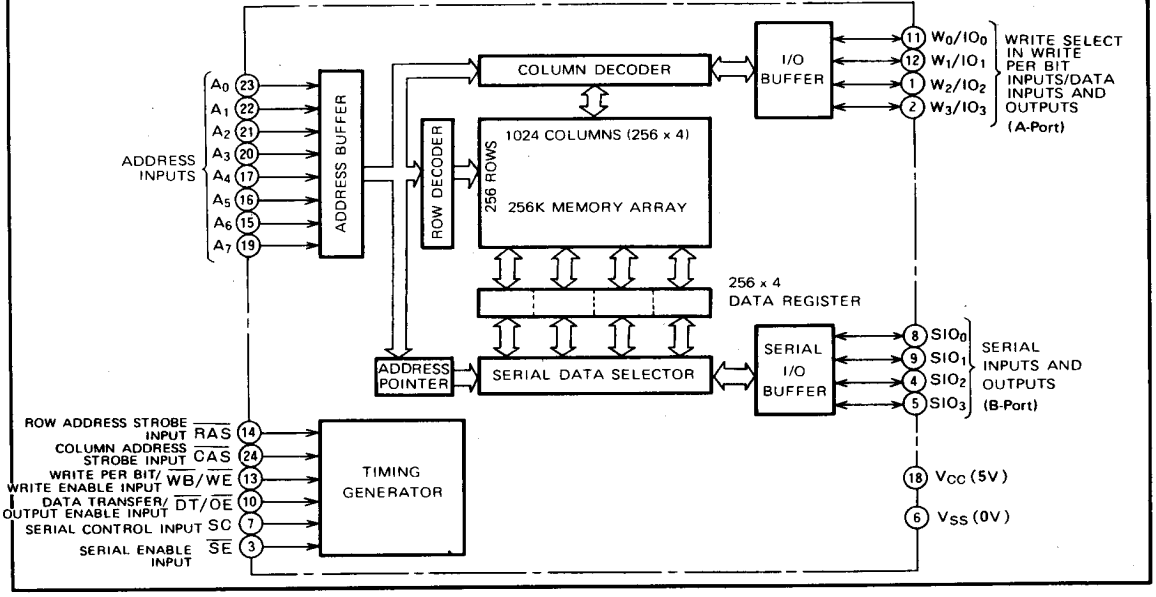
Outline 24P5L

FEATURES

Type name	RAS Access Time	Random Read/Write Cycle Time	Serial Read/Write Cycle Time	Random Read/Write VCC Supply Current	Serial Read/Write VCC Supply Current
M5M4C264L-10	100ns	200ns	35ns	70mA	45mA
M5M4C264L-12	120ns	220ns	40ns	60mA	40mA
M5M4C264L-15	150ns	260ns	60ns	50mA	30mA

- Dual Port Architecture
  - RAM Port: 64K word x 4 bit
    - Access Time . . . . . 100ns (MAX)
  - Serial Read/Write Port: 256 word x 4 bit
    - Cycle Time . . . . . 35ns (MAX)
- Bidirectional Data Transfer function between the RAM array and the Data Register.
- Fully Asynchronous Dual Port Accessability (except during the Data Transfer Period.)
- Addressable Start of Serial Read/Write (Pointer Control Function)
- Write per Bit Function.
- Real Time Data Transfer from the RAM Array to the Data Register.
- Page Mode, Hidden Refresh and CAS before RAS Refresh.
- 256 cycles/4ms Refresh.
- Fully TTL Compatible.

BLOCK DIAGRAM



- Outline 24 Pin ZIP
- N-well CMOS Process & Low Power dissipation
  RAM & SAM Active (-10/-12/-15)
  . . . . . 115/100/80mA max
  RAM & SAM Standby (-10/-12/-15)
  . . . . . 5/5/5mA max

APPLICATION

Display equipment for personal computer/work station, Frame memory for digital TV/VTR, Videotex, Teletext, Video printer, High Speed data transmission systems.

PIN DESCRIPTION

Pin	Name	Function
$\overline{RAS}$	ROW ADDRESS STROBE INPUT	It is used as a clock which latches the row address (A0-A7) and selects the word line. It also selects the write-per-bit, the data transfer and the $\overline{CAS}$-before-$\overline{RAS}$ refresh mode.
$\overline{CAS}$	COLUMN ADDRESS STROBE INPUT	It is used as a clock which latches the column address (A8-A15) and reads or writes the selected words. In the data transfer cycle, it becomes the SAM start address.
$A_0 \sim A_7$	ADDRESS INPUT	The M5M4C264L is an address multiplex method for inputting the row addresses and column addresses separately, in order to select one word from the 64K word memory cells. The various addresses are latched by the $\overline{RAS}$/$\overline{CAS}$ falling edge. In the data transfer cycle, this address input is also combined with the serial access start address.
$\overline{WB}/\overline{WE}$	WRITE-PER-BIT/ WRITE ENABLE INPUT	When the $\overline{WB}/\overline{WE}$ level in the $\overline{RAS}$ clock falling edge is "L", the write-per-bit or write transfer cycle is selected, and when it is "H", a 4 bit write to the $\overline{RAM}$ or a read transfer cycle from the $\overline{RAM}$ is selected.
$\overline{DT}/\overline{OE}$	DATA TRANSFER OUTPUT ENABLE INPUT	In the RAM read cycle, it makes the data output into enable. Also, when the $\overline{DT}/\overline{OE}$ level in the $\overline{RAS}$ clock falling edge is "L", the data transfer cycle is selected, and when it is "H", the read/write cycle is selected.
$W_0 \sim W_3$/ $IO_0 \sim IO_3$	WRITE-PER-BIT SELECTION INPUT/ DATA INPUT/OUTPUT	These are the data input/output pins to the RAM. During the write-per-bit cycle in the $\overline{RAS}$ clock falling edge, the "H" pin is enable and the selected bit-only-write is performed. Also, in the write cycle, the data in the late falling edge, whether it is $\overline{CAS}$ or $\overline{WE}$, is latched.
SC	SERIAL CONTROL INPUT	The serial access is started from the SC clock rising edge. In the serial read cycle the output data is held until the next clock rise. Also in the serial write cycle, the data is latched at the SC clock rising edge.
$SIO_0 \sim SIO_3$	SERIAL INPUT/ OUTPUT	256 x 4 word serial data input/output pins.
$\overline{SE}$	SERIAL ENABLE INPUT	This makes serial input/output into enable. In the $\overline{RAS}$ clock falling edge, when $\overline{SE}$ is "H", it is a pseudo transfer, and when it is "L". It is a write transfer.

NB: SAM: Serial Access Memory

FUNCTION

RAM Port Operation

The row/column addresses are specified by the $\overline{RAS}$/$\overline{CAS}$ clocks.

The RAM read/write cycle is set up by maintaining the $\overline{DT}/\overline{OE}$ at "H" level, while the $\overline{RAS}$ clock is falling. In addition, the column address is specified while the $\overline{RAS}$ clock is held at "L" level and goes into page mode when the $\overline{CAS}$ clock is activated, and then the column datas in one row can be read/written continually.

1. Random Read Cycle

Data is read out when $\overline{DT}/\overline{OE}$ is a "L" level.

2. Random Write Cycle

Data is written in when $\overline{WB}/\overline{WE}$ is a "L" level.

When the $\overline{WE}$ clock is input before the $\overline{CAS}$ clock, it becomes an early write cycle, and the data from the $\overline{CAS}$ clock falling, is written in the RAM.

When the $\overline{WE}$ clock is input after the $\overline{CAS}$ clock, it becomes a late write cycle and the data from the $\overline{WE}$ clock falling is written in the RAM.

The read-modify-write cycle modifies the data which has been read and writes it in again. This time also, the $\overline{OE}$, $\overline{WE}$ clock controls the reading/writing of data.

In this random write cycle, the write-per-bit function (Note 1) is available.

SAM Port Operation

At the falling edge of the $\overline{RAS}$ clock, the data transfer cycle is set up by maintaining the $\overline{DT}/\overline{OE}$ at "L" level. At such a time, the transfer cycle is the read transfer when the $\overline{WB}/\overline{WE}$ clock is "H" level, and the write transfer when it is "L" level.

In the transfer cycle, the row address sets up the RAM row and the column address becomes the serial access start address.

- $\overline{DT}/\overline{OE}$ signal can be used to select RAM or SAM independent mode (DT = "H") and between RAM and SAM data transfer mode (DT = "L").
- Within one transfer cycle, transfer of data (256 x 4 bits) is possible between any rows in the RAM and SAM.
- $\overline{WE}$ signal permits the designation of transfer direction. ($\overline{WE}$ = "H": RAM → SAM (read transfer)/$\overline{WE}$ = "L": SAM → RAM (write transfer))
- During read transfer, high-speed transfer execution is started at $\overline{DT}/\overline{OE}$ leading edge. (Note 2)
- Transfer cycle allows the selection of SAM I/O mode.
- In write transfer mode, $\overline{SE}$ control allows the transfer execution to be inhibited. (pseudo write transfer) (Note 3)
- ROW address in transfer cycle permits the transfer page of RAM.
- Column address in transfer cycle is specified the read (write) start address of SAM after transfer.

Memory Refresh Operation

The M5M4C264 consists of dynamic RAMs memory cells so a refresh operation is required every 4m seconds.

The refresh operation consists of reading the data from the memory, amplifying it in the sense amp and then rewriting it. With the M5M4C264, all the memory cells are refreshed by performing a refresh operation on all 256 row addresses which are designated by the 8 bits.

1. $\overline{RAS}$ Only Refresh

When the row address is input while the $\overline{CAS}$ clock is held at "H" level, and the $\overline{RAS}$ clock is activated, all the column data in the designated row address are refreshed simultaneously.

2. $\overline{CAS}$-Before-$\overline{RAS}$ Refresh

When the $\overline{CAS}$ clock is activated before the $\overline{RAS}$ clock, the designated row address, which is generated by the internal 8 bit refresh counter, is refreshed. The built-in refresh counter is incremented with every refresh cycle. Then all the memory cells are refreshed by repeating the $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle 256 times.

3. Hidden Refresh

The memory cells are refreshed by the 8 bit refresh counter built into the chip, in the same way as the $\overline{CAS}$-before-$\overline{RAS}$ refresh, by activating the RAS clock while the $\overline{CAS}$, $\overline{OE}$ clocks are being held at "L" level after the previous read cycle. At this time, the data which was read into the previous cycle is held in the output.

SAM READ OUT/WRITE IN

In the same way as a shift register, SAM inputs and outputs data simultaneously with the SC clock rise. SE is used to control the data inputs/outputs.

RAM and SAM are connected to each other by 1024 data buses, and the data from RAM can be transferred to SAM and the data from SAM can be transferred to RAM.

1. SERIAL READ TRANSFER CYCLE (RAM→SAM TRANSFER)

When the RAS clock is falling, the serial read transfer mode is selected and at the same time the row address indicates the row for transfer from RAM to SAM and the data are read out. When the column address is input and the DT signal is "H", the one row data read out from RAM is transferred to the data register. At the same time as this, the decoded column address is set to the serial selector and the serial read start address is determined. (pointer control) After this, every time the SC clock goes from "L" to "H", the data is output to the serial port and the selector moves onto the next bit. For the serial selector to be cyclic, when the SC clock is input more than 257 times, the same data from the start address mentioned above is output again. SE clock controls the serial output buffer. When SE is "L", the data register contents are output to the SIO pins and when SE is "H", the SIO pins are at high impedance. The serial selector has no relation with the SE level and shifts one bit every time the SC clock is input. Serial read transfer can be done when SAM is in operation and also, data from different rows can be continuously output. (real time transfer)

A horizontal scroll can easily be realized with the pointer control function which is utilized to indicate the arbitrary address.

The memory can be effectively used with the real time transfer function which is utilized to scan multiple lines horizontally.

2. SERIAL WRITE TRANSFER CYCLE (SAM→RAM TRANSFER)

When the RAS clock is falling, the serial write transfer mode is selected and at the same time the row transferred from SAM is designated by the row address, in the same way as for the serial read transfer mode. When the column address is input and the DT signal is turned "H", the single row data which are read out from SAM is written into the row selected by RAM. At the same time as this, the decoded row address is set to the serial selector and the next serial write start address is determined. After this, every time the SC clock is input, the data which are input to SIO are written into SAM. SE controls the serial input buffer. It writes into the data register when the level is "L", and when the level is "H", it only shifts the serial selector without writing in the data.

3. PSEUDO WRITE TRANSFER CYCLE

This is the same as the write transfer cycle, except for the fact that data is not transferred from SAM to RAM. (The row address which is input is ignored.)

When the mode changes from serial read to serial write, this cycle is used so that the RAM data is not destroyed, and also for changing the mode of the serial port.

Different to serial read transfer, serial write transfer and pseudo write transfer cycles cannot be done while SAM is operating, and it cannot input data continuously to different rows.

Note 1: Write-Per-Bit Function

During the RAM operation, data is written to the specified terminals of the four I/O common terminals, while being inhibited at the others.

Write-Per-Bit mode is specified by $\overline{WB}$ (="L") at $\overline{RAS}$ falling edge.

Write terminals are specified by W/IO (Write = "H", Write inhibit = "L") at this time. Actual writing is then carried out by $\overline{WE}$ in the same manner as with the conventional DRAM.

Note 2: Real-time Data Transfer

Read transfer (RAM → SAM) is executed with $\overline{DT}$ leading timing in transfer cycle. In the SC clock input before this timing, the SAM contents before transfer are output, while the new SAM contents after read transfer are output in the SC clock input after this timing.

During read transfer, continuous SC clock is also applied, thus making it possible to continuously produce SAM output before read transfer and SAM output after transfer.

Note 3: Pseudo Write Transfer

In order to write data to SAM when it has been in the output mode it is necessary to change the SAM I/O common terminals (SIO) to the input mode using the write transfer mode. If write transfer is not desired, the pseudo write transfer mode should be used.

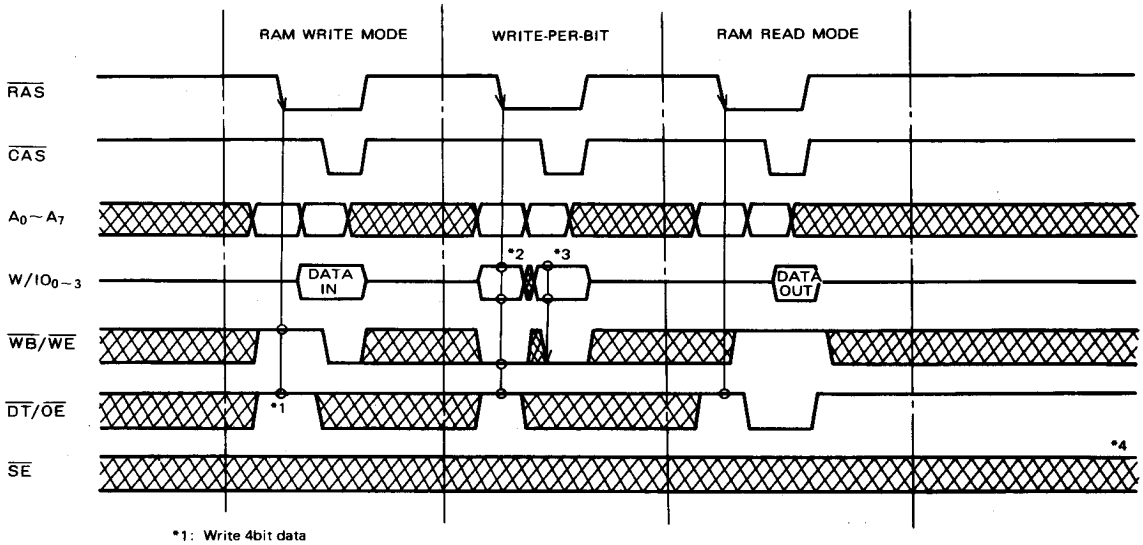
If $\overline{SE}$ is in "H" at $\overline{RAS}$ falling edge of write transfer mode is selected; thus, SAM I/O common terminals are set to the input mode, but SAM to RAM data transfer is not executed.

MODE SELECTION

Input pin state at $\overline{RAS}$ falling				RAM		SAM
$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	$\overline{SE}$	W/IO 0~3		Bit Mask	SIO 0~3
H	X	X	X	READ	—	—
	H			WRITE	—	—
	L	X	H	Write-Per-Bit	Non Masked	—
			L		Masked	
L	H	X	X	RAM→SAM (read transfer)	—	Output mode
	L	L	X	SAM→RAM (write transfer)	—	Input mode
		H	X	Pseudo Write Transfer (No RAM contents will be changed)	—	Input mode

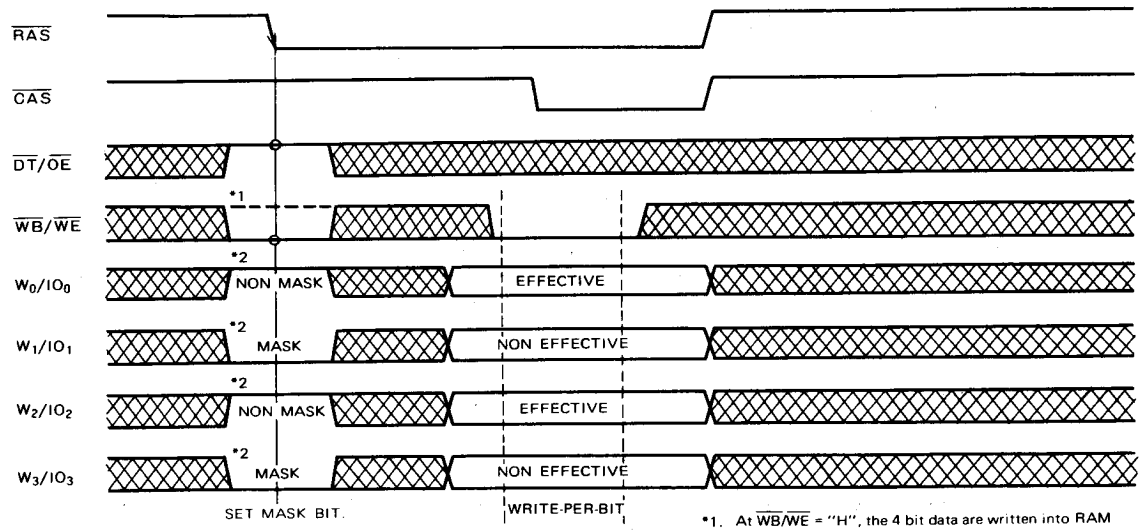
X: Not specified.

RAM Access Mode



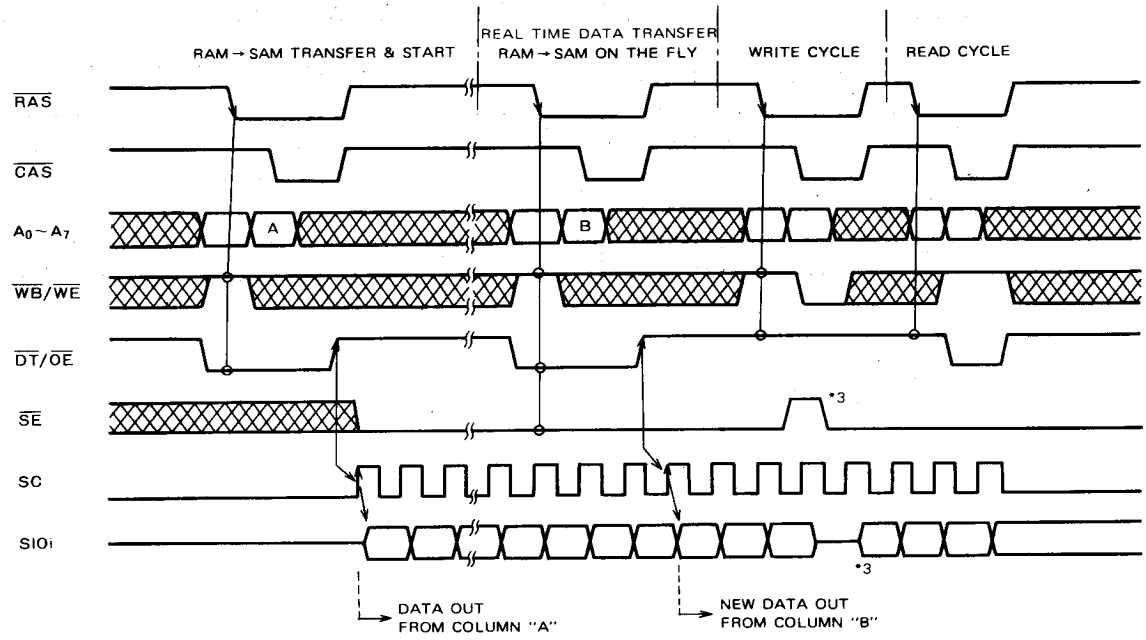
*1: Write 4bit data
*2: Set mask bit
*3: Write selected bit
*4: Indicates the don't care input

Write-Per-Bit Operation



*1. At WB/WE = "H", the 4 bit data are written into RAM
*2. W0~3/IO0~3 = "H": Non masked
W0~3/IO0~3 = "L": Masked

Serial Output Mode



*3. If SE goes "H" level, SIOi become into high impedance state, but serial data selector is continuously working.

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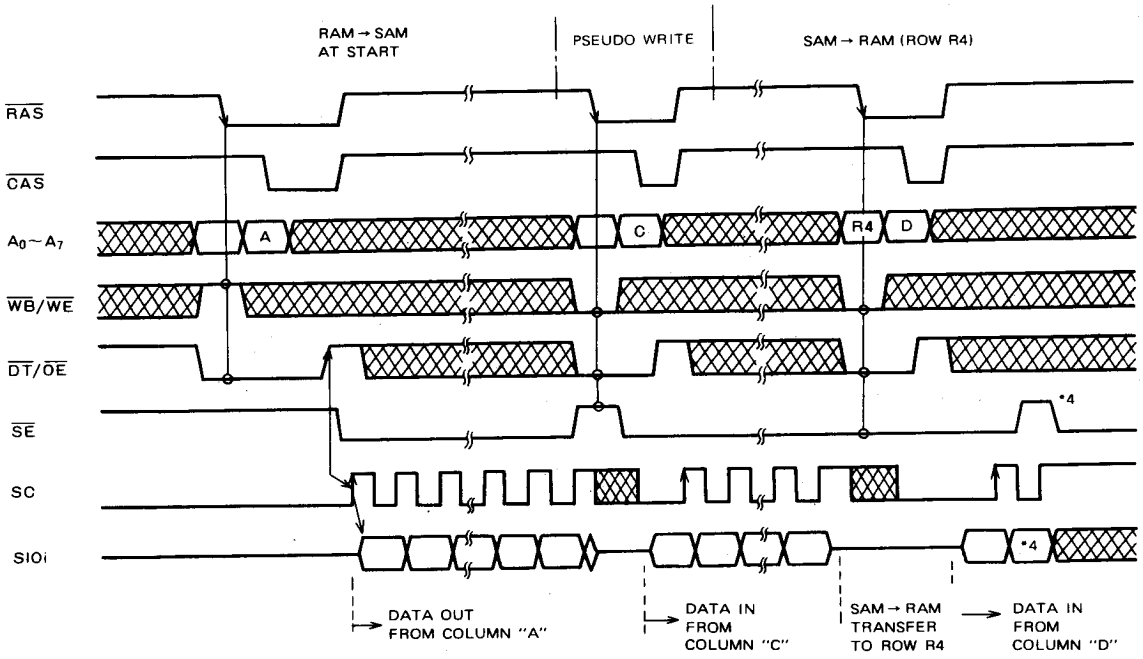
Serial Input Mode



*4. If $\overline{SE}$ goes "H" level, SIOi input data is ignored, but serial data selector is continuously working.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−1~7	V
V_I	Input voltage		−1~7	V
V_O	Output voltage		−1~7	V
I_O	Output current		50	mA
Pd	Power dissipation	Ta = 25°C	1000	mW
Topr	Operating temperature		0~70	°C
Tstg	Storage temperature		−65~150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = 0 ~ 70°C unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage all inputs	2.4		V_{CC}+1	V
V_{IL}	Low-level input voltage all inputs	−1		0.8	V

Note 1: All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OH} (R)	High-level output voltage (RAM Port)	I_{OH} (R) = −2mA	2.4		V_{CC}	V
V_{OL} (R)	Low-level output voltage (RAM Port)	I_{OL} (R) = 4.2mA	0		0.4	V
V_{OH} (S)	High-level output voltage (Serial I/O Port)	I_{OH} (S) = −2mA	2.4		V_{CC}	V
V_{OL} (S)	Low-level output voltage (Serial I/O Port)	I_{OL} (S) = 4.2mA	0		0.4	V
I_{OZ}	Off-state output current	Q floating 0V ≦ V_{OUT} ≦ 5.5V	−10		10	μA
I_I	Input current	0V ≦ V_{IN} ≦ V_{CC} Other input pins = 0V	−10		10	μA

Note 2: Current flowing into an IC is positive, out is negative

Symbol	Parameter		Limits			Unit
			-10	-12	-15	
(Note 3)	RAM Port	Serial I/O Port	Max	Max	Max	
I_{CC1} (AV)	Random R/W cycle ($\overline{RAS}$/$\overline{CAS}$ cycling, t_{RC} = t_{RC} (min))	Standby (SC = V_{IL})	70	60	50	mA
I_{CC2}	Standby ($\overline{RAS}$ = V_{IH}, Dout = H_{IZ}) (Note 4)	Standby (SC = V_{IL}) (Note 4)	5	5	5	mA
I_{CC3} (AV)	RAS only refresh cycle ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} (min))	Standby (SC = V_{IL})	60	50	40	mA
I_{CC4} (AV)	Page mode cycle ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = t_{PC} (min))	Standby (SC = V_{IL})	50	40	35	mA
I_{CC5} (AV)	CAS before RAS refresh ($\overline{CAS}$ low as $\overline{RAS}$ falls, t_{RC} = t_{RC} (min))	Standby (SC = V_{IL})	60	50	40	mA
I_{CC6} (AV)	Data transfer cycle ($\overline{DT}$ low as $\overline{RAS}$ falls, t_{RC} = t_{RC} (min))	Standby (SC = V_{IL})	75	65	55	mA
I_{CC7} (AV)	Random R/W cycle ($\overline{RAS}$/$\overline{CAS}$ cycling, t_{RC} = t_{RC} (min))	Active (t_{SCC} = t_{SCC} (min.))	115	100	80	mA
I_{CC8} (AV)	Standby ($\overline{RAS}$ = V_{IH}, Dout = H_{IZ} (min))	Active (t_{SCC} = t_{SCC} (min.))	45	40	30	mA
I_{CC9} (AV)	RAS only refresh cycle ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} (min))	Active (t_{SCC} = t_{SCC} (min.))	105	90	70	mA
I_{CC10} (AV)	Page mode cycle ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{RC} = t_{RC} (min))	Active (t_{SCC} = t_{SCC} (min.))	95	80	65	mA
I_{CC11} (AV)	CAS before RAS refresh ($\overline{CAS}$ low as $\overline{RAS}$ falls, t_{RC} = t_{RC} (min))	Active (t_{SCC} = t_{SCC} (min.))	105	90	70	mA
I_{CC12} (AV)	Data transfer cycle ($\overline{DT}$ low as $\overline{RAS}$ falls, t_{RC} = t_{RC} (min))	Active (t_{SCC} = t_{SCC} (min.))	120	105	85	mA

Note 3: I_{CC} (AV) is obtained with the output open. (AV) specifies average value.
4: If V_{IH} ≧ V_{CC} × 0.9 and V_{IL} ≦ 0.6V, then I_{CC2} ≦ 1.5 mA. ($\overline{CAS}$, $\overline{SE}$ and SIO_0 ~ SIO_3 must be stable in high or low level.)

CAPACITANCE (T_a = 25°C, f = 1MHz, V_I = 25mVmrs)

Symbol	Parameter	Min	Max	Unit
C_{IN0}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WB}$/$\overline{WE}$, SC, $\overline{SE}$, $\overline{DT}$/$\overline{OE}$		8	pF
C_{IN1}	A_0~A_7		5	pF
C_{IO0}	W_0/IO_0~ W_3/IO_3, SIO_0~SIO_3		7	pF

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SWITCHING CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Note 5)

Symbol	Parameter		Alternative Symbol	Limits						Unit
				M5M4C264-10		M5M4C264-12		M5M4C264-15		
				Min	Max	Min	Max	Min	Max	
$t_{a(C)}$	Access time from $\overline{CAS}$	(Note 6,8)	t_{CAC}		50		60		75	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	(Note 6,9)	t_{RAC}		100		120		150	ns
$t_{a(OE)}$	Access time from $\overline{OE}$	(Note 6)	t_{OEA}		30		35		40	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	(Note 10)	t_{OFF}	0	25	0	30	0	40	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high	(Note 10)	t_{OEZ}	0	25	0	30	0	40	ns
$t_{a(SC)}$	Access time from SC high	(Note 7)	t_{SCA}		35		40		50	ns
$t_{a(SE)}$	Access time from $\overline{SE}$ low	(Note 7)	t_{SOA}		30		35		50	ns
$t_{dis(SE)}$	Output disable time after $\overline{SE}$ high	(Note 10)	t_{SOZ}	0	25	0	30	0	40	ns
$t_{h(SCHD)}$	Serial output hold time after SC high	(Note 7)	t_{SOH}	10		10		10		ns
t_{SOLD}	Delay time, $\overline{SE}$ low to serial setup	(Note 7)	t_{SOO}	5		5		5		ns

Note 5: An initial pause of 500μs is required after power-up followed by any 8 $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles before proper device operation is achieved.
Note that $\overline{RAS}$ may be cycled during the initial pause.
And any 8 $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles are required after prolonged periods (greater than 4ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
6: Measured with a load circuit equivalent to 2TTL loads and 100pF.
7: Measured with a load circuit equivalent to 2TTL loads and 50pF.
8: Assume that $t_{RLCL} \geq t_{RLCL}$ max.
9: Assume that $t_{RLCL} < t_{RLCL}$ max. When t_{RLCL} is greater than t_{RLCL} max., $t_{a(R)}$ will increase by the amount that t_{RLCL} exceeds t_{RLCL} max.
10: $t_{dis(CH)}$ max and $t_{dis(OE)}$ max define the time at which the output achieves the high impedance state ($I_{OUT} \leqq |\pm 10\mu A|$) and are not reference to V_{OH} min or V_{OL} max.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Page-Mode Cycles)

(T_a=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted, See notes 11)

Symbol	Parameter		Alternative Symbol	Limits						Unit
				M5M4C264-10		M5M4C264-12		M5M4C264-15		
				Min	Max	Min	Max	Min	Max	
$t_{C(RF)}$	Refresh cycle time		t_{REF}		4		4		4	ms
$t_{W(RH)}$	$\overline{RAS}$ high pulse width		t_{RP}	80		90		100		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 12)	t_{RCD}	25	50	25	60	30	75	ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	(Note 13)	t_{CRP}	10		10		10		ns
$t_{su(RA)}$	Row address setup time before $\overline{RAS}$ low		t_{ASR}	0		0		0		ns
$t_{su(CA)}$	Column address setup time before $\overline{CAS}$ low		t_{ASC}	0		0		0		ns
$t_{h(RA)}$	Row address hold time after $\overline{RAS}$ low		t_{RAH}	15		15		20		ns
$t_{h(CLCA)}$	Column address hold time after $\overline{CAS}$ low		t_{CAH}	20		20		25		ns
$t_{h(RLCA)}$	Column address hold time after $\overline{RAS}$ low		t_{AR}	70		80		100		ns
t_T	Transition time (rise and fall)	(Note 14)	t_T	3	50	3	50	3	50	ns
$t_{su(WPB)}$	Write per bit mode setup time before $\overline{RAS}$ low		t_{WBS}	0		0		0		ns
$t_{h(WPB)}$	Write per bit mode hold time after $\overline{RAS}$ low		t_{WBH}	20		20		25		ns
$t_{su(W)}$	Write mask setup time before $\overline{RAS}$ low		t_{WS}	0		0		0		ns
$t_{h(W)}$	Write mask hold time after $\overline{RAS}$ low		t_{WH}	20		20		25		ns
$t_{su(DTH)}$	$\overline{DT}$ high setup time before $\overline{RAS}$ low		t_{DHS}	0		0		0		ns
$t_{h(DTH)}$	$\overline{DT}$ high hold time after $\overline{RAS}$ low		t_{DHH}	20		20		25		ns

Note 11: The timing requirements assume t_T=5ns.
V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals.
12: t_{RLCL} max is specified as a reference point only; When t_{RLCL} is less than t_{RLCL} max, access time is $t_{a(R)}$. When t_{RLCL} is greater than t_{RLCL} max, access time is $t_{RLCL} + t_{a(C)}$. t_{RLCL} min is specified as t_{RLCL} min. = $t_{h(RA)} + 2t_T + t_{su(CA)}$.
13: t_{CHRL} requirement is only applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by a $\overline{CAS}$ only cycle (i.e., For systems where $\overline{CAS}$ has not been decoded with $\overline{RAS}$).
14: t_T is measured between V_{IH} min and V_{IL} max.

For Read and Refresh Cycles

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4C264-10		M5M4C264-12		M5M4C264-15		
			Min	Max	Min	Max	Min	Max	
$t_{c(rd)}$	Read cycle time	t_{RC}	200		220		260		ns
$t_{w(RL)}$	$\overline{RAS}$ low pulse width	t_{RAS}	100	10000	120	10000	150	10000	ns
$t_{w(CL)}$	$\overline{CAS}$ low pulse width	t_{CAS}	50	10000	60	10000	75	10000	ns
$t_{w(CH)}$	$\overline{CAS}$ high pulse width	t_{CPN}	25		25		30		ns
$t_{h(RLCH)}$	$\overline{CAS}$ hold time after $\overline{RAS}$ low	t_{CSH}	100		120		150		ns
$t_{h(CLRH)}$	$\overline{RAS}$ hold time after $\overline{CAS}$ low	t_{RSH}	50		60		75		ns
$t_{su(rd)}$	Read setup time before $\overline{CAS}$ low	t_{RCS}	0		0		0		ns
$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ high (Note 15)	t_{RCH}	0		0		0		ns
$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ high (Note 15)	t_{RRH}	20		20		20		ns
$t_{h(OECH)}$	$\overline{CAS}$ hold time after $\overline{OE}$ low	—	25		30		40		ns
$t_{h(OERH)}$	$\overline{RAS}$ hold time after $\overline{OE}$ low	t_{OES}	25		30		40		ns
$t_{h(CLOE)}$	$\overline{OE}$ hold time after $\overline{CAS}$ low	t_{COH}	50		60		75		ns
$t_{h(RLOE)}$	$\overline{OE}$ hold time after $\overline{RAS}$ low	—	100		120		150		ns
t_{DOEL}	Delay time, Data to $\overline{OE}$ low	—	0		0		0		ns
t_{OEHD}	Delay time, $\overline{OE}$ high to Data	t_{OED}	25		35		40		ns
t_{RHCL}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	t_{RPC}	0		0		0		ns
t_{DCL}	Delay time, Data to $\overline{CAS}$ low	t_{DZC}		0		0		0	ns

Note 15: Either $t_{h(CHrd)}$ or $t_{h(RHrd)}$ must be satisfied for a read cycle.

For Write Cycles (Early Write and Delayed Write)

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4C264-10		M5M4C264-12		M5M4C264-15		
			Min	Max	Min	Max	Min	Max	
$t_{c(w)}$	Write cycle time	t_{RC}	200		220		260		ns
$t_{w(RL)}$	$\overline{RAS}$ low pulse width	t_{RAS}	100	10000	120	10000	150	10000	ns
$t_{w(CL)}$	$\overline{CAS}$ low pulse width	t_{CAS}	50	10000	60	10000	75	10000	ns
$t_{w(CH)}$	$\overline{CAS}$ high pulse width	t_{CPN}	25		25		30		ns
$t_{h(RLCH)}$	$\overline{CAS}$ hold time after $\overline{RAS}$ low	t_{CSH}	100		120		150		ns
$t_{h(CLRH)}$	$\overline{RAS}$ hold time after $\overline{CAS}$ low	t_{RSH}	50		60		75		ns
$t_{su(WCL)}$	Write setup time before $\overline{CAS}$ low (Note 16)	t_{WCS}	0		0		0		ns
$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low	t_{WCH}	35		35		45		ns
$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low	t_{WCR}	85		95		120		ns
$t_{h(WCH)}$	$\overline{CAS}$ hold time after $\overline{WE}$ low	t_{CWL}	35		40		45		ns
$t_{h(WRH)}$	$\overline{RAS}$ hold time after $\overline{WE}$ low	t_{RWL}	35		40		45		ns
$t_{w(W)}$	Write pulse width	t_{WP}	35		35		45		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		0		ns
$t_{h(WLD)}$	Data hold time after $\overline{WE}$ low	t_{DH}	35		35		45		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	35		35		45		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	85		95		120		ns
t_{OEHD}	Delay time, $\overline{OE}$ high to Data	t_{OED}	35		35		40		ns
$t_{h(WOE)}$	$\overline{OE}$ hold time after $\overline{WE}$ low	t_{OEH}	30		30		40		ns

Note 16: When $t_{su(WCL)} \geqq t_{su(WCL)}$ min, the cycle is an early write cycle and I/O pins will remain high impedance throughout the entire cycle.
When $t_{CLWL} = t_{CLWL}$ min, and $t_{RLWL} \geqq t_{RLWL}$ min, the cycle is a read-write cycle, and the data of the selected address will be read out on I/O pins. For all conditions other than those described above, the condition of data outputs (at access time and until $\overline{CAS}$ or $\overline{DT}/\overline{OE}$ goes back to V_{IH}) is not defined.

For Read-Modify-Write Cycles

Symbol	Parameter		Alternative Symbol	Limits						Unit
				M5M4C264-10		M5M4C264-12		M5M4C264-15		
				Min	Max	Min	Max	Min	Max	
$t_{C(rdW)}$	Read modify write cycle time	(Note 17)	t_{RWC}	270		295		345		ns
$t_{W(RL)}$	$\overline{RAS}$ low pulse width		t_{RAS}	170	10000	195	10000	235	10000	ns
$t_{W(CL)}$	$\overline{CAS}$ low pulse width		t_{CAS}	120	10000	135	10000	160	10000	ns
$t_{h(RLCH)}$	$\overline{CAS}$ hold time after $\overline{RAS}$ low		t_{CSH}	170		195		235		ns
$t_{h(CLRH)}$	$\overline{RAS}$ hold time after $\overline{CAS}$ low		t_{RSH}	120		135		160		ns
$t_{W(CH)}$	$\overline{CAS}$ high pulse width		t_{CPN}	25		25		30		ns
$t_{su(rd)}$	Read setup time before $\overline{CAS}$ low		t_{RCS}	0		0		0		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{WE}$ low	(Note 16)	t_{CWD}	80		90		110		ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{WE}$ low	(Note 16)	t_{RWD}	130		150		185		ns
$t_{h(WCH)}$	$\overline{CAS}$ hold time after $\overline{WE}$ low		t_{CWL}	35		40		45		ns
$t_{h(WRH)}$	$\overline{RAS}$ hold time after $\overline{WE}$ low		t_{RWL}	35		40		45		ns
$t_{W(W)}$	Write pulse width		t_{WP}	35		35		45		ns
$t_{su(D)}$	Data setup time		t_{DS}	0		0		0		ns
$t_{h(WLD)}$	Data hold time after $\overline{WE}$ low		t_{DH}	35		35		45		ns
$t_{h(CLOE)}$	$\overline{OE}$ hold time after $\overline{CAS}$ low		t_{COH}	50		60		75		ns
$t_{h(RLOE)}$	$\overline{OE}$ hold time after $\overline{RAS}$ low		—	100		120		150		ns
t_{DOEL}	Delay time, Data to $\overline{OE}$ low		—	0		0		0		ns
t_{OEHD}	Delay time, $\overline{OE}$ high to Data		t_{OED}	35		35		40		ns

Note 17: $t_{C(rdW)}$ is specified as $t_{C(rdW)}\text{-min} = t_{a(R)}\ \text{max} + t_{OEHD}\ \text{min} + t_{h(WRH)}\ \text{min} + t_{W(RH)}\ \text{min} + 4\ t_T$.

For Page-Mode Cycle (Note 18)

Symbol	Parameter		Alternative Symbol	Limits						Unit
				M5M4C264-10		M5M4C264-12		M5M4C264-15		
				Min	Max	Min	Max	Min	Max	
$t_{C(Prd)}$	Read cycle time		t_{PC}	100		120		145		ns
$t_{C(PW)}$	Write cycle time		t_{PC}	100		120		145		ns
$t_{W(RL)}$	$\overline{RAS}$ low pulse width	(Note 19)	t_{RAS}	200	30000	240	30000	295	30000	ns
$t_{C(PrdW)}$	Read modify write cycle time		t_{RWC}	170		195		250		ns
$t_{W(RL)}$	$\overline{RAS}$ low pulse width	(Note 20)	t_{RAS}	340	30000	390	30000	505	30000	ns
$t_{W(CH)}$	$\overline{CAS}$ high pulse width		t_{CP}	40		50		60		ns

Note 18 All previously specified timing requirements and switching characteristics are applicable to their respective page mode timing.
19 Specified for read or write cycle.
20 Specified for read-modify-write cycle.

For $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 21)

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4C264-10		M5M4C264-12		M5M4C264-15		
			Min	Max	Min	Max	Min	Max	
$t_{suR(CR)}$	$\overline{CAS}$ setup time for auto refresh	t_{CSR}	10		10		10		ns
$t_{hR(RC)}$	$\overline{CAS}$ hold time for auto refresh	t_{CHR}	20		25		30		ns
$t_{dR(RC)}$	Precharge to $\overline{CAS}$ active time	t_{RPC}	0		0		0		ns

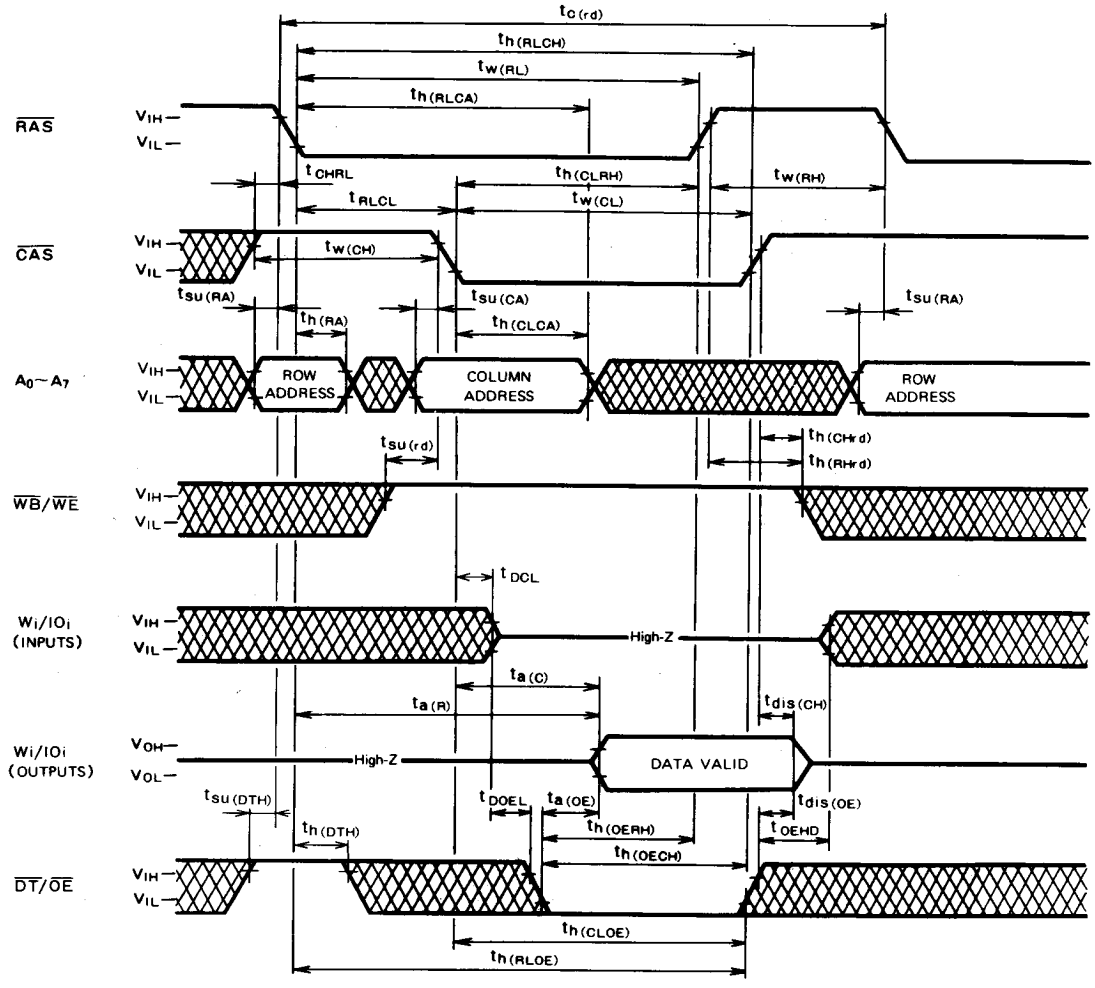
Note 21: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles is necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

For Read/Write/Pseudo Write Transfer and Serial Read/Write Cycle

Symbol	Parameter	Alternate Symbol	Limits						Unit
			M5M4C264-10		M5M4C264-12		M5M4C264-15		
			Min	Max	Min	Max	Min	Max	
$t_{C(rd)}$	Read cycle time	t_{RC}	200		220		260		ns
$t_{C(W)}$	Write cycle time	t_{RC}	200		220		260		ns
$t_{C(SC)}$	SC clock cycle time	t_{SCC}	35	50000	40	50000	60	50000	ns
$t_{W(RL)}$	$\overline{RAS}$ low pulse width	t_{RAS}	100	10000	120	10000	150	10000	ns
$t_{W(CL)}$	$\overline{CAS}$ low pulse width	t_{CAS}	50	10000	60	10000	75	10000	ns
$t_{W(RH)}$	$\overline{RAS}$ high pulse width	t_{RP}	80		90		100		ns
$t_{W(CH)}$	$\overline{CAS}$ high pulse width	t_{CPN}	25		25		30		ns
$t_{W(SCL)}$	SC low pulse width	t_{SCL}	10		10		20		ns
$t_{W(SCH)}$	SC high pulse width	t_{SCH}	10		10		20		ns
$t_{W(SEL)}$	$\overline{SE}$ low pulse width	t_{SOE}	10		10		20		ns
$t_{W(SEH)}$	$\overline{SE}$ high pulse width	t_{SOP}	10		10		20		ns
$t_{h(RLCH)}$	$\overline{CAS}$ hold time after $\overline{RAS}$ low	t_{CSH}	100		120		150		ns
$t_{h(CLRH)}$	$\overline{RAS}$ hold time after $\overline{CAS}$ low	t_{RSH}	50		60		75		ns
$t_{h(RLCA)}$	Column address hold time after $\overline{RAS}$ low	t_{AR}	70		80		100		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low (Note 13)	t_{CRP}	10		10		10		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (Note 12)	t_{RCD}	25	50	25	60	30	75	ns
$t_{su(RA)}$	Row address setup time before $\overline{RAS}$ low	t_{ASR}	0		0		0		ns
$t_{h(RA)}$	Row address hold time after $\overline{RAS}$ low	t_{RAH}	15		15		20		ns
$t_{su(CA)}$	Column address setup time before $\overline{CAS}$ low	t_{ASC}	0		0		0		ns
$t_{h(CLCA)}$	Column address hold time after $\overline{CAS}$ low	t_{CAH}	20		20		25		ns
$t_{su(WE)}$	$\overline{WE}$ setup time before $\overline{RAS}$ low	t_{WTS}	0		0		0		ns
$t_{h(WE)}$	$\overline{WE}$ hold time after $\overline{RAS}$ low	t_{WTH}	20		20		25		ns
$t_{su(DT)}$	$\overline{DT}$ setup time before $\overline{RAS}$ low	t_{DLS}	0		0		0		ns
$t_{h(DT)}$	$\overline{DT}$ hold time after $\overline{RAS}$ low	t_{RDH}	80		90		130		ns
$t_{h(CLDT)}$	$\overline{DT}$ low hold time after $\overline{CAS}$ low	t_{CDH}	30		40		55		ns
$t_{su(DTRH)}$	$\overline{DT}$ high setup time before $\overline{RAS}$ high	t_{DTR}	10		10		10		ns
$t_{h(DTRH)}$	$\overline{DT}$ high hold time after $\overline{RAS}$ high	t_{DTH}	20		20		25		ns
$t_{su(DTCH)}$	$\overline{DT}$ high setup time before $\overline{CAS}$ high	t_{DTC}	10		10		10		ns
$t_{su(SE)}$	$\overline{SE}$ setup time before $\overline{RAS}$ low	t_{ES}	0		0		0		ns
$t_{h(SE)}$	$\overline{SE}$ hold time after $\overline{RAS}$ low	t_{EH}	15		15		20		ns
$t_{su(SCDT)}$	SC low set up time before $\overline{DT}$ high	—	10		10		10		ns
$t_{h(DTSC)}$	SC high hold time after $\overline{DT}$ high	—		80		90		100	ns
$t_{h(SCDT)}$	SC low hold time after $\overline{DT}$ high	t_{SDH}	10		10		20		ns
$t_{su(SD)}$	Serial input data setup time before SC high	t_{SIS}	0		0		0		ns
$t_{h(SD)}$	Serial input data hold time after SC high	t_{SIH}	10		10		15		ns
t_{SHDH}	Delay time, SC high to $\overline{DT}$ high	t_{SDD}	20		20		25		ns
$t_{su(SCRL)}$	SC setup time before $\overline{RAS}$ low	t_{SRS}	20		20		30		ns
$t_{su(SEH)}$	$\overline{SE}$ disable setup time before SC high	t_{SWIS}	10		10		15		ns
$t_{h(SEH)}$	$\overline{SE}$ disable hold time after SC high	t_{SWIH}	20		20		30		ns
$t_{su(SEL)}$	$\overline{SE}$ enable setup time before SC high	t_{SWS}	10		10		15		ns
$t_{h(SEL)}$	$\overline{SE}$ enable hold time after SC high	t_{SWH}	20		20		30		ns
t_{DDTH}	Delay time, Data to $\overline{DT}$ high	t_{SZS}		0		0		0	ns
t_{DTHD}	Delay time, $\overline{DT}$ high to Data	—	20		20		30		ns

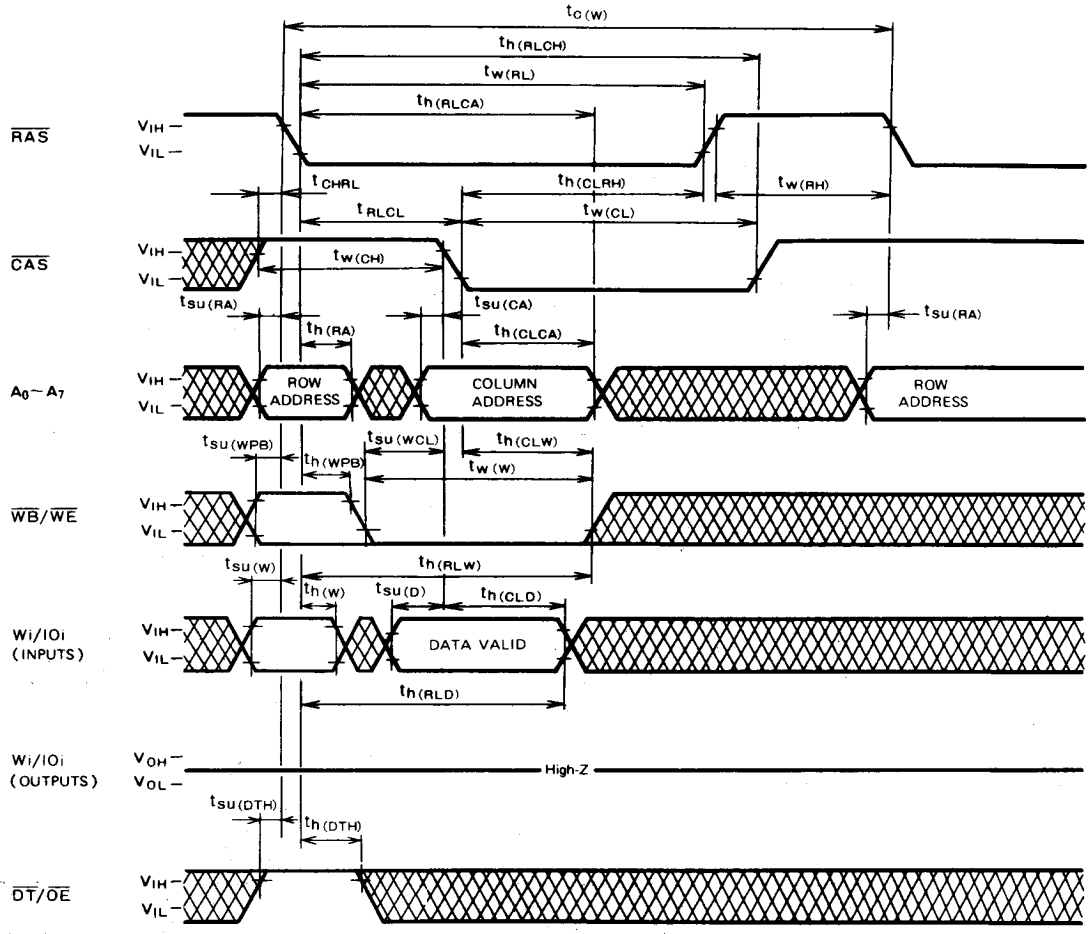
TIMING DIAGRAMS (Note 22)

Read Cycle

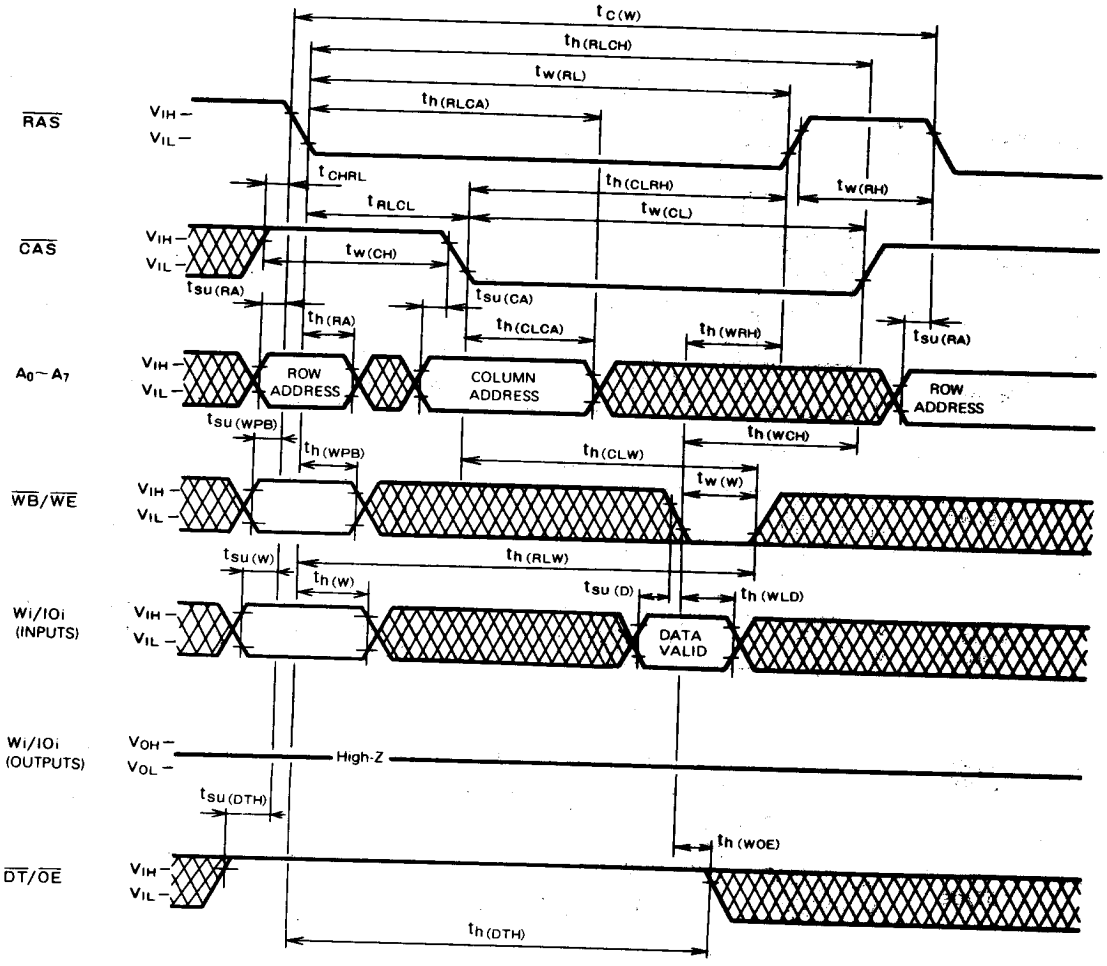


Note 22.  Indicates the don't care input.

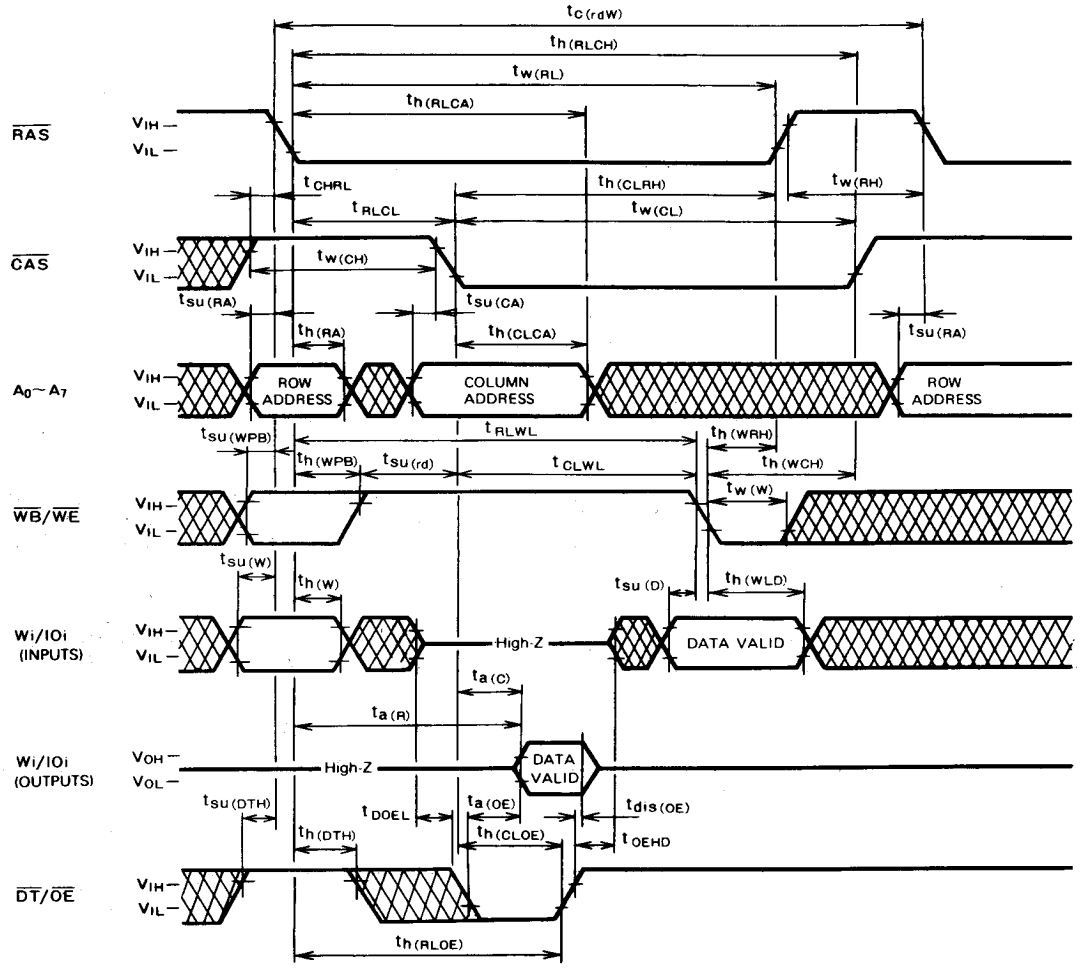
Write Cycle (Early Write)



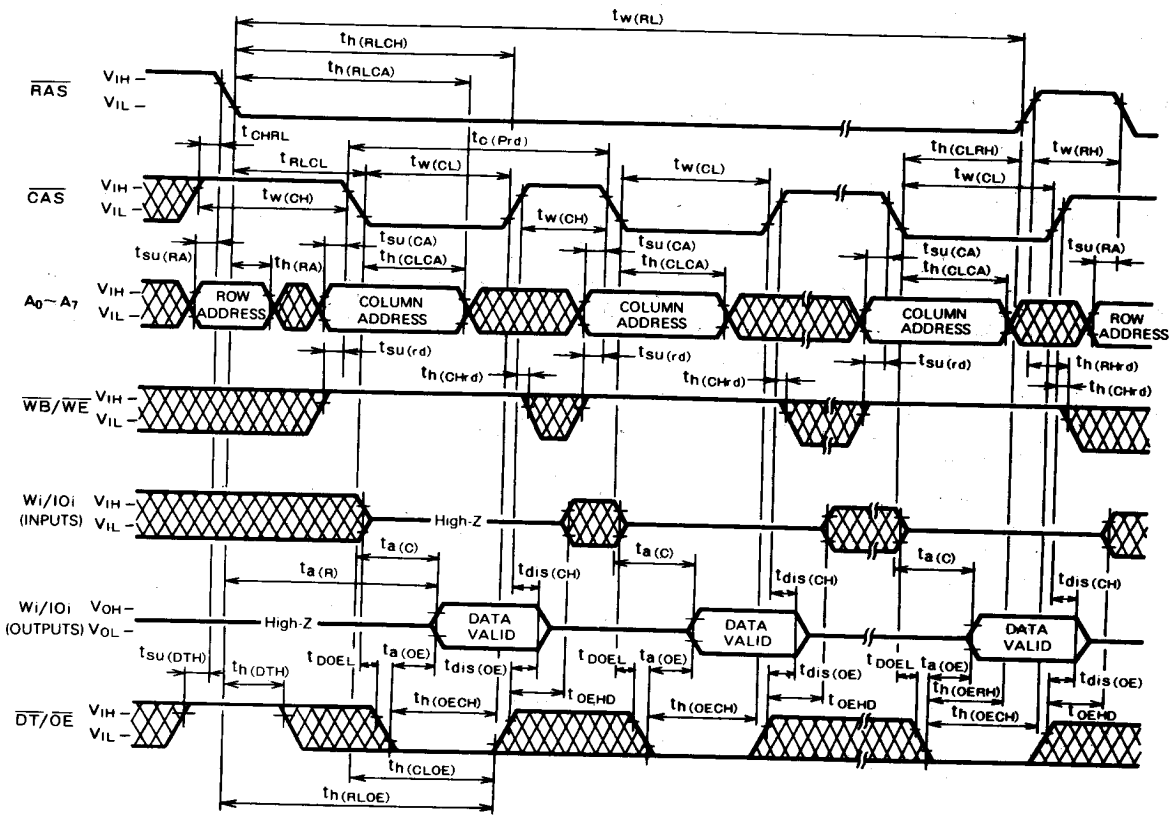
Write Cycle (Delayed Write)



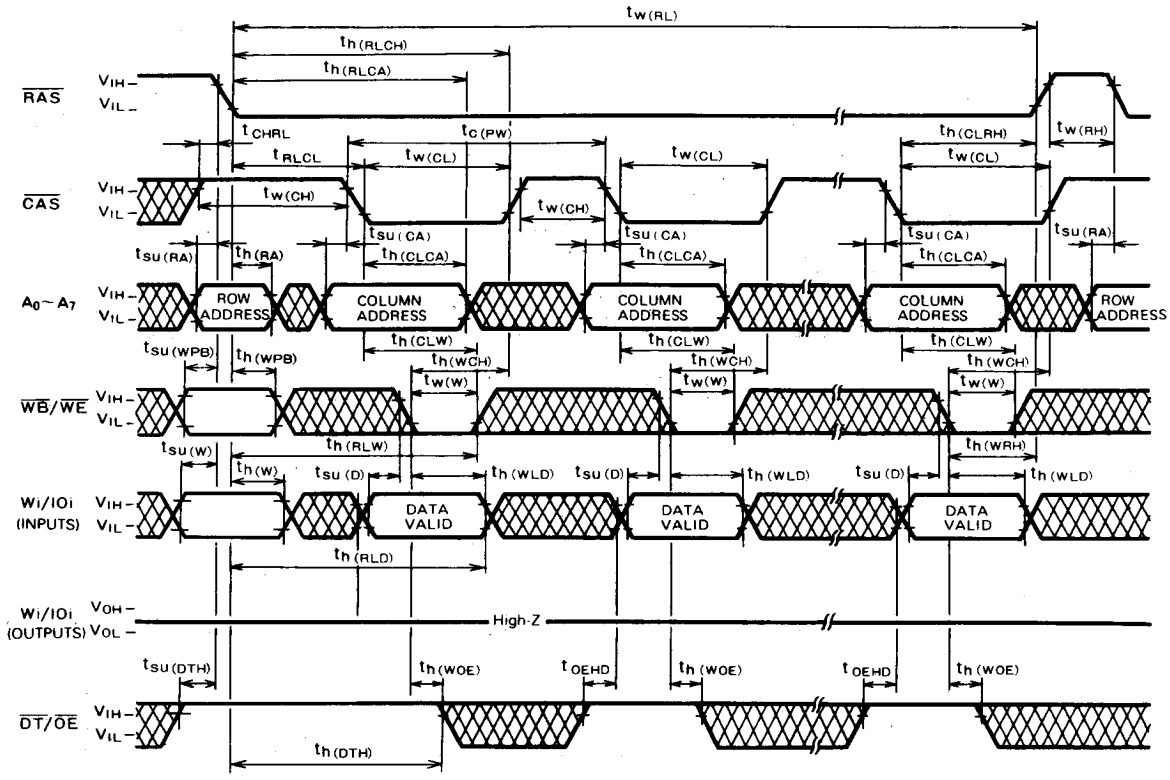
Read-Modify-Write Cycles



Page-Mode Read Cycle



Page-Mode Write Cycle



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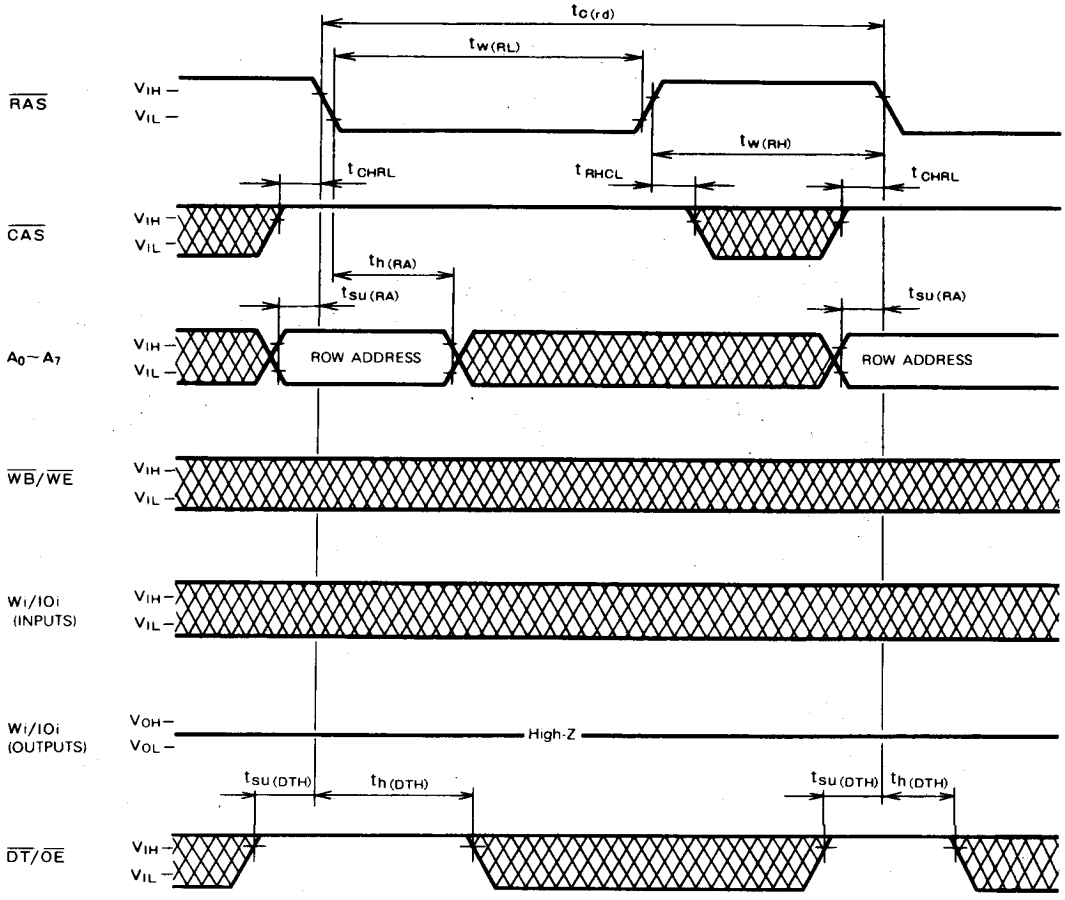
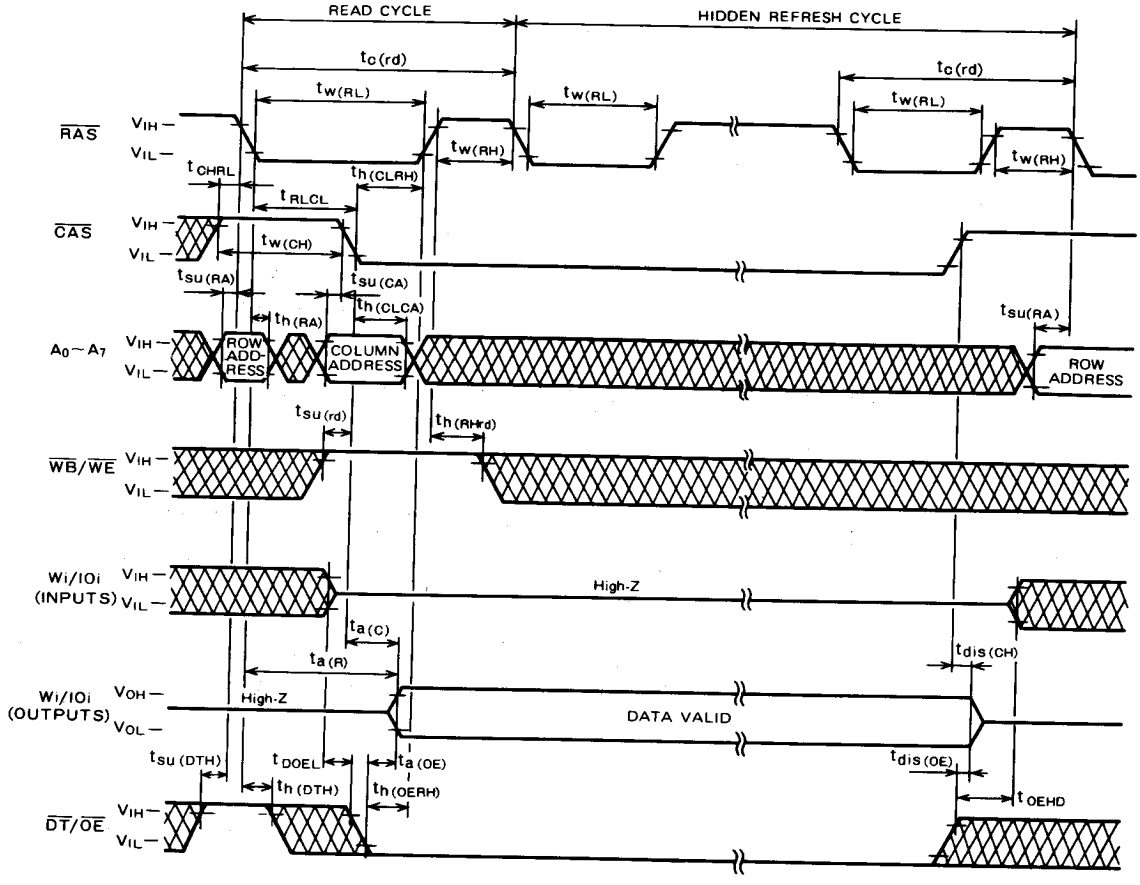
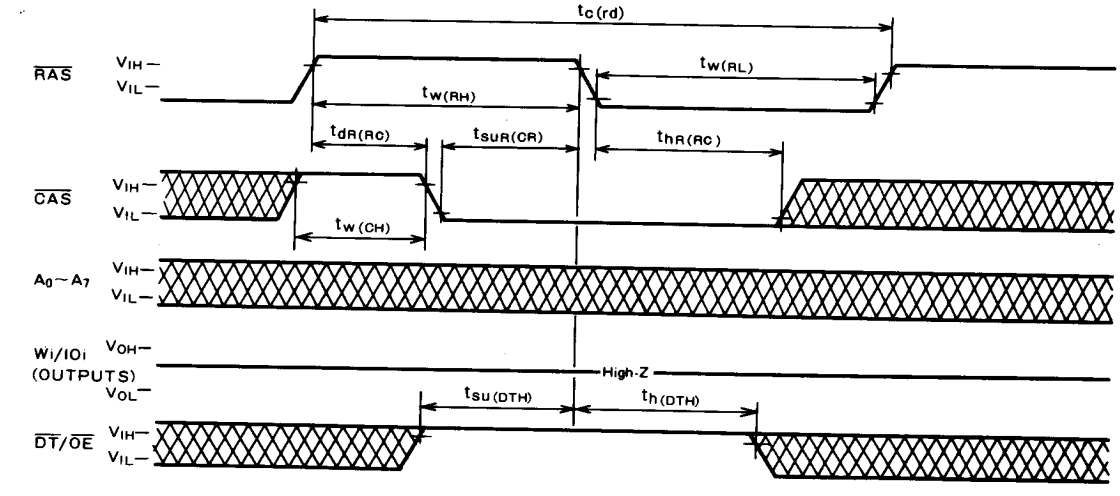
$\overline{RAS}$-Only Refresh Cycle



Hidden Refresh Cycle

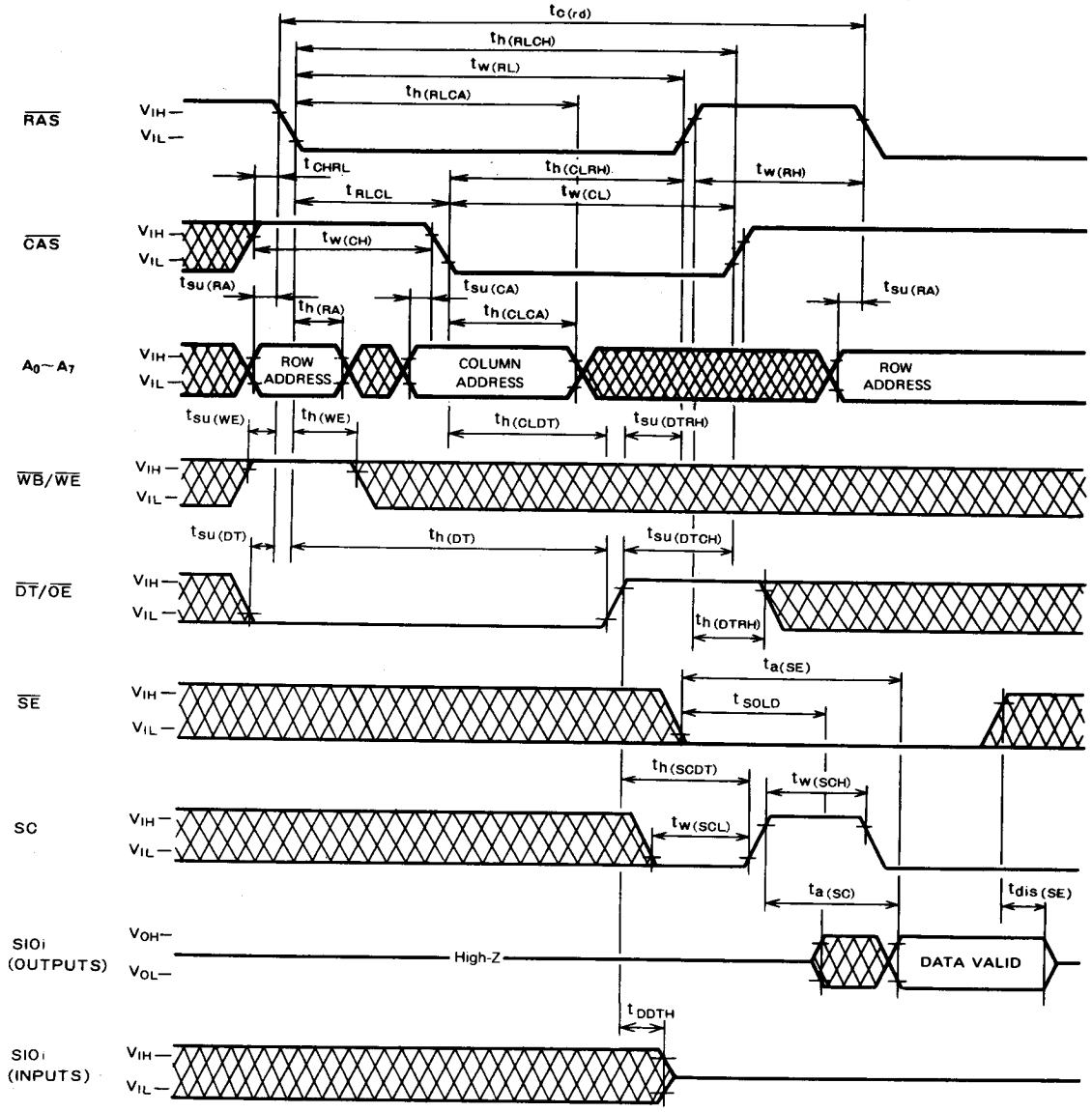


CAS before RAS Refresh Cycle

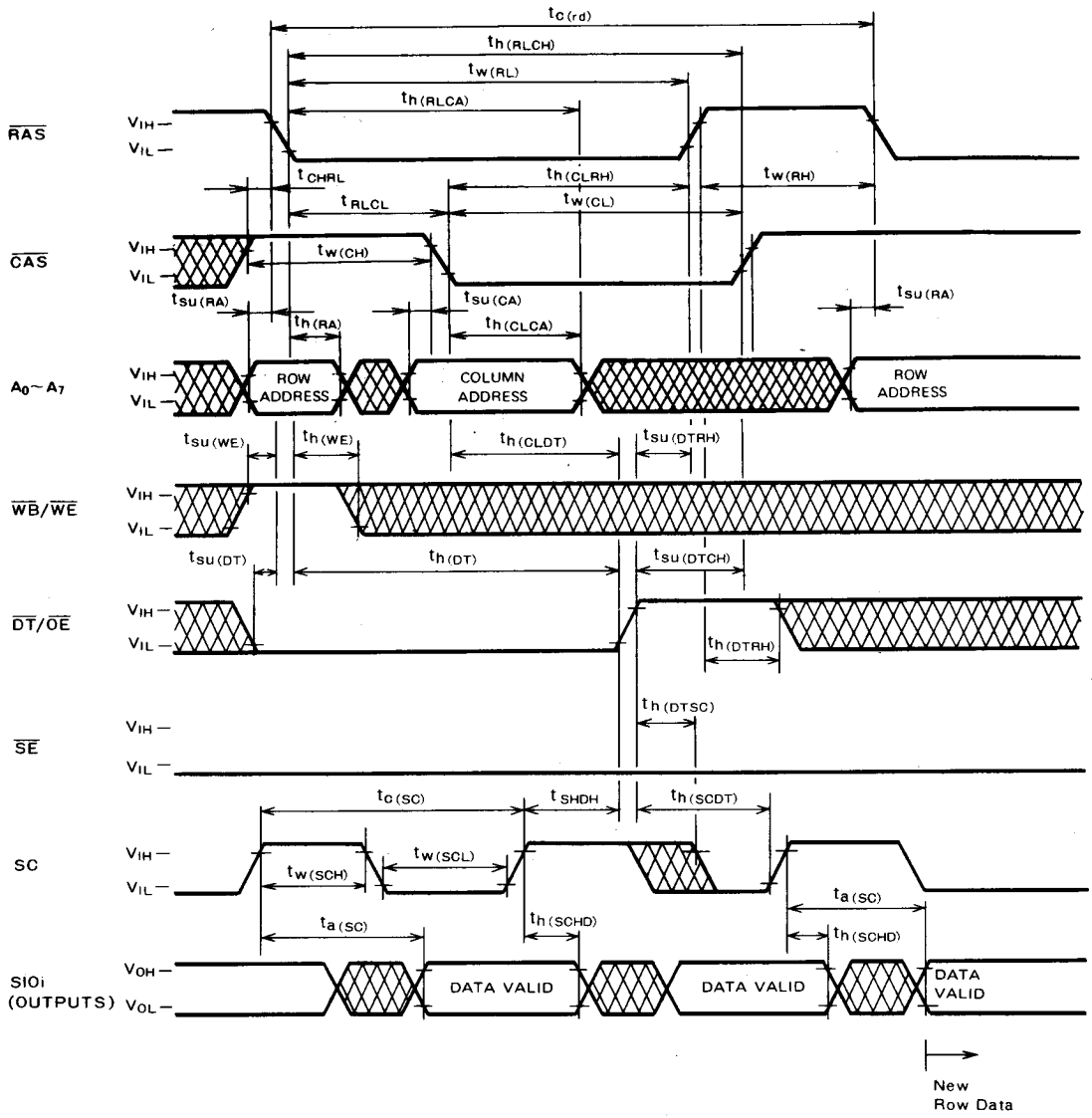


MITSUBISHI ELECTRIC

Read Transfer Cycle (B-port standby) Serial Read Setup (RAM → SAM)



Read Transfer Cycle (B-port Active) Serial Read Setup (RAM → SAM)



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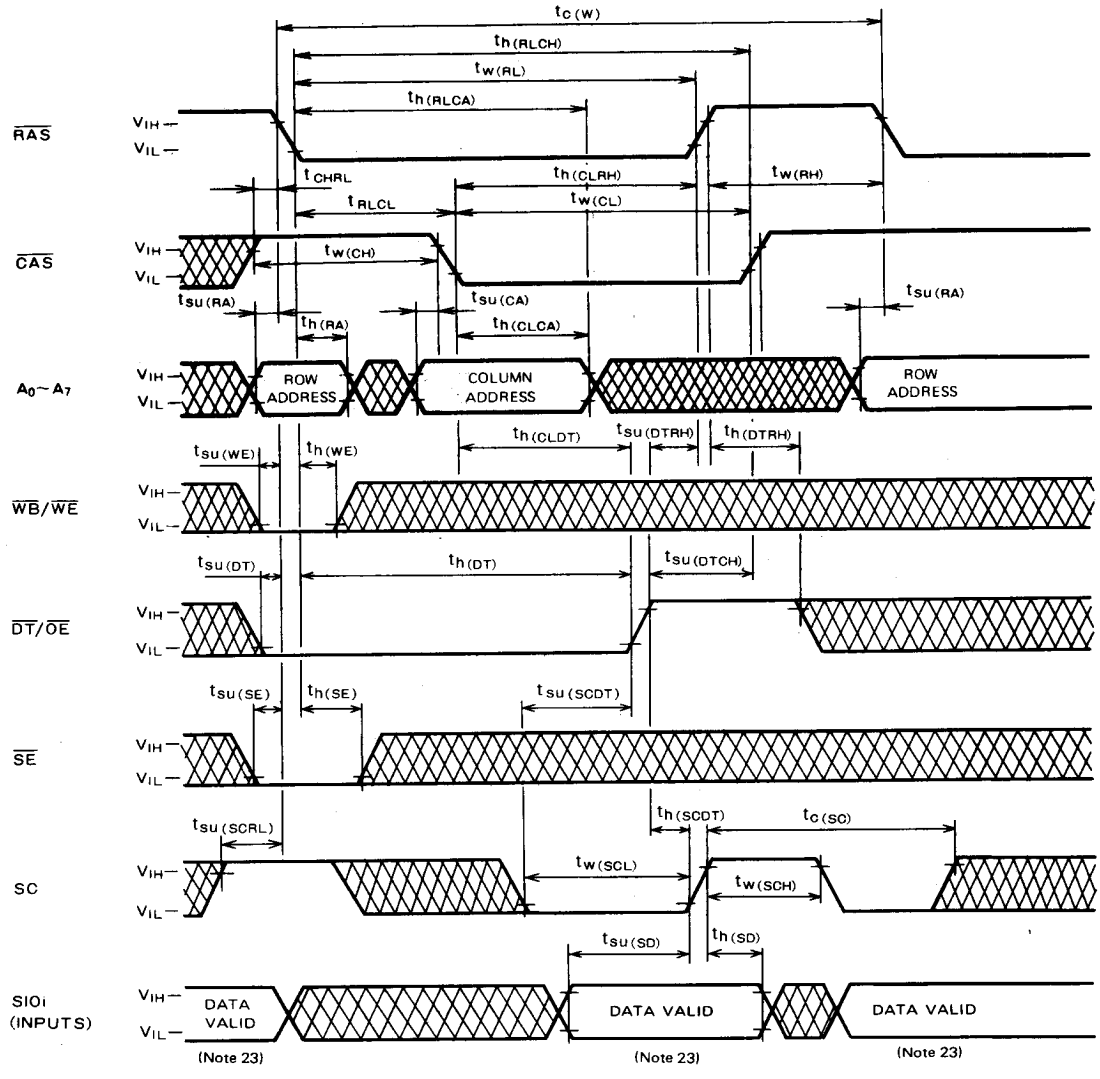
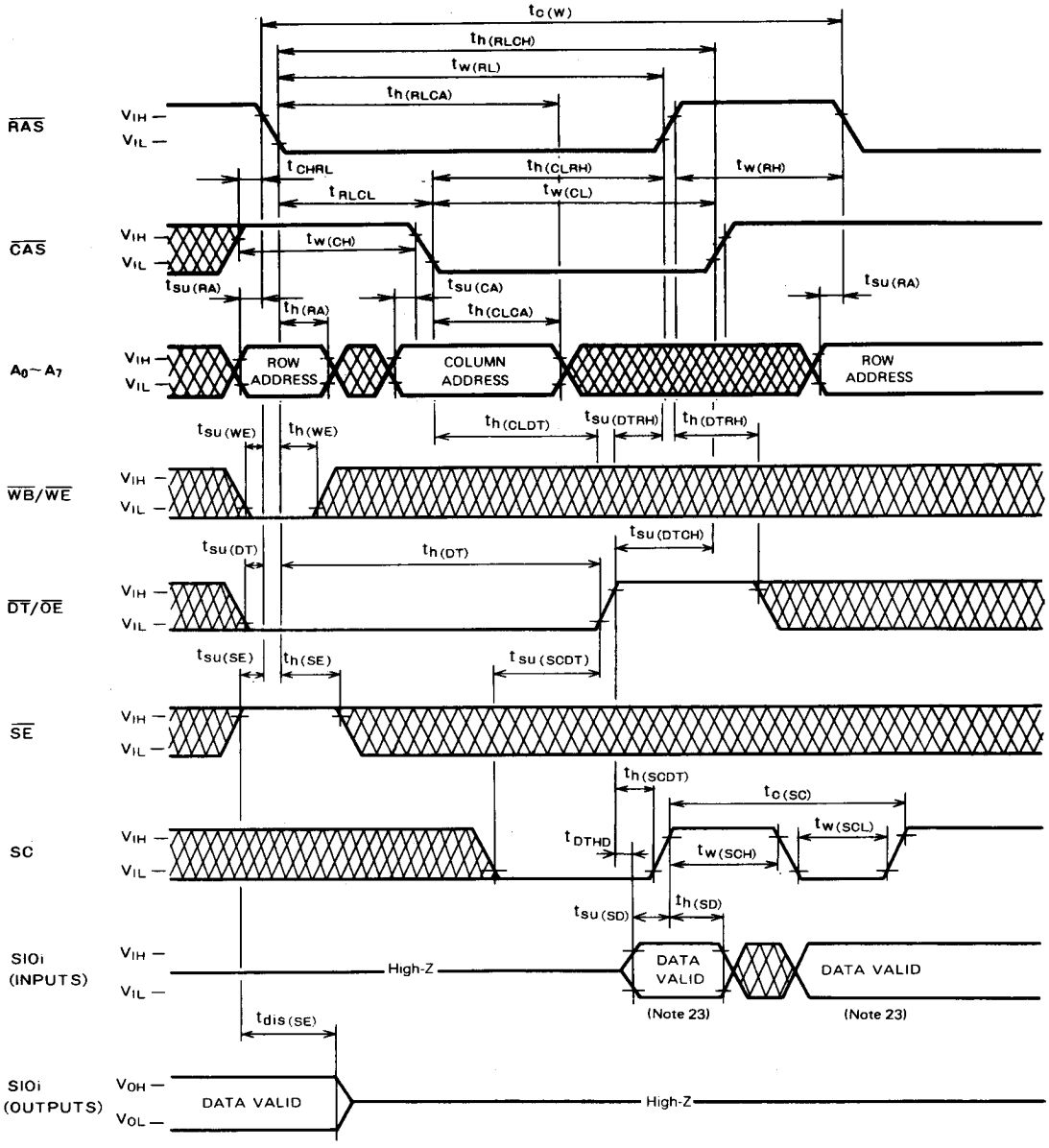
Write Transfer Cycle (B-port Active) Serial Write Setup (SAM → RAM)



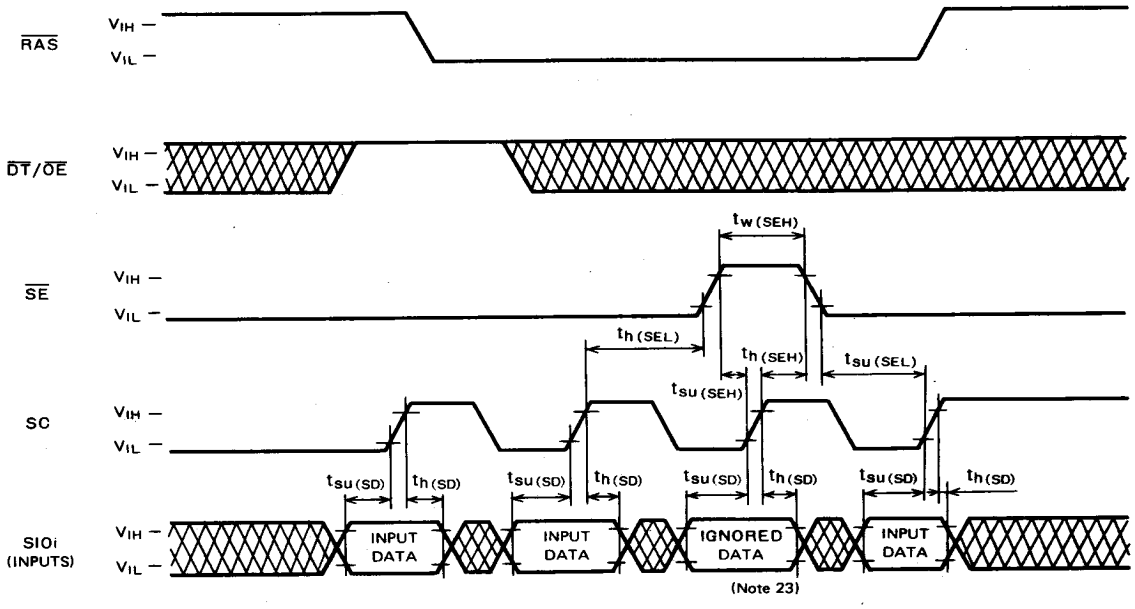
Note 23: When $\overline{SE}$ is "H" level, the serial input data are not written into the Data register, but the serial data selector is worked.

Pseudo Write Transfer Cycle (B-port Active) Serial Write Setup



MITSUBISHI ELECTRIC

Serial Write Cycle



Serial Read Cycle