YAMAHA LSI

YM3526

NO.85-05

YM3526

廃番

FM OPERATOR TYPE-L (OPL)

■ OUTLINE

The OPL (FM Operator Type-L) is a newly developed sound generator designed for CAPTAIN (Character and Pattern Telephone Access Information Network) systems and teletext. FM sound generators are used by melody part, and various sounds can be generated under software control. A sound generator with the features of various musical instruments is provided for rhythm part. This sound generator has built-in low frequency oscillators for vibrato and amplitude modulation to reduce software workload.
tion to reduce software workload.
Because OPL output is digital, a D/A converter (YM3014 or equivalent) is required.

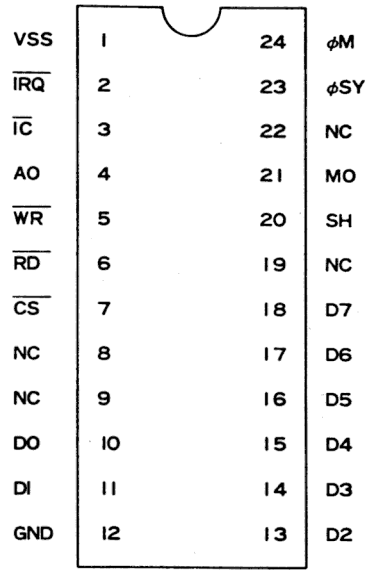
■ FEATURES

- The FM sound generator is used to produce more realistic sounds.
- The mode selector enables switching between the sounding of all nine tones at one time, and of six melodies and five rhythms. In either case, the tones can varied.
- The vibrato oscillator and amplitude modulation oscillator are built in.
- Two programmable timers are incorporated.
- Composite Sinusoidal Modeling is possible.
- Input and output are TTL compatible.
- Si-gate CMOS LSI.
- 5V single power supply.

NIPPON GAKKI CO., LTD.

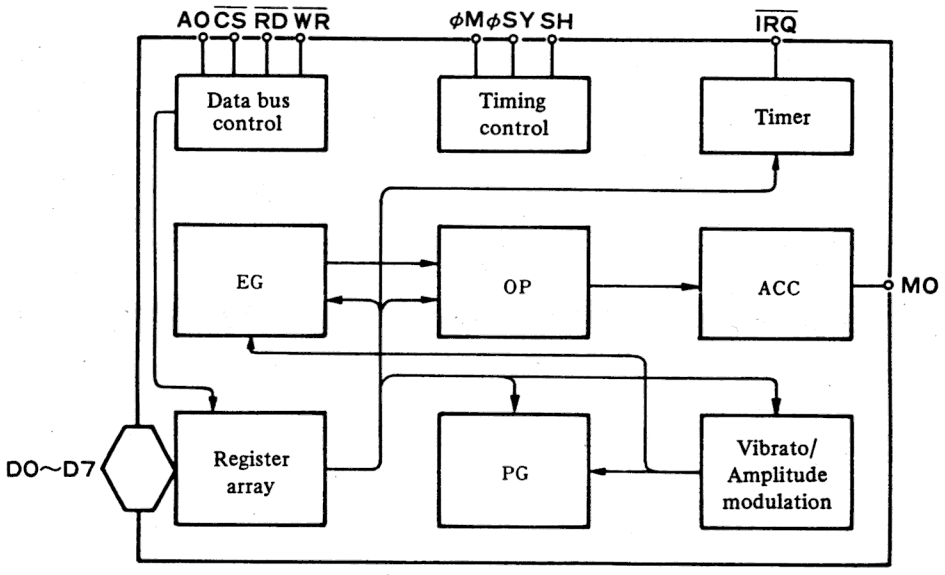
Catalog No. LSI-2135260

■ PIN LAYOUT



*NC : No Connection

■ BLOCK DIAGRAM



■ DESCRIPTION OF TERMINAL FUNCTIONS

1. ϕM

This is the master clock of OPL. The input frequency is 3.58 MHz.

2. ϕSY, SH

These are the clock (ϕSY) and synchronizing signals (SH) for driving the D/A converter that converts digital output of the FM sound generator to analog values.

3. D0 ~ D7

This is an 8-bit bidirectional bus that send and receive data between OPL and the processor.

4. $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, AO

These control bidirectional bus D0 ~ D7.

$\overline{CS}$	RD	WR	AO	
0	1	0	0	The register address is written to OPL.
0	1	0	1	The contents of the register are written to OPL.
0	0	1	0	The contents of OPL status are read.
0	0	1	1	The data on the bus are not guaranteed.
1	x	x	x	Bus lines of D0 ~ D7 have high impedance.

5. $\overline{IRQ}$

This interrupt signal output from two timers. It can be masked by the program.

6. $\overline{IC}$

When set to low levels, the system is reset. The contents of the register array become "0."

7. MO

This is the digital output of the FM sound generator. An external D/A converter is required.

8. VCC

+5 V power terminal.

9. GND

Grounding terminal.

■ DESCRIPTION OF FUNCTIONS

OPL has two sounding modes: nine melodies, and a combination of six melodies and five rhythms. This mode selection can be controlled by the program. For melodies, the same FM sound generator as used in the Yamaha DX-7 synthesizer is used for creating excellent sound quality.

For this reason, this LSI is the most suitable for sound generators for new media-related equipment, including CAPTAIN systems and teletex.

Frequency modulation for this LSI is obtained by the following expressions. Either sine waves synthesis (1) or frequency modulation (2) can be programmed for individual sounds.

$$F_1 = I_1 \sin w_1 t + I_2 \sin w_2 t \ldots\ldots (1)$$

$$F_2 = I_2 (w_1 t + I_2 \sin w_2 t) \ldots\ldots (2)$$

A noise generator and synthesizer are provided for rhythmic sounds. Sounding requires no special external control. Five rhythmic sounds: bass drum (BD), snare drum (SD), high-hat cymbals (HH), top cymbal (TC) and tom-tom (TOM) can be generated.
The internal parts of OPL are functionally divided into nine blocks to perform the following:

(a) Register array:
OPL is controlled by the register array contents and the shape of the envelope and phase data are determined.

(b) Phase generator (PG):
A phase of the FM sound generator at each time step is generated. This receives and accumulates phases from the register array, thereby calculating a phase at each time step.

(c) Envelope generator (EG):
This generates an envelope and modulation index for each sound. This generator receives instructions for such items as slope (rate) and offset (total level) from the register array to generate an envelope.

(d) Operator (OP):
The operator receives phase information (θ) from PG and envelope information (E) from EG, and calculates $E\sin\theta$.

(e) Accumulator (ACC):
The accumulator is used to accumulate each sound at each sampling time (50 KHz) in order to convert data to match the D/A converter.

(f) Vibrato oscillator/amplitude modulation oscillator:
Low frequency oscillators for vibrato and amplitude modulation. The oscillation frequency is 6.4 Hz for vibrato and 7 Hz for amplitude modulation.

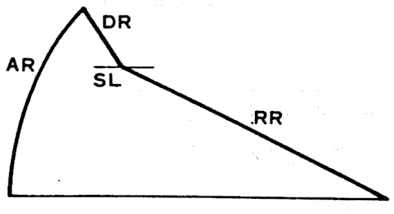
(g) Timers:
Threre are two types for general-purpose timers for long and short.

(h) Data bus control.

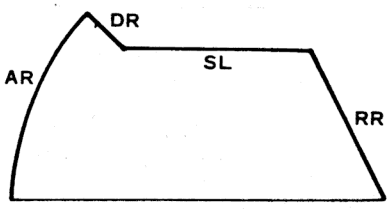
(i) Timing control.

■ CONTENTS OF EACH REGISTER

	Address	
1	01	TEST information. Usually set to "0."
2	02	Time setting on timer 1.
3	03	Time setting on timer 2.
4	04	Controls the operation of timers 1 and 2 and resets interrupt signals.
5	08	CSM is for the CSM speech synthesis mode. NOTE SEL is for switching the keyboard split by using the F-Number.
6	20 ~ 35	MULTI controls the relationship between fundamental waves and harmonics. KSR is key scale of RATE. EG-TYPE is for the switching of Non Percussive Tone and Percussive Tone. 0 is for Percussive Tone and is for Non Percussive Tone. VIB indicates the ON/OFF of vibrato. AM indicates the ON/OFF of modulation.
7	40 ~ 55	TL provides a total level for adjustment of each sound level. KSL is the level key scale.
8	60 ~ 75	DR sets the decay rate at the decay time. AR sets the rate of increase at the attack time.
9	80 ~ 95	RR provides the decay rate at Release/Sustain time. SL. provides the level for shifting from decay to sustain.
10	AO ~ B8	F-Number provides chords within one octave. Block represents octave information for each sound. KON indicates that the sound being generated when it is "1."
11	BD	Controls rhythmic sounds and the corresponding bits for setting the ON/OFF of each rhythm. When the R bit is 1, the system is in the rhythm mode. VIB DEP indicates the depth of vibrato. 0 = 7¢, 1 = 14¢ AM DEP indicates the depth of amplitude modulation. 0 = 1dB, 1 = 4.8dB.
12	C0 ~ C8	FB indicates FM feedback factor. C indicates Sin wave synthesis or FM modulation.



Percussive Tone



Non Percussive Tone

■ ELECTRIC CHARACTERISTICS

1. Absolute maximum rating

Item	Rated Value	Unit
Terminal voltage	−0.3 ~ 7.0	V
Operating ambient temperature	0 ~ 70	°C
Storage temperature	−50 ~ 125	°C

2. Recommended operating conditions

Item	Symbol	Minimum	Standard	Maximum	Unit
Power voltage	Vcc	4.5	5	5.5	V
	GND	0	0	0	V

3. DC characteristics

Item		Symbol	Conditions	Minimum	Standard	Maximum	Unit
Input high-level voltage	All input	V_{IH}		2.0			V
Input low-level voltage	All input	V_{IL}				0.8	V
Input leak current	$\phi M \cdot \overline{WR} \cdot \overline{RD} \cdot AO$	I_L	Vin = 0 ~ 5V	−10		10	μA
Three-state (off-state) input current	$D_0 \sim D_7$	I_{TSL}	Vin = 0 ~ 5V	−10		10	μA
Output high-level voltage	Output except for $\overline{IRQ}$	V_{OH1}	I_{OH1} = 0.4mA	2.4			V
		V_{OH2}	I_{OH2} = 40μA	3.3			V
Output low-level voltage	All output	V_{OL}	I_{OL} = 2.0mA			0.4	V
Output leak current (off-state)	$\overline{IRQ}$	I_{LOFF}	V_{OH} = 0 ~ 5V	−10		10	V
Pull-up resistor	$\overline{IC}$, $\overline{CS}$	R_{PU}		80		400	KΩ
Input capacity	All input	C_I				10	PF
Output capacity	All output	C_O				10	PF
Power supply current		I_{CC}				30	mA

4. AC characteristics

Item		Symbol	Conditions	Minimum	Standard	Maximum	Unit
Input clock frequency	φM	fc	Fig. A-1	2.0	3.58	4.0	MHz
Input clock duty	φM			40	50	60	%
Input clock rise time	φM	T_R	Fig. A-1				ns
Input clock fall time	φM	Tf	Fig. A-1				ns
Address setup time	Ao	T_{AS}	Fig. A-2, Fig. A-3	10			ns
Address hold time	Ao	T_{AH}	Fig. A-2, Fig. A-3	20			ns
Chip select write width	$\overline{CS}$	T_{CSW}	Fig. A-2	100			ns
Chip select read width	$\overline{CS}$	T_{CSR}	Fig. A-3	200			ns
Write pulse write width	$\overline{WR}$	T_{WW}	Fig. A-2	100			ns
Write data setup time	$D_0 \sim D_7$	T_{DS}	Fig. A-2	20			ns
Write date hold time	$D_0 \sim D_7$	T_{DH}	Fig. A-2	30			ns
Read pulse width	$\overline{RD}$	T_{RW}	Fig. A-3	200			ns
Read data access time	$D_0 \sim D_7$	T_{ACC}	Fig. A-3			200	ns
Read data hold time	$D_0 \sim D_7$	T_{RDH}	Fig. A-3	10			ns
Output rise time	φSY	T_{OR1}	Fig. A-4			100	ns
Output fall time	MO · SH	T_{OR2}	Fig. A-5			150	ns
Output fall time	φSY	T_{OF1}	Fig. A-4			100	ns
	MO · SH	T_{OF2}	Fig. A-5			150	ns
Reset pulse width	$\overline{IC}$	N_{ICW}	Fig. A-6	80			cycle

■ REGISTER MAP

ADDRESS	D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	COMMENT.
01	TEST	LSI TEST DATA
02	TIMER－1	TIMER－1 DATA
03	TIMER－2	TIMER－2 DATA
04	RST | MASK T1 T2 | ST2 ST1	IRQ RESET/TIMER CONTROL
08	CSM | SEL	CSM speech synthesis mode/Note Select.
20 … 35	AM | VIB | EG-TYP | KSR | MULTI	AM/VIB/EG－TYPE/KSR/MULTIPLE
40 … 55	KSL | TL	KSL/TOTAL LEVEL
60 … 75	A R | D R	ATTACK RATE/DECAY RATE
80 … 95	S L | R R	SUSTAIN RATE/RELEASE RATE
A0 … A8	F－Number(L)	KON/BLOCK/F－Number
B0 … B8	KON | BLOCK | F-Num (H)	
BD	DEP AM VIB | R | BD SD TOM TC HH	DEPTH(AM/VIB)/RHYTHM(BD·SD·TOM·TC·HH)
C0 … C8	F B | C	FEEDBACK/CONNECTION

■ STATUS REGISTER

IRQ | FLAG T1 T2	IRQ/FLAG(T1、T2)

■ TIMING CHART (For setting the timing, use V_{IH} = 2.0V, V_{IL} = 0.8V as reference values.)

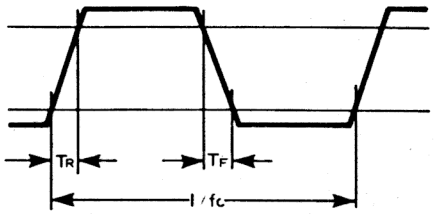
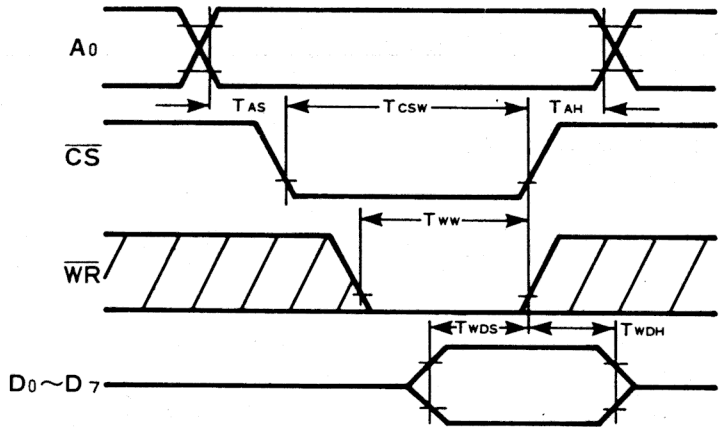
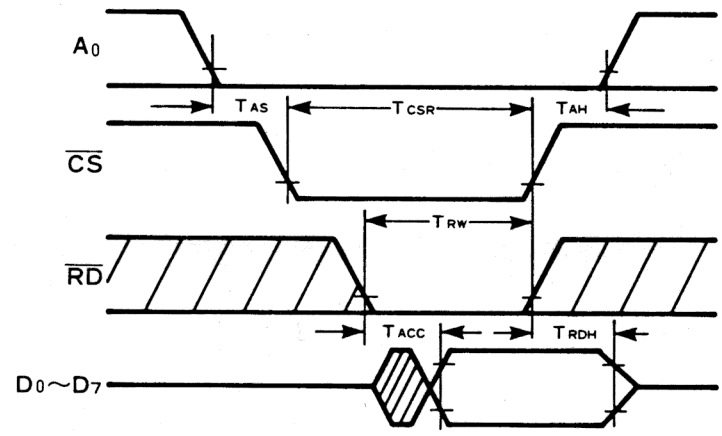


Fig. A-1. Clock timing



(Note)
T_{CSW}, T_{WW} and T_{WDH} are based on whether CS or WR is set at a high level.

Fig. A-2. Write timing



(Note)
T_{ACC} is based on either CS or RD, depending on which reaches a low level next.
T_{CSR}, T_{RW} and T_{RDH} are based whether CS or RD is set at a high level.

Fig. A-3. Read timing

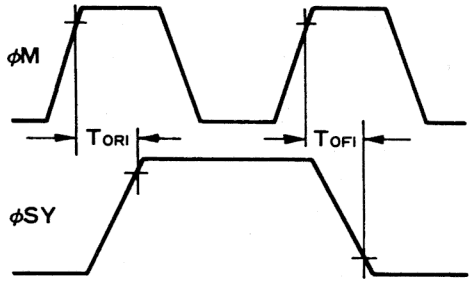


Fig. A-4. φM and φSY

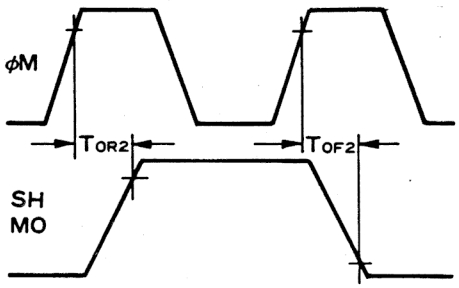


Fig. A-5. φM and SH · MO

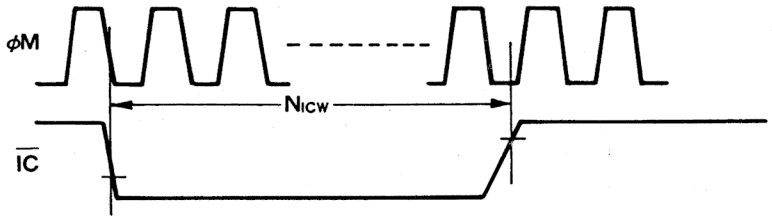
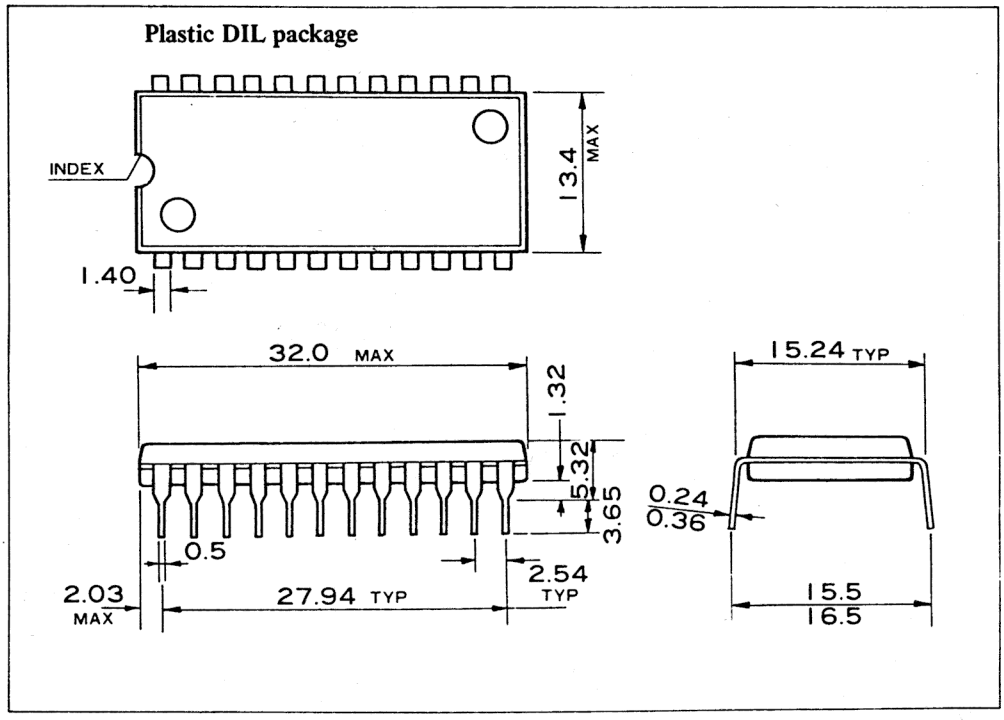


Fig. A-6. Reset pulse

■ DIMENSIONS



* Specifications subject to change for improvement without notice.

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