Asynchronous Communication Interface Adapter (ACIA)

GOULD Electronics

S6850/S68A50/S68B50

Features

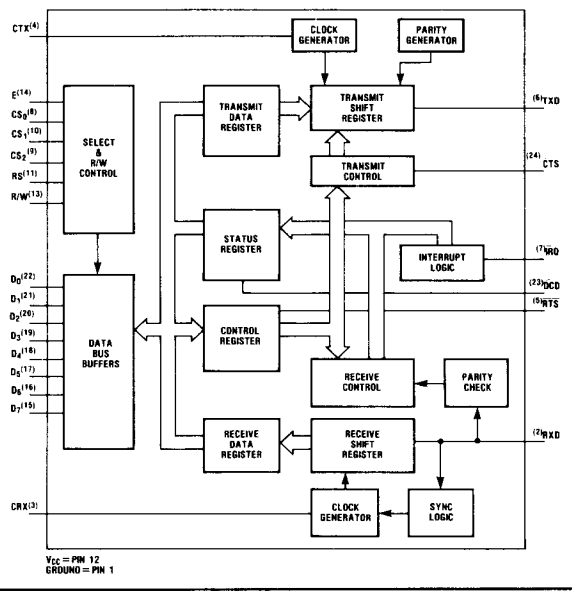
- 8-Bit Bi-directional Data Bus for Communication with MPU
- False Start Bit Deletion
- Peripheral/Modem Control Functions
- Double Buffered Receiver and Transmitter
- One or Two Stop Bit Operation
- Eight and Nine-Bit Transmission With Optional Even and Odd Parity
- Parity, Overrun and Framing Error Checking
- Programmable Control Register
- Optional ÷1, ÷16, and ÷64 Clock Modes
- Up to 500,000 bps Transmission

Functional Description

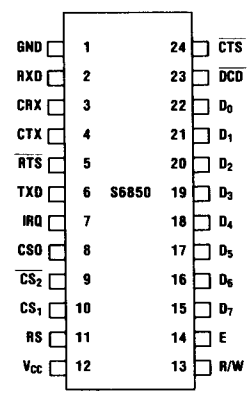
The S6850 Asynchronous Communications Interface Adapter (ACIA) provides the data formatting and control to interface serial asynchronous data communications to bus organized systems such as the S6800 Microprocessing Unit.

The S6850 includes select enable, read/write, interrupt and bus interface logic to allow data transfer over an 8-bit bi-directional data bus. The parallel data of the bus system is serially transmitted and received by the asynchronous data interface, with proper formatting and error checking. The functional configuration of the ACIA is programmed via the data bus during system initialization. Word lengths, clock division ratios and transmit control through the Request to Send output may be programmed. For modem operation three control lines are provided. These lines allow the ACIA to interface directly with the S6860 0-600 bps digital modem.

Block Diagram



Pin Configuration



S6850/S68A50/S68B50

Absolute Maximum Ratings*

Supply Voltage	−0.3V to +7.0V
Operating Temperature Range	0°C to +70°C
Input Voltage	−0.3V to +7.0V
Storage Temperature Range	−55°C to +150°C

*NOTE: This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC (Static) Characteristics: (V_{CC} = 5.0V ±5%, T_A = 25°C, unless otherwise noted.)

Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{IHT}	Input High Threshold Voltage	+2.0	—	—	Vdc
V_{ILT}	Input Low Threshold Voltage	—	—	+0.8	Vdc
I_{IN}	Input Leakage Current (V_{IN} = 0 to 5.0 Vdc) R/W, RS, CS_0, CS_1, $\overline{CS_2}$, Enable	—	1.0	2.5	μAdc
I_{TSI}	Three-State (Off State) Input Current (V_{IN} = 0.4 to 2.4 Vdc, V_{CC} = max) D_0, D_7	—	2.0	10	μAdc
V_{OH}	Output High Voltage (I_{LOAD} = 100μAdc, Enable Pulse Width 25μs) All Outputs Except $\overline{IRQ}$	+2.4	—	—	Vdc
V_{OL}	Output Low Voltage (I_{LOAD} = 1.6mAdc) Enable Pulse Width 25μs	—	—	+0.4	Vdc
I_{LOH}	Output Leakage Current (Off State) $\overline{IRQ}$	—	1.0	10	μAdc
P_D	Power Dissipation	—	300	525	mW
C_{IN}	Input Capacitance (V_{IN} = 0, T_A = 25°C, f = 1.0MHz)				pF
	D_0 - D_7	—		10	12.5
	R/W, RS, CS_0, CS_1, $\overline{CS_2}$, RXD, $\overline{CTD}$, $\overline{DCD}$, CTX, CRX	—		7.0	7.5
	Enable	—		7.0	7.5
C_{OUT}	Output Capacitance (V_{IN} = 0, T_A = 25°C, f = 1.0MHz)	—	—	10	pF

Figure 1. Enable Signal Characteristics

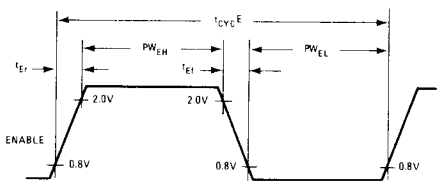
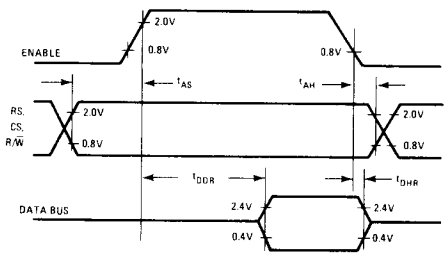


Figure 2. Bus Read Timing Characteristics



S6800 FAMILY

S6850/S68A50/S68B50

AC (Dynamic) Characteristics

Loading = 130pF and one TTL load for D_0-D_7 = 20pF and 1 TTL load for RTS and TXD = 100pF and 3KΩ to V_{CC} for IRQ.

Symbol	Parameter	S6850		S68A50		S68B50		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{cyc(E)}$	Enable Cycle Time	1000		666		500		ns
PW_{EH}	Enable Pulse Width, High	450		280		220		ns
PW_{EL}	Enable Pulse Width, Low	430		280		210		ns
t_{Er}, t_{Ef}	Enable Pulse Rise and Fall Times		25		25		25	ns
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{DDR}	Data Delay Time, Read		320		220		180	ns
t_{DHR}	Data Hold Time, Read	10		10		10		ns
t_{DSW}	Data Setup Time, Write	195		80		60		ns
t_{DHW}	Data Hold Time, Write	10		10		10		ns

Transmit/Receive Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Unit
f_C	÷1 mode ÷16 mode ÷64 mode			500 800 800	KHz KHz KHz
PW_{CL}	Clock Pulse Width, Low State	600			nsec
PW_{CH}	Clock Pulse Width, High State	600			nsec
t_{TDD}	Delay Time, Transmit Clock to Data Out			1.0	μsec
t_{RDSU}	Set Up Time, Receive Data	500			nsec
t_{RDH}	Hold Time, Receive Data	500			nsec
t_{IRQ}	Delay Time, Enable to $\overline{IRQ}$ Reset			1.2	μsec
t_{RTS}	Delay Time, Enable to $\overline{RTS}$			1.0	μsec

Figure 3. Bus Write Timing Characteristics

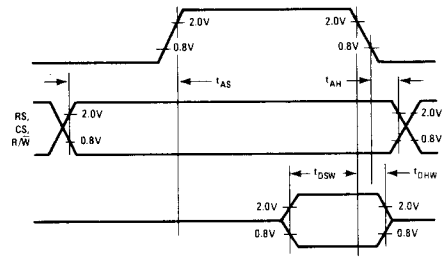


Figure 4. Bus Timing Test Loads