Am2716/Am4716

2048 x 8-Bit UV Erasable PROM

DISTINCTIVE CHARACTERISTICS

- Direct replacement for Intel 2716
- Interchangeable with Am9218 – 16K ROM
- Single +5V power supply
- Fast access time – 450ns standard with 350ns and 390ns options
- Low power dissipation
  - 525mW active
  - 132mW standby
- Fully static operation – no clocks
- Three-state outputs
- TTL compatible inputs/outputs
- 100% MIL-STD-883 reliability assurance testing

GENERAL DESCRIPTION

The Am2716/Am4716 is a 16384-bit ultraviolet erasable and programmable read-only memory. It is organized as 2048 words by 8 bits per word, operates from a single +5V supply, has a static standby mode and features fast single address location programming.

Because the Am2716/Am4716 operates from a single +5V supply, it is ideal for use in microprocessor systems. All programming signals are TTL levels, requiring a single pulse. For programming outside of the system, existing EPROM programmers may be used. Locations may be programmed singly, in blocks, or at random. Total programming time for all bits is 100 seconds.

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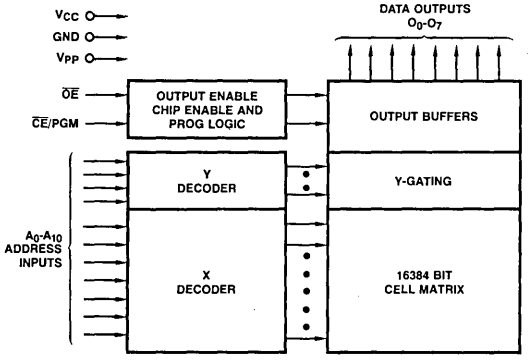
BLOCK DIAGRAM



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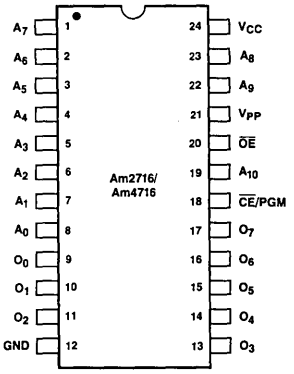
MODE SELECTION

Mode \ Pins	CE/PGM (18)	OE (20)	VPP (21)	VCC (24)	Outputs (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

CONNECTION DIAGRAM
Top View



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A_0-A_{10}: Addresses
O_0-O_7: Outputs
CE/PGM: Chip Enable/Program
OE: Output Enable

ORDERING INFORMATION

Package Type	Ambient Temperature Specification	Order Number	t_{ACC} (ns)	t_{CE}(ns)	t_{OE}(ns)
Hermetic DIP Transparent Window	0°C ≤ T_A ≤ +70°C	AM2716DC	450	450	120
		AM2716-1DC	350	350	120
		AM2716-2DC	390	390	120
		AM2716-6DC	450	650	200
		AM4716DC	450	1000	200
		AM4716-6DC	650	650	200

MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	−65 to +125°C
Ambient Temperature Under Bias	−10 to +80°C
Voltage on All Inputs/Outputs (except V_{PP}) with Respect to GND	+6 to −0.3V
Voltage on V_{PP} During Program with Respect to GND	+26.5 to −0.3V

READ OPERATION

DC CHARACTERISTICS

$0°C \leq T_A \leq +70°C$, V_{CC} (Notes 1, 2) = +5V ±5%, except +5V ±10% for Am2716-1, V_{PP} (Note 2) = V_{CC} for all device types.

Parameters	Description	Test Conditions	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 5.25V/0V		10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 5.25V/0V		10	μA
I_{PP1} (Note 2)	V_{PP} Current	V_{PP} = 5.25V		5 (Note 3)	mA
I_{CC1} (Note 2)	V_{CC} Current (Standby)	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}		25	mA
I_{CC2} (Note 2)	V_{CC} Current (Active)	$\overline{OE}$ = $\overline{CE}$ = V_{IL}		100	mA
V_{IL}	Input Low Voltage		−0.1	0.8	Volts
V_{IH}	Input High Voltage		2.0	V_{CC}+1	Volts
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA @ V_{CC} (Min)		0.45	Volts
V_{OH}	Output High Voltage	I_{OH} = −400μA @ V_{CC} (Min)	2.4		Volts

AC CHARACTERISTICS

$0°C \leq T_A \leq +70°C$, V_{CC} (Notes 1, 2) = +5V ±5%, except +5V ±10% for Am2716-1, V_{PP} (Note 2) = V_{CC} for all device types.

Parameters	Description	Test Conditions (Note 4)	Min Values	Max Values 2716	2716-1	2716-2	2716-6	4716	4716-6	Units
t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		450	350	390	450	450	650	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		450	350	390	650	1000	650	ns
t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}		120	120	120	200	200	200	ns
t_{DF}	Output Enable High to Output Float	$\overline{CE}$ = V_{IL}	0	100	100	100	100	100	100	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0							ns

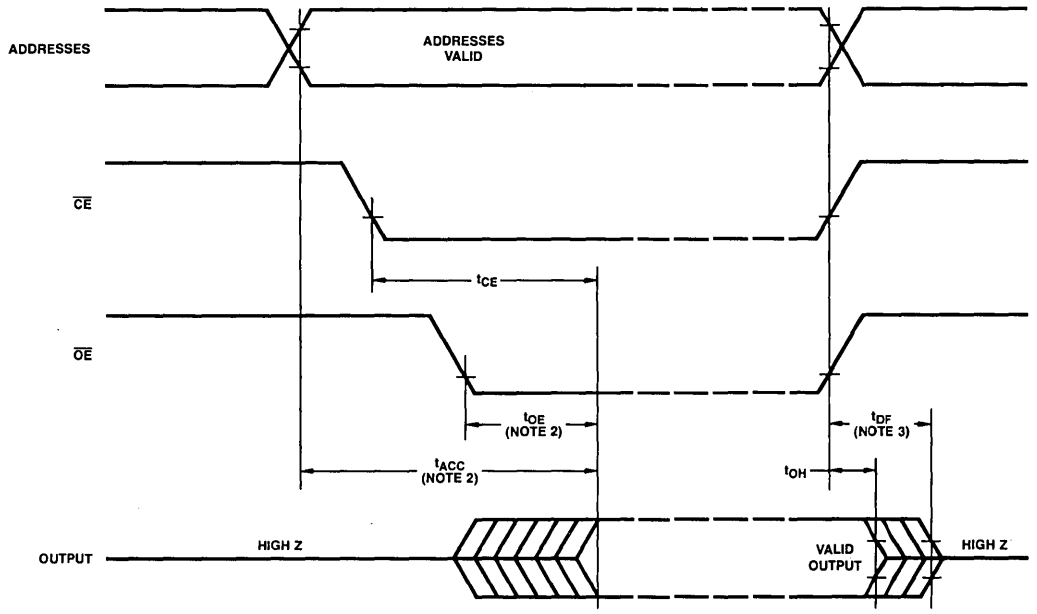
CAPACITANCE (Note 5)

T_A = +25°C, f = 1MHz

Parameters	Description	Test Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. 8mA for Am4716 and Am4716-6.
4. Other Test Conditions: a) Output Load: 1 TTL gate and C_L = 100pF
b) Input Rise and Fall Times: ≤20ns
c) Input Pulse Levels: 0.8 to 2.2V
d) Timing Measurement Reference Level:
Inputs: 1V and 2V
Outputs: 0.8V and 2V
5. This parameter is only sampled and is not 100% tested.

AC WAVEFORMS (Note 1)



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Notes: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

PROGRAM OPERATION

DC PROGRAMMING CHARACTERISTICS

T_A = +25°C ±5°C, V_{CC} (Note 1) = 5V ±5%, V_{PP} (Notes 1, 2) = 25V ±1V

Parameters	Description	Test Conditions	Min	Max	Units
I_{LI}	Input Current	V_{IN} = 5.25/0.45V		10	μA
I_{PP1}	V_{PP} Supply Current	$\overline{CE}$/PGM = V_{IL}		5	mA
I_{PP2}	V_{PP} Supply Current During Programming Pulse	$\overline{CE}$/PGM = V_{IH}		30	mA
I_{CC}	V_{CC} Supply Current			100	mA
V_{IL}	Input Low Level		−0.1	0.8	Volts
V_{IH}	Input High Level		2.0	V_{CC}+1	Volts

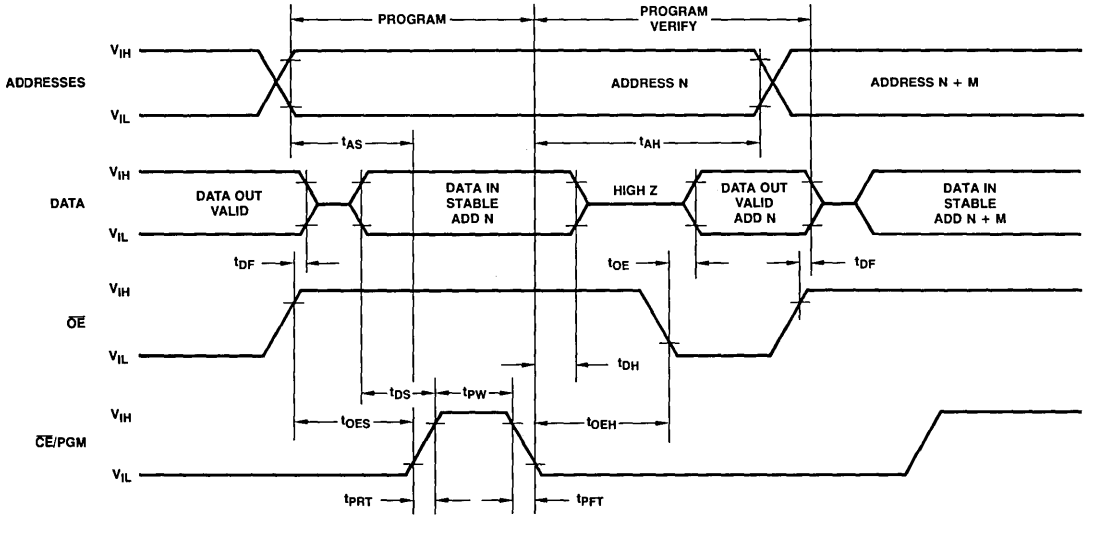
AC PROGRAMMING CHARACTERISTICS

T_A = +25°C ±5°C, V_{CC} (Note 1) = 5V ±5%, V_{PP} (Notes 1, 2) = 25V ±1V

Parameters	Description	Test Conditions	Min	Max	Units
t_{AS}	Address Set-up Time	Input t_R and t_F (10% to 90%) = 20ns Input Signal Levels = 0.8 to 2.2V Input Timing Reference Level = 1V and 2V Output Timing Reference Level = 0.8V and 2V	2		μs
t_{OES}	Output Enable Set-up Time		2		μs
t_{DS}	Data Set-up Time		2		μs
t_{AH}	Address Hold Time		2		μs
t_{OEH}	Output Enable Hold Time		2		μs
t_{DH}	Data Hold Time		2		μs
t_{DF}	Output Disable to Output Float Delay ($\overline{CE}$/PGM = V_{IL})		0	120	ns
t_{OE}	Output Enable to Output Delay ($\overline{CE}$/PGM = V_{IL})		–	120	ns
t_{PW}	Program Pulse Width		45	55	ms
t_{PRT}	Program Pulse Rise Time		5	–	ns
t_{PFT}	Program Pulse Fall Time		5	–	ns

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} must not be greater than 26 volts including overshoot. Permanent device damage may occur if the device is taken out of or put into the socket when V_{PP} = 25 volts is applied. Also, during $\overline{OE}$ = $\overline{CE}$/PGM = V_{IH}, V_{PP} must not be switched from 5 volts to 25 volts or vice versa.

PROGRAMMING WAVEFORMS



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ERASING THE Am2716/Am4716

In order to clear all locations of their programmed contents, it is necessary to expose the Am2716/Am4716 to an ultraviolet light source. A dosage of 15 Wseconds/cm^2 is required to completely erase an Am2716/Am4716. This dosage can be obtained by exposure to an ultraviolet lamp [wavelength of 2537 Angstroms (Å)] with intensity of 12000μW/cm^2 for 15 to 20 minutes. The Am2716/Am4716 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am2716/Am4716, and similar devices, will erase with light sources having wavelengths shorter than 4000 Angstroms. Although erasure times will be much longer than with UV sources at 2537Å, nevertheless the exposure to florescent light and sunlight will eventually erase the Am2716/Am4716, and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

PROGRAMMING THE Am2716/Am4716

Upon delivery, or after each erasure the Am2716/Am4716 has all 16384 bits in the "1," or high state. "0s" are loaded into the Am2716/Am4716 through the procedure of programming.

The programming mode is entered when +25V is applied to the V_{PP} pin and when $\overline{OE}$ is at V_{IH}. The address to be programmed is applied to the proper address pins. 8-bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 50msec, TTL high level pulse is applied to the $\overline{CE}$/PGM input to accomplish the programming.

The procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. All that is required is that one 50msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55msec. Therefore, applying a DC level to the $\overline{CE}$/PGM input is prohibited when programming.

READ MODE

The Am2716/Am4716 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the outputs pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}) for all devices except Am2716-6 and Am4716. Data is available at the outputs 120ns or 200ns (t_{OE}) after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE

The Am2716/Am4716 has a standby mode which reduces the active power dissipation by 75%, from 525mW to 132mW. The Am2716/Am4716 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

OUTPUT OR-TIEING

To accommodate multiple memory connections, a 2-line control function is provided to allow for:

1. Low memory power dissipation
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

PROGRAM INHIBIT

Programming of multiple Am2716/Am4716s in parallel with different data is also easily accomplished. Except for $\overline{CE}$/PGM, all like inputs (including $\overline{OE}$) of the parallel Am2716/Am4716s may be common. A TTL level program pulse applied to an Am2716/Am4716's $\overline{CE}$/PGM input with V_{PP} at 25V will program that Am2716/Am4716. A low level $\overline{CE}$/PGM input inhibits the other Am2716/Am4716s from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify may be performed with V_{PP} at 25V. Except during programming and program verify, V_{PP} must be at V_{CC}.