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NTE21128
Integrated Circuit
NMOS, 128K (16K x 8) UV EPROM

Description:

The NTE21128 is a 131,072 bit UV erasable and electrically programmable memory EPROM in a 28–Lead DIP type package organized as 16,384 words by 8 bits. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

Features:

- Access Time: 250ns
- Single 5V Supply Voltage
- Low Standby Current: 40mA Max
- TTL Compatible During Read and Program
- Fast Programming Algorithm
- Programming Voltage: 12V Typ

Absolute Maximum Ratings:

Supply Voltage, V_{CC} . . . . . –0.6V to 6.25V
Program Supply, V_{PP} . . . . . –0.6V to 14V
A9 Voltage, V_{A9} . . . . . –0.6V to 13.5V
Input or Output Voltages, V_{IO} . . . . . –0.6V to 6.25V
Ambient Operating Temperature, T_A . . . . . 0° to +70°C
Temperature Under Bias, T_{BIAS} . . . . . –10° to +80°C
Storage Temperature Range, T_{stg} . . . . . –65° to +125°C

Note 1. Except for the rating “Operating Temperature Range”, stresses above those listed in the table “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DC Characteristics (Read Mode and Standby Mode):

(T_A = 0° to + 70°C, V_{CC} = +5V ±5%, V_{PP} = V_{CC})

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output High Voltage	V_{OH}	I_{OH} = –400µA	2.4	–	–	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA	–	–	0.45	V
Input High Voltage	V_{IH}		2.0	–	V_{CC} +1	V
Input Low Voltage	V_{IL}		–0.1	–	0.8	V
Output Leakage Current	I_{LO}	V_{OUT} = 5.25V	–	–	10	µA
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	µA
V_{CC} Current (Standby)	I_{CC1}	$\overline{E}$ = V_{IH}	–	–	25	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{G}$ = $\overline{E}$ = V_{IL}	–	60	100	mA
V_{PP} Current	I_{PP1}	V_{PP} = 5.25V	–	–	15	mA

DC Characteristics (Program, Program Verify, and Program Inhibit Modes):

(T_A = +25° ±5°C, V_{CC} = +5V ±5% Note 2, V_{PP} = +21V ±0.5V)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input High Voltage	V_{IH}		2.0	–	V_{CC} +1	V
Input Low Voltage	V_{IL}		–0.1	–	0.8	V
Input Leakage Current	I_{LI}	V_{IN} = V_{IL} or V_{IH}	–	–	10	µA
Output High Voltage	V_{OH}	I_{OH} = –400µA	2.4	–	–	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA	–	–	0.45	V
V_{CC} Current (Program Inhibit)	I_{CC1}	$\overline{E}$ = V_{IH}	–	–	25	mA
V_{CC} Current (Program Verify)	I_{CC2}		–	–	100	mA
V_{PP} Current (Program)	I_{PP2}	$\overline{E}$ = $\overline{P}$ = V_{IL}	–	–	30	mA
V_{PP} Current (Program Verify)	I_{PP3}	$\overline{E}$ = V_{IL}, $\overline{P}$ = V_{IH}	–	–	15	mA
V_{PP} Current (Program Inhibit)	I_{PP4}	$\overline{E}$ = V_{IH}	–	–	15	mA

Note 2. V_{CC} = 6V ±0.25V for high–speed programming.

AC Characteristics (Read Mode and Standby Mode):

(T_A = 0° to + 70°C, V_{CC} = +5V ±5%, V_{PP} = V_{CC})

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Address to Output Delay	t_{ACC}	$\overline{E}$ = $\overline{G}$ = V_{IL}	–	–	250	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{E}$ = V_{IL}	–	–	250	ns
Output Enable to Output Delay	t_{OE}	$\overline{E}$ = V_{IL}	–	–	100	ns
Output Enable High to Output Delay	t_{DF}	$\overline{E}$ = V_{IL}	0	–	85	ns
Address to Output Hold Time	t_{OH}	$\overline{E}$ = $\overline{G}$ = V_{IL}	0	–	–	ns

Test Conditions:

Input Rise and Fall Times: 20ns
Input Pulse Levels: 0.45V to 2.4V
Timing Measurement Reference Levels:
Inputs: 0.8V and 2.0V
Outputs: 0.8V and 2.0V

AC Characteristics (Program, Program Verify, and Program Inhibit Modes):
(T_A = +25° ±5°C, V_{CC} = +5V ±5%, V_{PP} = +21V ±0.5V)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Address Setup Time	t_{AS}	Input Pulse Levels = 0.45V to 2.4V, Input Timing Reference Level = 0.8V and 2V, Output Timing Reference Level = 0.8V and 2V, Input Rise and Fall Times: 20ns	2	–	–	µs
$\overline{E}$ Setup Time	t_{OES}		2	–	–	µs
Data Setup Time	t_{DS}		2	–	–	µs
Address Hold Time	t_{AH}		0	–	–	µs
$\overline{E}$ Setup Time	t_{CES}		2	–	–	µs
Data Hold Time	t_{DH}		2	–	–	µs
Chip Enable to Output Float Delay	t_{DF}		0	–	130	ns
Data Valid from $\overline{E}$	t_{OE}		–	–	150	ns
Program Pulse Width (Note 3)	t_{PW}		45	50	55	ms
V_{PP} Setup Time	t_{VS}		2	–	–	µs

Note 3. Initial Program Pulse width tolerance is 1msec ±5%.

Test Conditions:

Input Pulse Levels: 0.45V to 2.4V
Input Timing Reference Level: 0.8V and 2.0V
Output Timing Reference Level: 0.8V and 2.0V
Input Rise and Fall Times: 20ns

Capacitance: (T_A = +25°C, f = 1MHz)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	–	4	8	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	–	8	14	pF

Device Operation:

A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP}.

Read Mode

The NTE21128 has the following two control functions: Chip Enable ($\overline{E}$) is the power control used for device selection and Output Enable ($\overline{G}$) is the output control used to gate data to the output pins, independent of device selection.

Address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the outputs after the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least $t_{AVQV} - t_{GLQV}$.

Standby Mode

The standby mode, reducing the maximum active power current from 85mA to 40mA, is achieved by applying a TTL high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

Device Operation (Cont'd):

Two Line Output Control

The NTE21128 features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a. the lowest possible memory power dissipation,
b. complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus.

This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current (I_{CC}) has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of these transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selecting decoupling capacitors. It is recommended that a 1μf ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7μf bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When delivered, all bits of the NTE21128 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NTE21128 is in the programming mode when the V_{PP} input is at 12.5V and $\overline{E}$ and $\overline{P}$ are at TTL low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Fast Programming Algorithm

Fast Programming Algorithm rapidly programs the NTE21128 EPROM using an efficient and reliable method suited to the production programming environment. Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. The Fast Programming Algorithm utilizes two different pulse types: initial and overprogram.

The duration of the initial $\overline{P}$ pulse(s) is 1ms, which will then be followed by a longer overprogram pulse of length 3ms by n (n is equal to the number of the initial one–millisecond pulses applied to a particular NTE21128 location), before a correct verify occurs. Up to 25 one–millisecond pulses per byte are provided for before the over program pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6V and V_{PP} = 12.5V. When the Fast Programming cycle has been completed, all bytes should be compared to the original data with V_{CC} = 5V and V_{PP} = 5V.

Device Operation (Cont'd):

Program Inhibit

Programming of multiple NTE21128s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs (including $\overline{G}$) of the parallel NTE21128 may be common. A TTL low pulse applied to an NTE21128's $\overline{E}$ input, with V_{PP} = 12.5V, will program that NTE21128> A high level $\overline{E}$ input inhibits the other NTE21128s from being programmed.

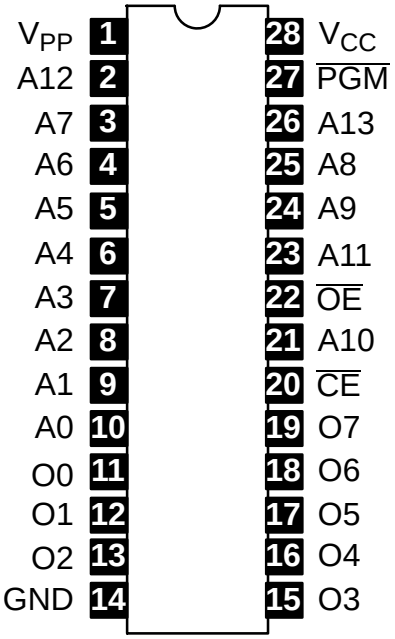
Program Verify

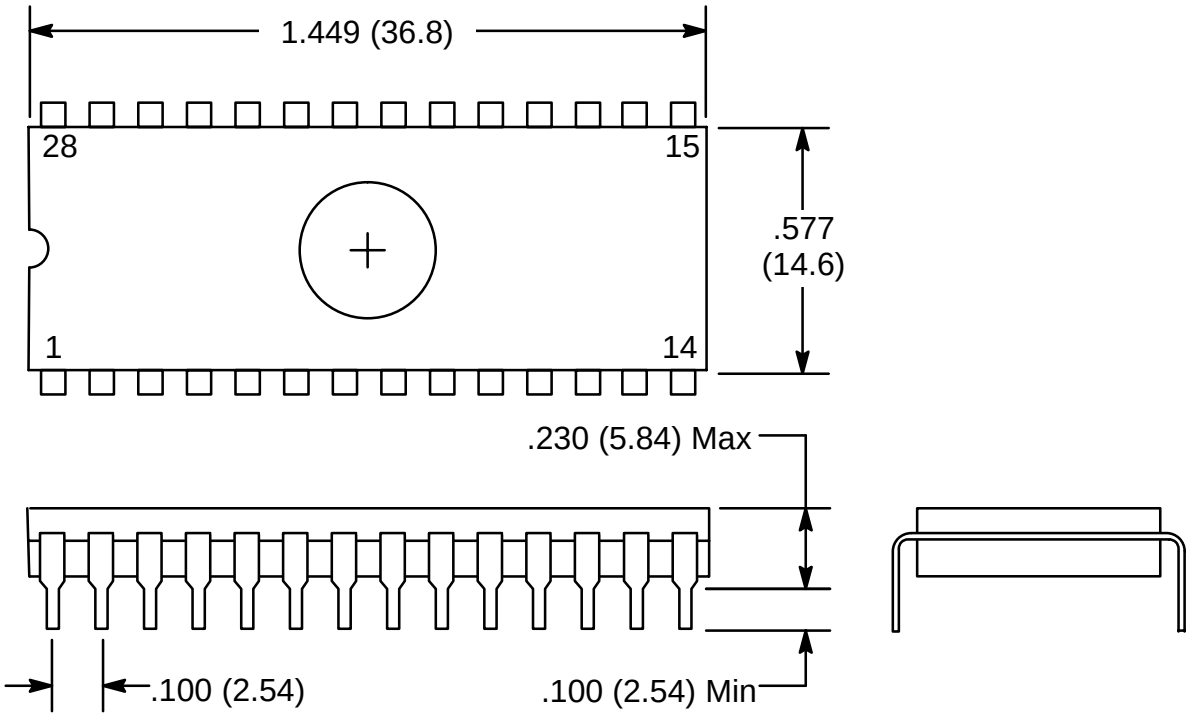
A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{G} = V_{IL}$, $\overline{E} = V_{IL}$, $\overline{P} = V_{IH}$, and V_{PP} at 12.5V.

Erasure Operation:

The erasure characteristic of the NTE21128 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 angstroms. The recommended erasure procedure for the NTE21128 is exposure to short wave ultraviolet light which has a wavelength of 2537 angstroms. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 μW/cm^2 power rating. The NTE21128 should be placed within 2.5cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

Pin Connection Diagram




1.449 (36.8)
28
15
1
14
.577
(14.6)
.230 (5.84) Max
.100 (2.54)
.100 (2.54) Min