OKI semiconductor

T-46-23-17

MSM514256A

262,144-WORD x 4-BIT DYNAMIC RAM

GENERAL DESCRIPTION

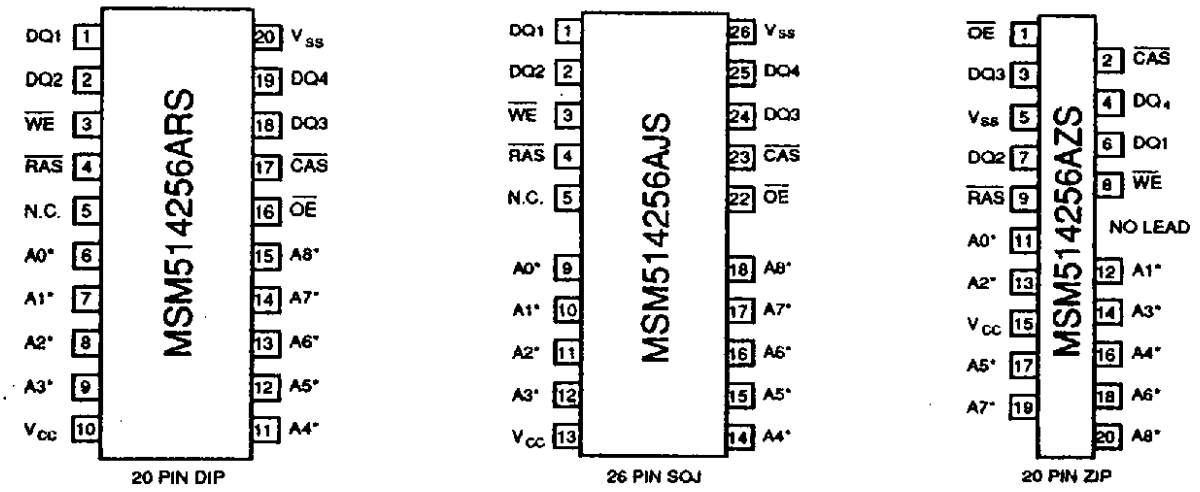
The MSM514256A is a new generation dynamic RAM organized as 262,144 words x 4 bits. The technology used to fabricate the MSM514256A is OKI's CMOS silicon gate process technology. The device operates at a single +5V power supply. Its I/O pins are TTL compatible.

FEATURES

- Silicon gate, triple polysilicon CMOS, 1-transistor memory cell
- Single +5V power supply, ±10% tolerance
- Input: TTL compatible, address input, data input latch
- Output: TTL compatible, tristate, nonlatch
- Refresh: 512 cycles/8 ms
- Output impedance controllable through Early Write and $\overline{OE}$ operations
- 262,144-word x 4-bit organization
- Fast page mode, read/write capability
- $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh, $\overline{RAS}$-only refresh capability
- Gated $\overline{CAS}$
- Built-in V_{BB} generator circuit

Family	Access Time (Max.)	Cycle Time (Min.)	Power Dissipation	
			Operating (Max.)	Standby (Max.)
MSM514256A-70	70ns	140ns	468mW	5.5mW
MSM514256A-80	80ns	160ns	413mW	
MSM514256A-10	100ns	190ns	358mW	

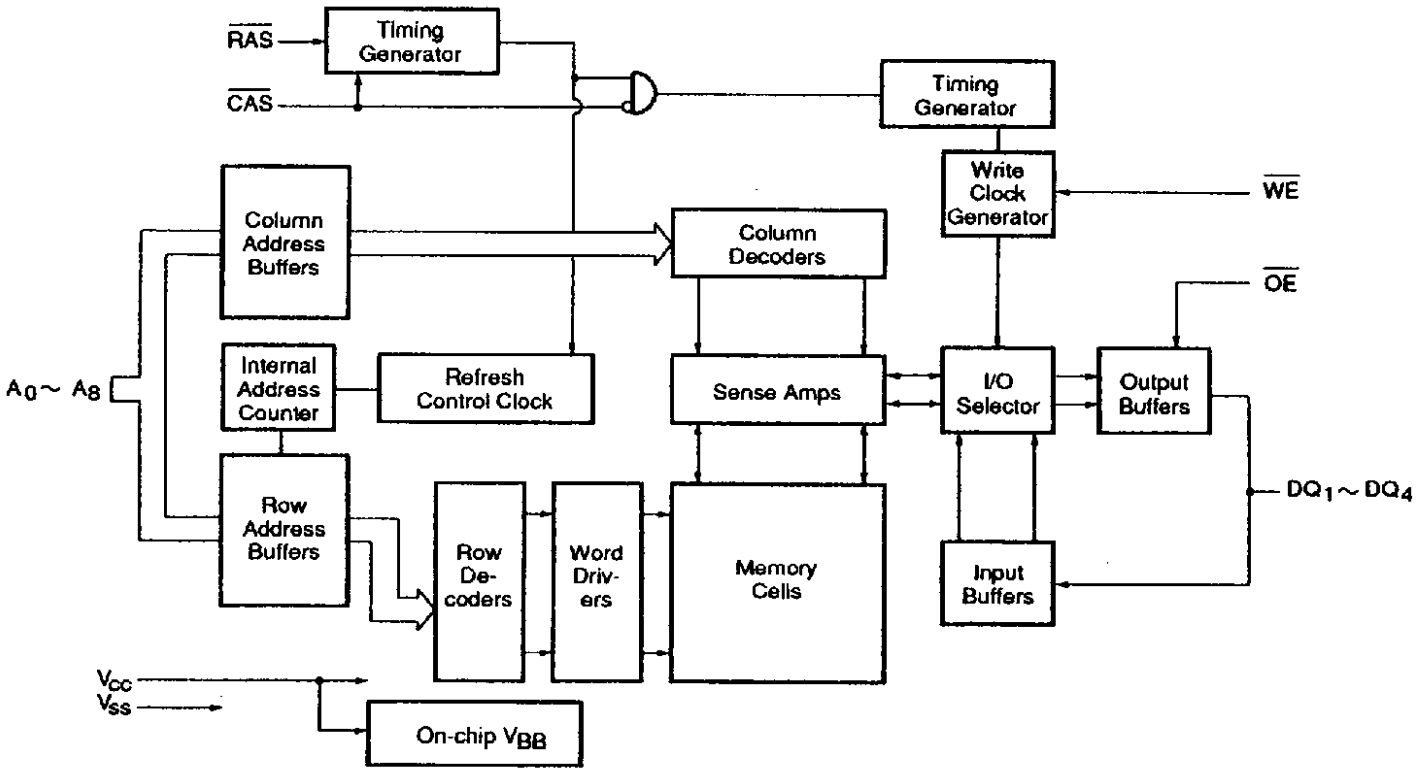
PIN CONFIGURATION (TOP VIEW)



* Refresh Address

Pin Names	Function
A_0 to A_8	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
DQ1 to DQ4	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
Vcc	Power Supply (+5V)
Vss	Ground (0V)
N.C.	No Connection

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Conditions	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	Ta = 25°C	−1.0 to +7.0	V
Short circuit output current	I_{OS}	Ta = 25°C	50	mA
Power dissipation	P_D	Ta = 25°C	1	W
Operating temperature	T_{opr}	–	0 to +70	°C
Storage temperature	T_{stg}	–	−55 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Ta = 0 ~ 70°C)

Parameter	Symbol	Conditions	Value			Unit	Operating Temperature
			Min.	Typ.	Max.		
Supply voltage	V_{CC}	–	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	–	0	0	0	V	
Input high voltage	V_{IH}	–	2.4	–	6.5	V	
Input low voltage	V_{IL}	–	−1.0	–	0.8	V	

DC CHARACTERISTICS

(V_{CC} = 5V ± 10%, Ta = 0 to +70°C)

Parameter	Symbol	Conditions	MSM 514256A-70		MSM 514256A-80		MSM 514256A-10		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
Output high voltage	V_{OH}	I_{OH} = -5.0mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	–
Output low voltage	V_{OL}	I_{OL} = 4.2mA	0	0.4	0	0.4	0	0.4	V	–
Input leakage current	I_{LI}	0V ≦ VI ≦ 6.5V; all other pins not under test = 0V	-10	10	-10	10	-10	10	μA	–
Output leakage current	I_{LO}	D_{OUT} disable 0V ≦ VO ≦ 5.5V	-10	10	-10	10	-10	10	μA	–
Average power supply current* (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = min	–	85	–	75	–	65	mA	–
Power supply current* (Standby)	I_{CC2}	$\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IH}, D_{OUT}=Hz — TTL	–	2	–	2	–	2	mA	–
		MOS	–	1	–	1	–	1		
Average power supply current* ($\overline{RAS}$-only refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH}, t_{RC}=min	–	85	–	75	–	65	mA	–
Average power supply current* ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	$\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$	–	85	–	75	–	65	mA	–
Average power supply current* (Fast page mode)	I_{CC7}	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling, t_{PC}=min	–	75	–	65	–	60	mA	–

* I_{CC} depends on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	Value		Unit
			Min.	Max.	
Input capacitance (A_0 to A_8)	C_{IN1}	–	–	6	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{IN2}	–	–	7	pF
Output capacitance (DQ1 to DQ4)	$C_{I/O}$	–	–	7	pF

AC CHARACTERISTICS

(V_{CC} = 5V ± 10%, Ta = 0 to +70°C) Notes 1,2,3

Parameter	Symbol	MSM 514256A-70		MSM 514256A-80		MSM 514256A-10		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Refresh period	t_{REF}	–	8	–	8	–	8	ms	–
Random read or write cycle time	t_{RC}	140	–	160	–	190	–	ns	–
Read/write cycle time	t_{RWC}	195	–	215	–	255	–	ns	–
Fast page mode cycle time	t_{PC}	45	–	50	–	55	–	ns	–
Fast page mode read/write cycle time	t_{PRWC}	100	–	105	–	120	–	ns	–
Access time from $\overline{RAS}$	t_{RAC}	–	70	–	80	–	100	ns	4,5,6
Access time from $\overline{CAS}$	t_{CAC}	–	20	–	20	–	25	ns	4,5
Access time from column address	t_{AA}	–	35	–	40	–	50	ns	4,6
Access time from $\overline{CAS}$ precharge	t_{CPA}	–	40	–	45	–	50	ns	4
Output low impedance time from $\overline{CAS}$	t_{CLZ}	0	–	0	–	0	–	ns	4
Output buffer turn-off delay	t_{OFF}	0	20	0	20	0	20	ns	–
Transition time	t_T	3	50	3	50	3	50	ns	3
$\overline{RAS}$ precharge time	t_{RP}	60	–	70	–	80	–	ns	–
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	–
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	–
$\overline{RAS}$ hold time	t_{RSH}	20	–	20	–	25	–	ns	–
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10	–	10	–	10	–	ns	–
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	–
$\overline{CAS}$ hold time	t_{CSH}	70	–	80	–	100	–	ns	–
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	22	60	25	75	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	17	40	20	50	ns	6
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	–	10	–	10	–	ns	–
Row address set-up time	t_{ASR}	0	–	0	–	0	–	ns	–
Row address hold time	t_{RAH}	10	–	12	–	15	–	ns	–
Column address set-up time	t_{ASC}	0	–	0	–	0	–	ns	–
Column address hold time	t_{CAH}	15	–	15	–	20	–	ns	–
Column address hold time from $\overline{RAS}$	t_{AR}	55	–	60	–	75	–	ns	–

AC CHARACTERISTICS (CONT.)

Parameter	Symbol	MSM 512456A-70		MSM 512456A-80		MSM 512456A-10		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	–	40	–	50	–	ns	–
Read command set-up time	t_{RCS}	0	–	0	–	0	–	ns	–
Read command hold time	t_{RCH}	0	–	0	–	0	–	ns	8
Write command hold time from $\overline{RAS}$	t_{WCR}	55	–	60	–	75	–	ns	–
Write command set-up time	t_{WCS}	0	–	0	–	0	–	ns	7
Write command hold time	t_{WCH}	15	–	15	–	20	–	ns	–
Write command pulse width	t_{WP}	15	–	15	–	20	–	ns	–
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	–	20	–	25	–	ns	–
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	–	20	–	25	–	ns	–
Data-in set-up time	t_{DS}	0	–	0	–	0	–	ns	–
Data-in hold time	t_{DH}	15	–	15	–	20	–	ns	–
Data-in hold time from $\overline{RAS}$	t_{DHR}	55	–	60	–	75	–	ns	–
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	50	–	50	–	60	–	ns	7
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	100	–	110	–	135	–	ns	7
Column address to $\overline{WE}$ delay time	t_{AWD}	65	–	70	–	85	–	ns	7
Read command hold time reference to $\overline{RAS}$	t_{RRH}	0	–	10	–	10	–	ns	8
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	–	10	–	10	–	ns	–
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	30	–	30	–	30	–	ns	–
$\overline{CAS}$ active delay time from $\overline{RAS}$ precharge	t_{RPC}	10	–	10	–	10	–	ns	–
$\overline{CAS}$ precharge time (Refresh counter test)	t_{CPT}	40	–	40	–	50	–	ns	–
$\overline{CAS}$ precharge time	t_{CPN}	10	–	10	–	15	–	ns	–
$\overline{RAS}$ hold time reference to $\overline{OE}$	t_{ROH}	20	–	20	–	20	–	ns	–
Access time from $\overline{OE}$	t_{OEA}	–	20	–	20	–	25	ns	–
$\overline{OE}$ delay time	t_{OED}	20	–	20	–	25	–	ns	–
$\overline{OE}$ to data output buffer turn-off delay	t_{OEZ}	0	20	0	20	0	25	ns	–
$\overline{OE}$ command hold time	t_{OEH}	20	–	20	–	25	–	ns	–

Notes: 1. An initial pause of 100 μs is required after power-up followed by a minimum of any 8 $\overline{RAS}$ cycles (example: $\overline{RAS}$-only Refresh) before proper device operation is achieved.

2. The AC measurements assume the transition time (t_T) = 5 ns.

3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring the timing of the input signals. Transition times are measured between V_{IH} and V_{IL}.

4. Measured using an equivalent load circuit of 2 TTL loads and 100pF.

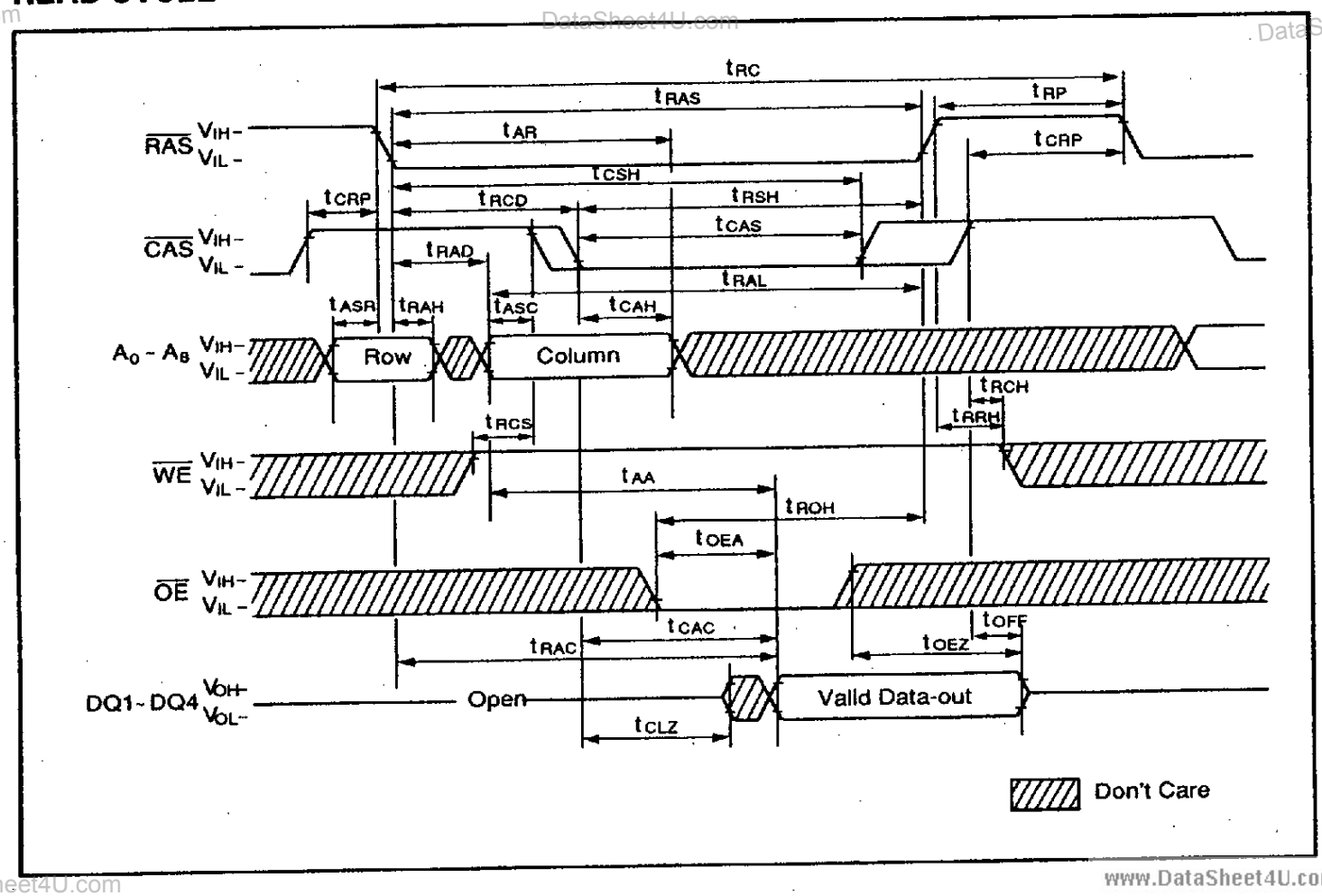
5. Operating within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. The spec. t_{RCD} (max.) is for reference only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, the access time is controlled exclusively by t_{CAC}.

6. Operating within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. The spec. t_{RAD} (max.) is for reference only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled exclusively by t_{AA}.

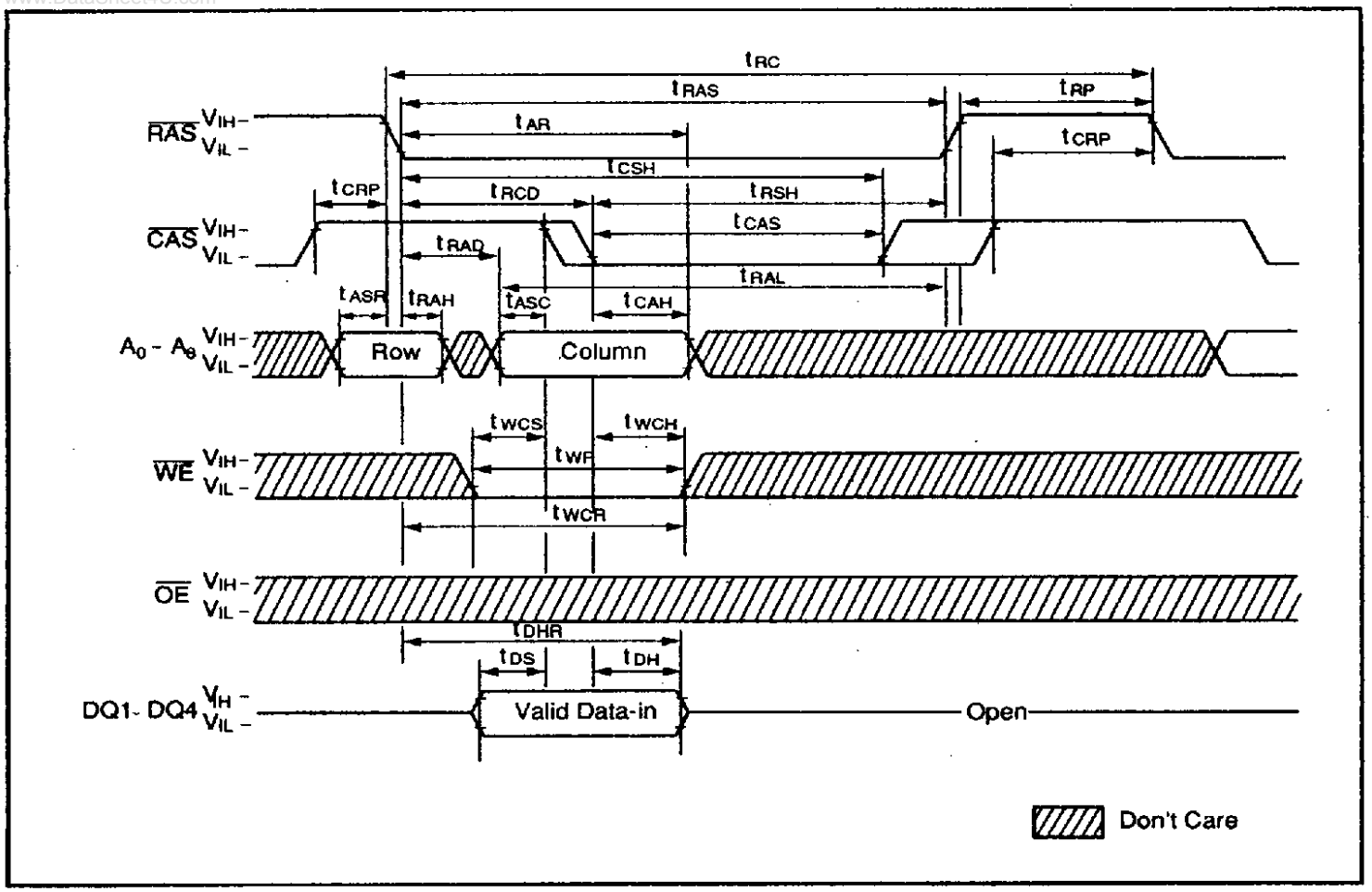
7. The specs t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet for reference only. If $t_{WCS} \geq t_{WCS}$ (min.), cycle is an Early Write cycle and data out remains in a high impedance state throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min.), $t_{RWD} \geq t_{RWD}$ (min.) and $t_{AWD} \geq t_{AWD}$ (min.), the cycle is a Read-Write cycle and the data out contains data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out is indeterminate at access time.

8. Either the t_{RRH} or the t_{RCH} spec. must be satisfied for a proper read cycle.

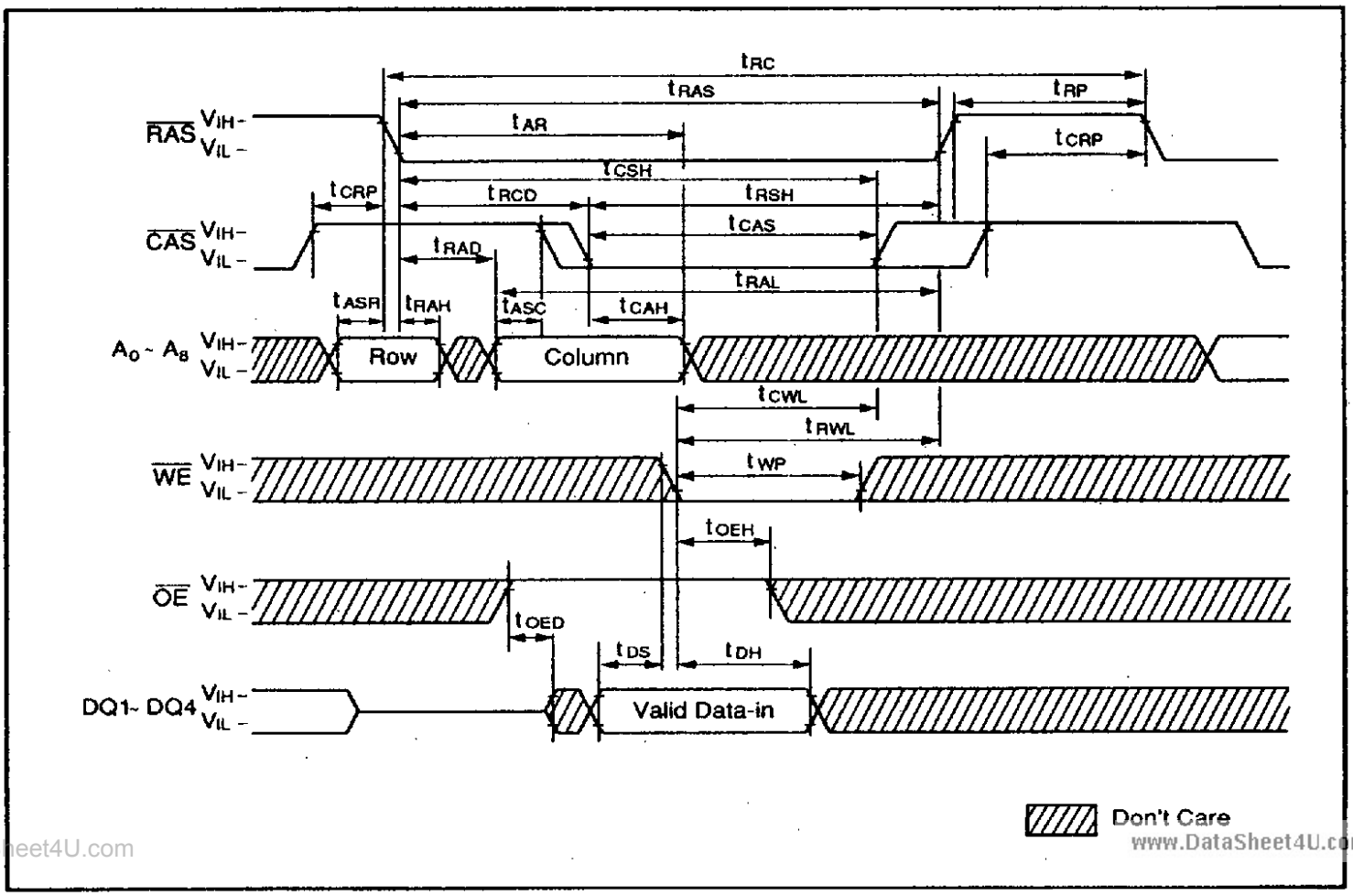
READ CYCLE



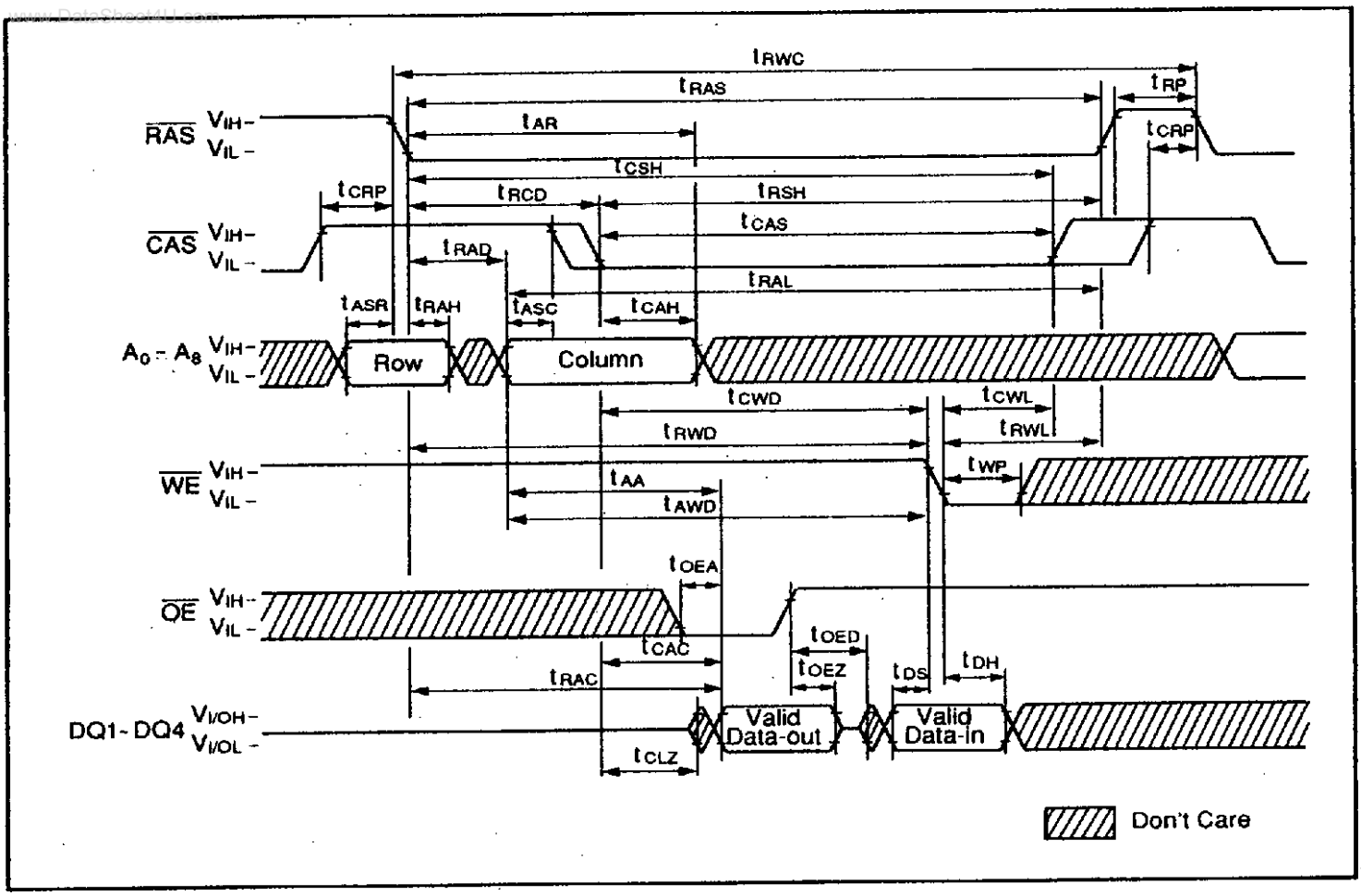
WRITE CYCLE (EARLY WRITE)



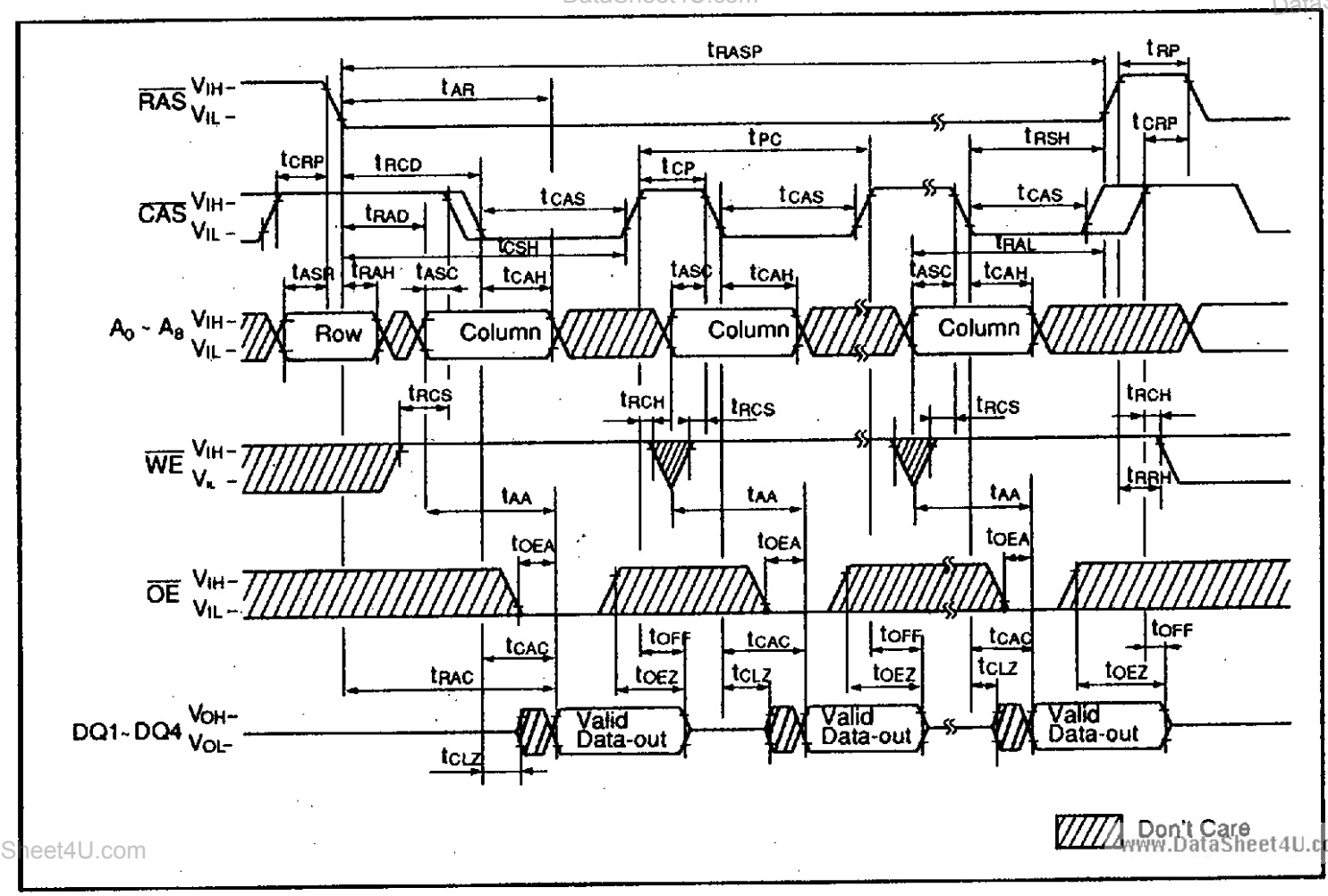
WRITE CYCLE ($\overline{OE}$ CONTROL WRITE)



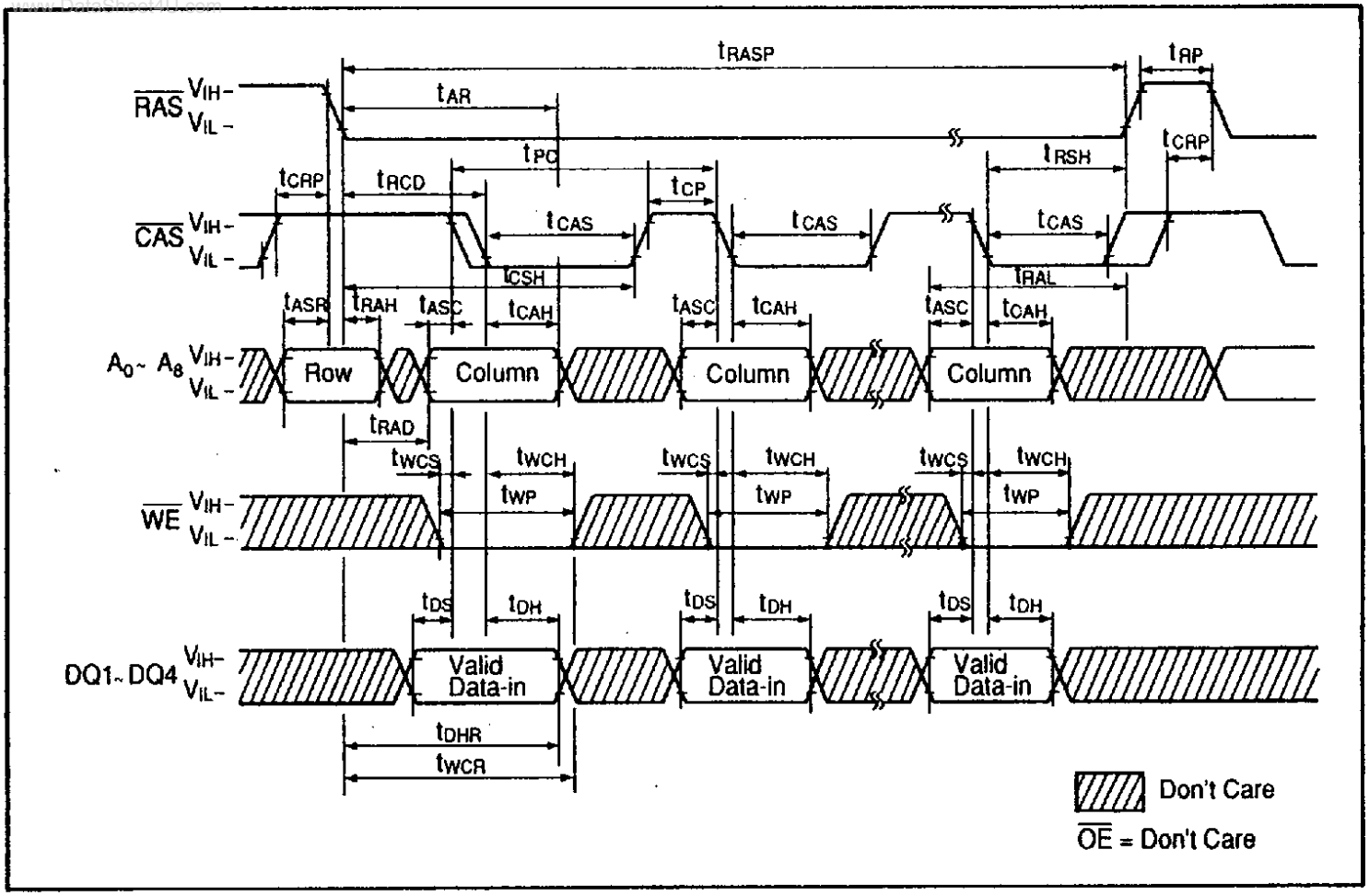
READ/WRITE CYCLE



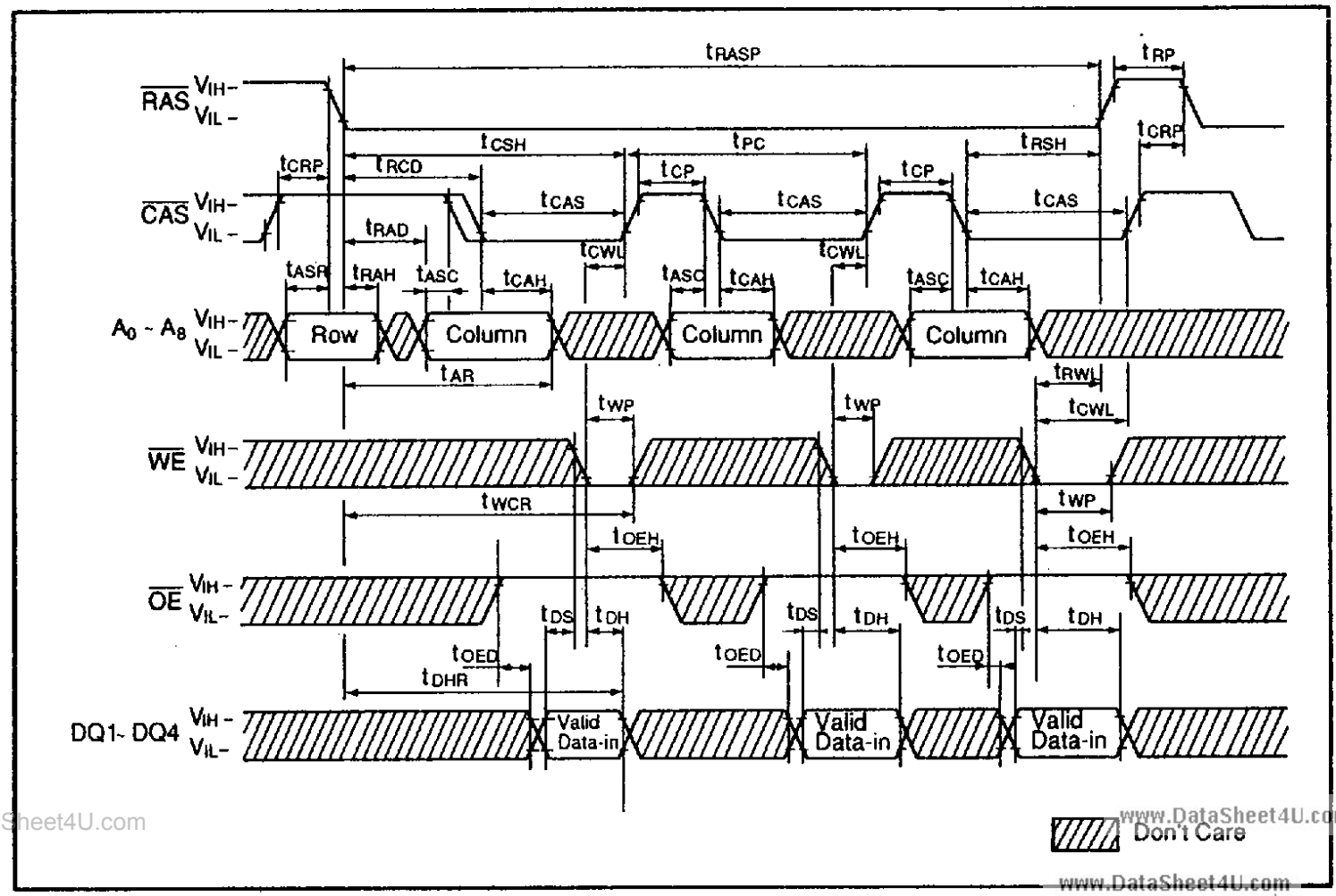
FAST PAGE MODE READ CYCLE



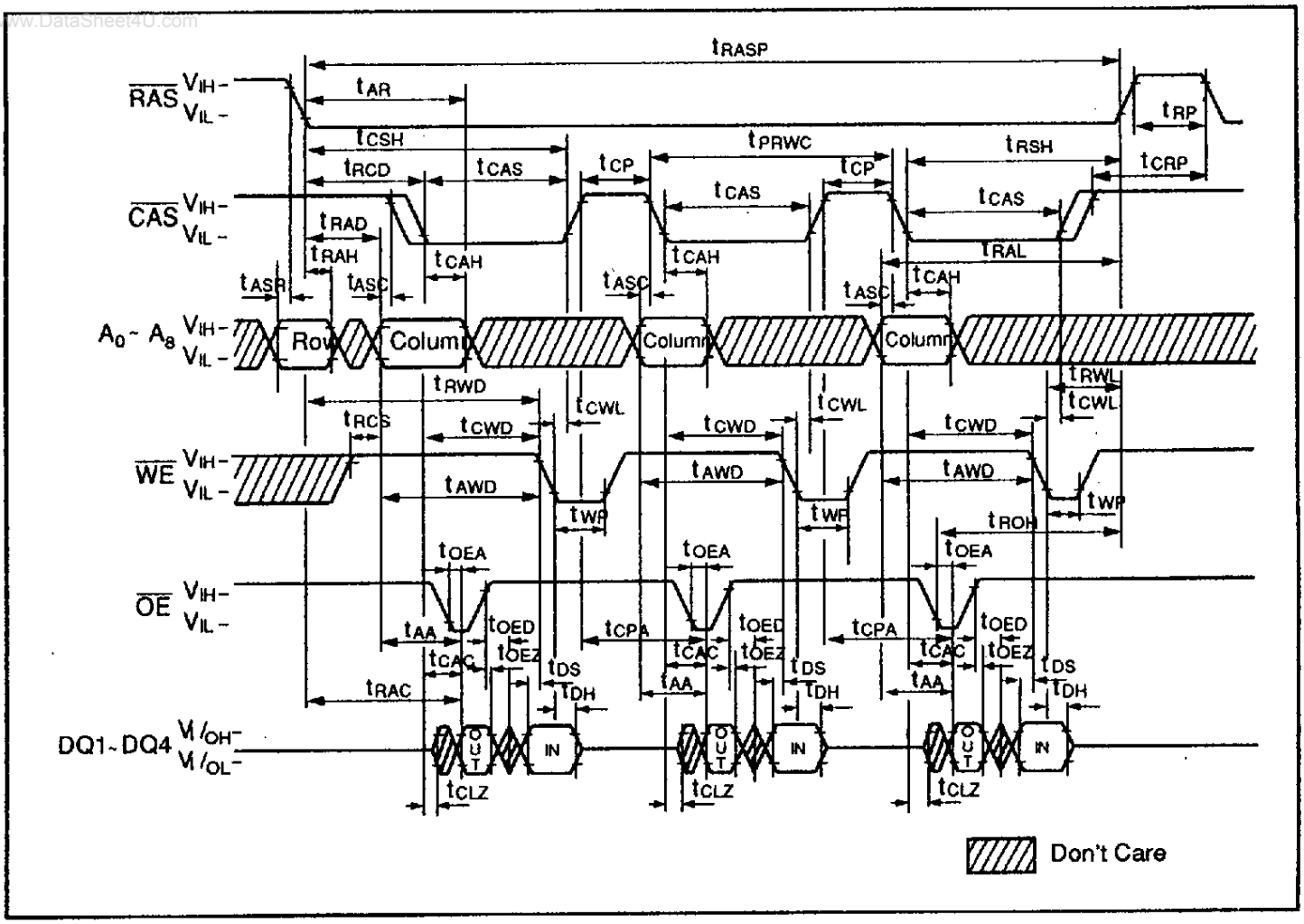
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



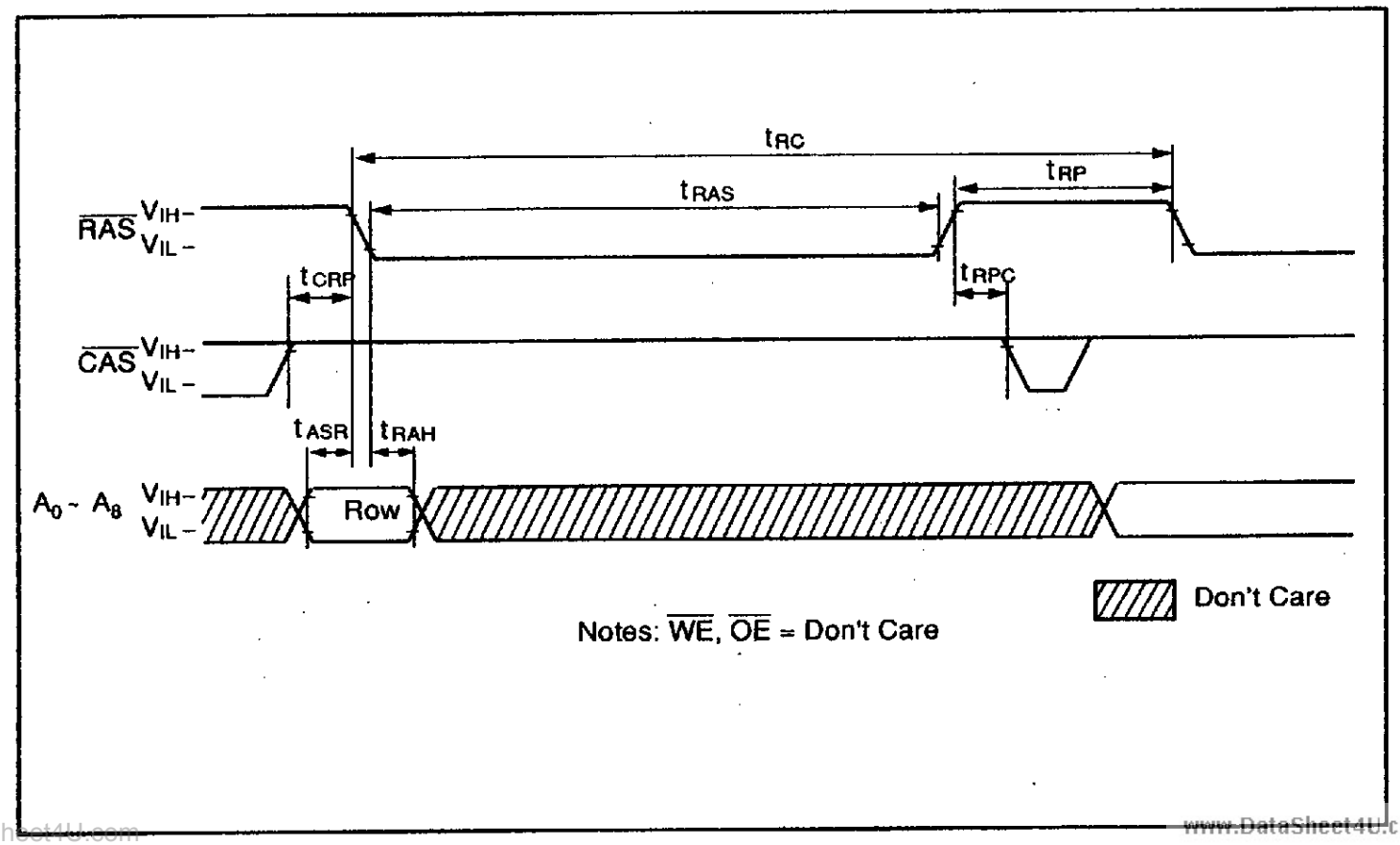
FAST PAGE MODE WRITE CYCLE ($\overline{OE}$ CONTROL WRITE)



FAST PAGE MODE READ/WRITE CYCLE

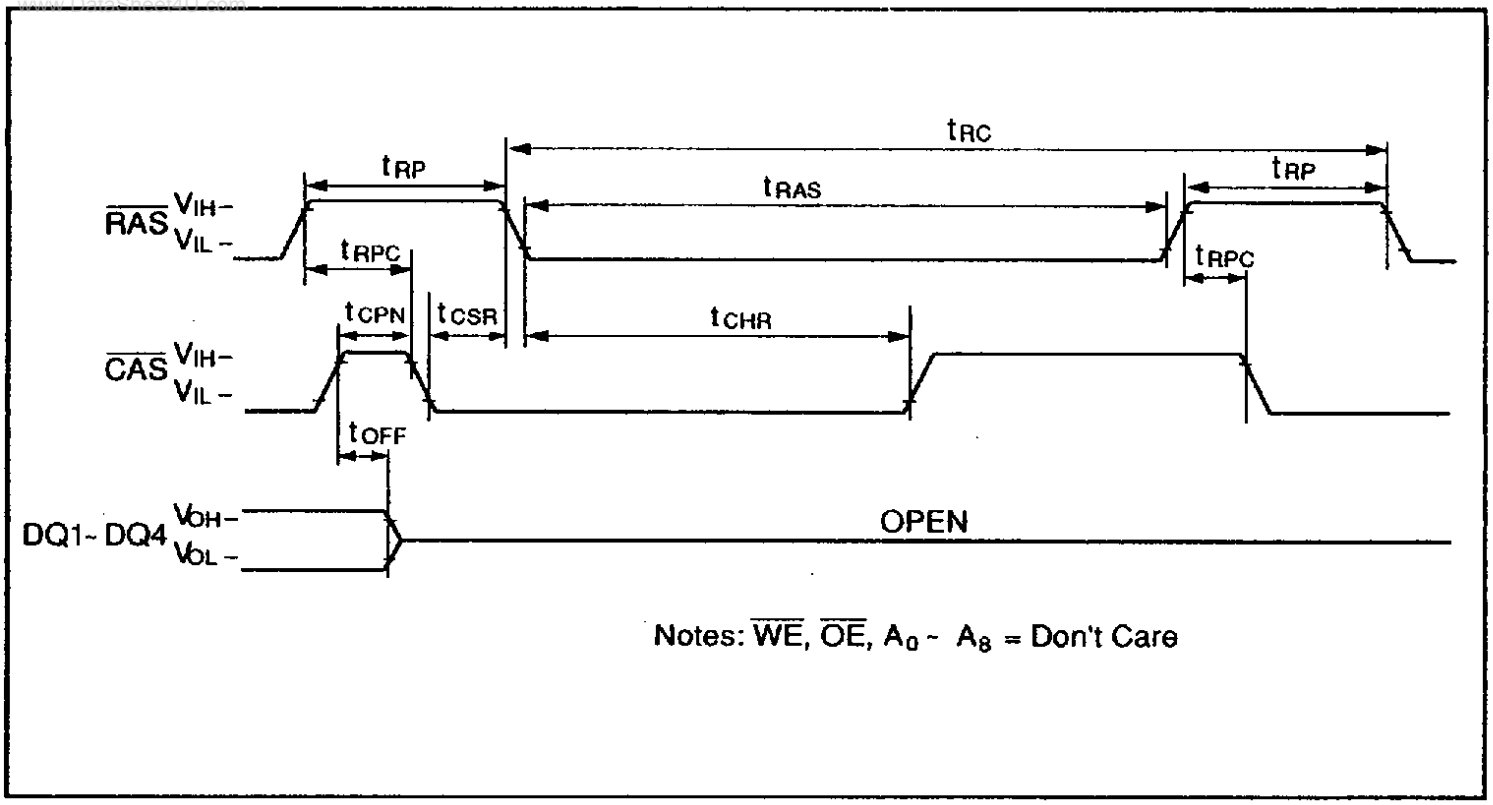


RAS-ONLY REFRESH CYCLE



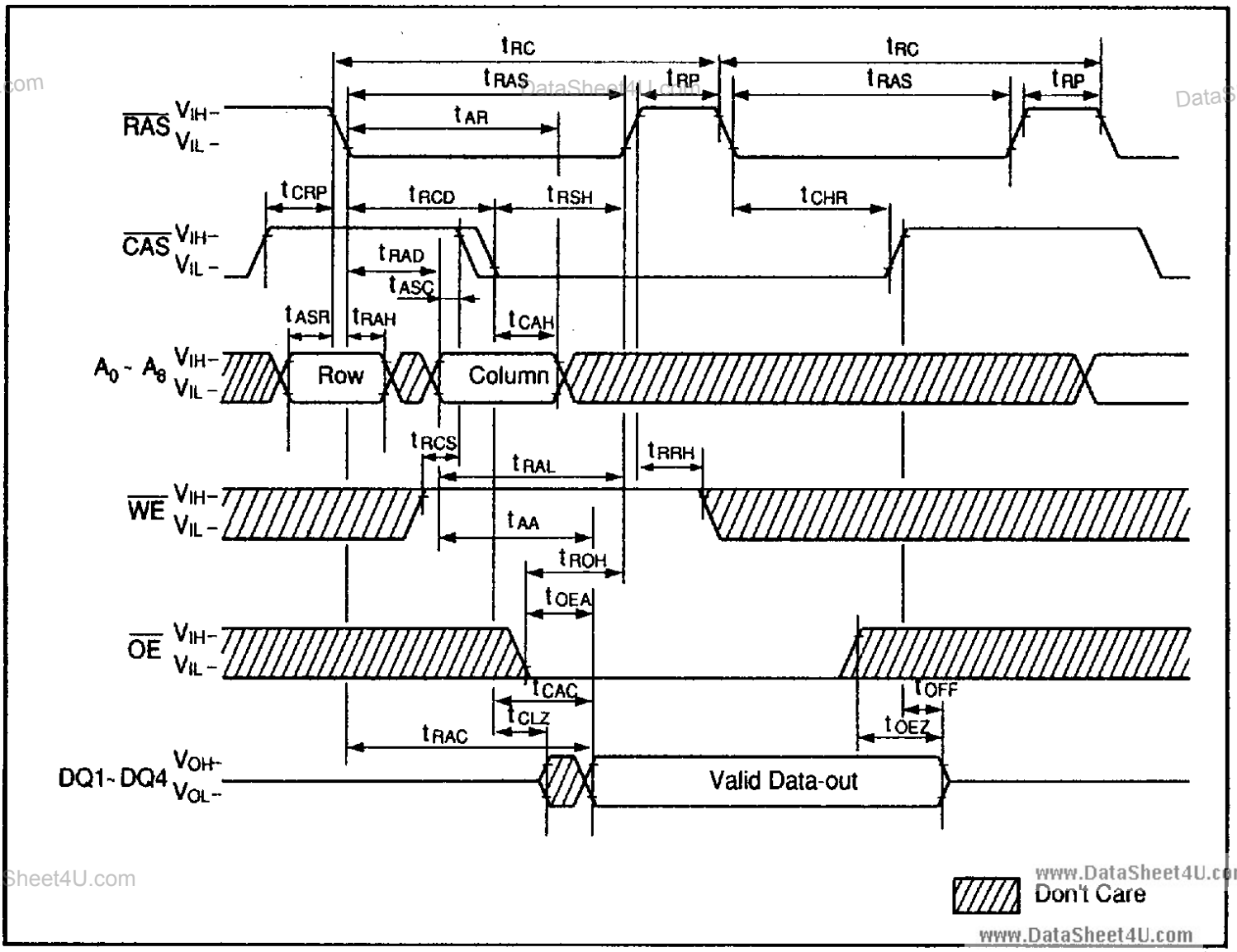
Notes: $\overline{WE}$, $\overline{OE}$ = Don't Care

CAS BEFORE RAS AUTO-REFRESH CYCLE

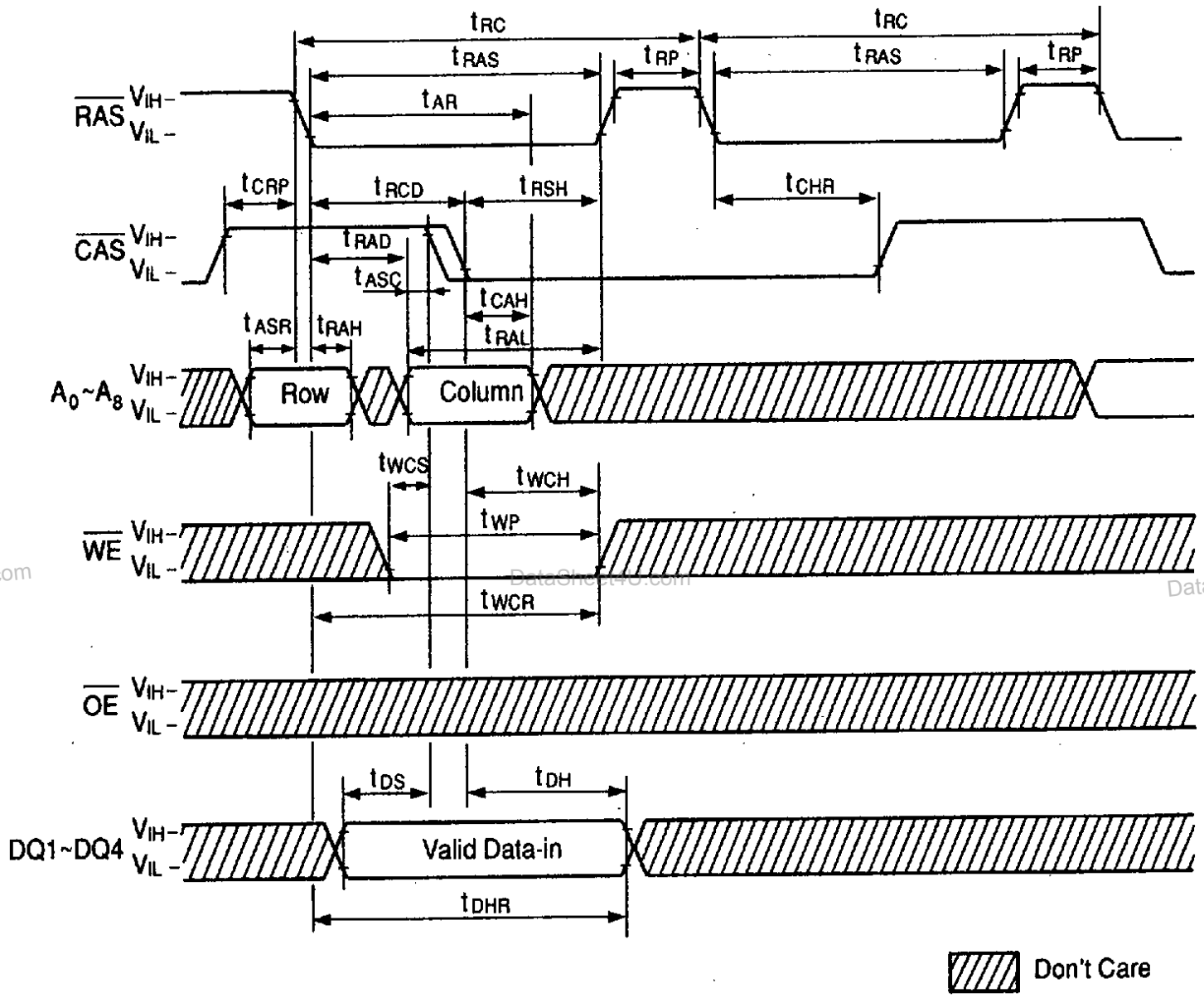


Notes: $\overline{WE}$, $\overline{OE}$, A_0 ~ A_8 = Don't Care

HIDDEN REFRESH READ CYCLE



HIDDEN REFRESH WRITE CYCLE



CAS BEFORE RAS REFRESH COUNTER TEST