



MICROCHIP

27LV512

512K (64K x 8) Low-Voltage CMOS EPROM

FEATURES

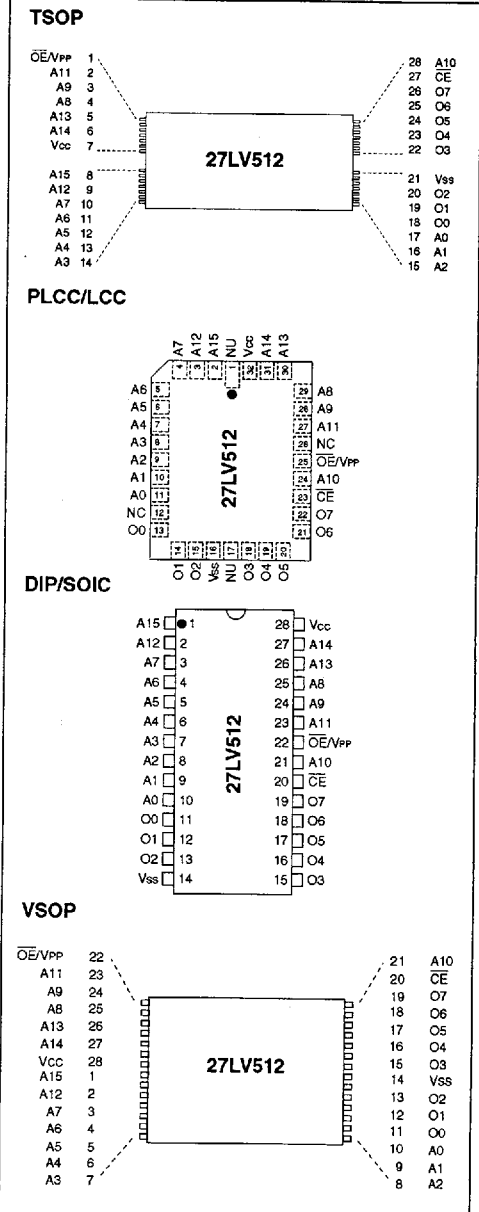
- Wide voltage range 3.0V to 5.5V
- High speed performance
 - 200 ns access time available at 3.0V
- CMOS Technology for low power consumption
 - 12 mA Active current at 3.0V
 - 35 mA Active current at 5.5V
 - 100 μ A Standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID™ aids automated programming
- Separate chip enable and output enable controls
- High speed "Express" programming algorithm
- Organized 64K x 8: JEDEC standard pinouts
 - 28-pin Dual-in-line package
 - 32-pin PLCC package
 - 28-pin SOIC package
 - 28-pin TSOP package
 - 28-pin VSOP package
 - Tape and reel
- Available for the following temperature ranges
 - Commercial: 0°C to +70°C
 - Industrial: -40°C to +85°C

DESCRIPTION

The Microchip Technology Inc. 27LV512 is a low-voltage (3.0 volt) CMOS EPROM designed for battery powered applications. The device is organized as a 64K x 8 (64K-Byte) non-volatile memory product. The 27LV512 consumes only 12 mA maximum of active current during a 3.0 volt read operation therefore improving battery performance. This device is designed for very low-voltage applications where conventional 5.0 volt only EPROMs can not be used. Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 200 ns at 3.0 volts. This device allows systems designers the ability to use low voltage non-volatile memory with today's low-voltage microprocessors and peripherals in battery powered applications.

A complete family of packages is offered to provide the most flexibility in applications. For surface mount applications, PLCC, SOIC or TSOP packaging is available. Tape and reel packaging is also available for PLCC or SOIC packages.

PACKAGE TYPE



1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC and input voltages w.r.t. VSS -0.6V to +7.25V

VPP voltage w.r.t. VSS during programming -0.6V to +14.0V

Voltage on A9 w.r.t. VSS -0.6V to +13.5V

Output voltage w.r.t. VSS -0.6V to VCC +1.0V

Storage temperature -65°C to +150°C

Ambient temp. with power applied -65°C to +125°C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0-A15	Address Inputs
\overline{CE}	Chip Enable
\overline{OE}/V_{PP}	Output Enable/Programming Voltage
O0 - O7	Data Output
VCC	+3.0V To +5.5V Power Supply
VSS	Ground
NC	No Connection; No Internal Connection
NU	Not Used; No External Connection Is Allowed

TABLE 1-2: READ OPERATION DC CHARACTERISTICS

VCC = 3.0V to 5.5V unless otherwise specified								
Commercial: Tamb = 0°C to +70°C								
Industrial: Tamb = -40°C to +85°C								
Parameter	Part*	Status	Symbol	Min.	Max.	Units	Conditions	
Input Voltages	all	Logic "1"	V _{IH}	2.0	V _{CC} +1	V		
		Logic "0"	V _{IL}	-0.5	0.8	V		
Input Leakage	all		I _{LI}	-10	10	μA	V _{IN} = 0 to V _{CC}	
Output Voltages	all	Logic "1"	V _{OH}	2.4		V	I _{OH} = -400 μA I _{OL} = 2.1 mA	
		Logic "0"	V _{OL}		0.45	V		
Output Leakage	all	—	I _{LO}	-10	10	μA	V _{OUT} = 0V to V _{CC}	
Input Capacitance	all	—	C _{IN}	—	6	pF	V _{IN} = 0V; Tamb = 25°C; f = 1 MHz	
Output Capacitance	all	—	C _{OUT}	—	12	pF	V _{OUT} = 0V; Tamb = 25°C; f = 1 MHz	
Power Supply Current, Active	C I	TTL input	I _{CC1}	—	35@5.0V 12@3.0V	mA	V _{CC} = 5.5V f = 1 MHz; \overline{OE}/V_{PP} = \overline{CE} = V _{IL} ; I _{OUT} = 0 mA; V _{IL} = -0.1 to 0.8V; V _{IH} = 2.0 to V _{CC} ; Note 1	
		TTL input	I _{CC2}	—	45@5.0V 12@3.0V	mA		
Power Supply Current, Standby	C I all	TTL input	I _{CC(S)TLL}	—	1@3.0V	mA	CE = V _{CC} ± 0.2V	
		TTL input	I _{CC(S)TLL}	—	2@3.0V	mA		
		CMOS input	I _{CC(S)CMOS}	—	100@3.0V	μA		

* Parts: C=Commercial Temperature Range; I=Industrial Temperature Range

Note 1: Typical active current increases .75 mA per MHz up to operating frequency for all temperature ranges.

TABLE 1-3: READ OPERATION AC CHARACTERISTICS

Parameter	Sym	27LV512-20		27LV512-25		27LV512-30		Units	Conditions
		Min	Max	Min	Max	Min	Max		
Address to Output Delay	t _{ACC}	—	200	—	250	—	300	ns	$\overline{CE} = \overline{OE} = V_{IL}$
\overline{CE} to Output Delay	t _{CE}	—	200	—	250	—	300	ns	$\overline{OE} = V_{IL}$
\overline{OE} to Output Delay	t _{OE}	—	90	—	100	—	125	ns	$\overline{CE} = V_{IL}$
\overline{CE} or \overline{OE} to O/P High Impedance	t _{OFF}	0	50	0	50	0	50	ns	
Output Hold from Address \overline{CE} or \overline{OE} , whichever goes first	t _{OH}	0	—	0	—	0	—	ns	

AC Testing Waveform: $V_{IH} = 2.4V$ and $V_{IL} = 0.45V$; $V_{OH} = 2.0V$ and $V_{OL} = 0.8V$
 Output Load: 1 TTL Load + 100 pF
 Input Rise and Fall Times: 10 ns
 Ambient Temperature: Commercial: $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$
 Industrial: $T_{amb} = -40^{\circ}C$ to $+85^{\circ}C$

FIGURE 1-1: READ WAVEFORMS

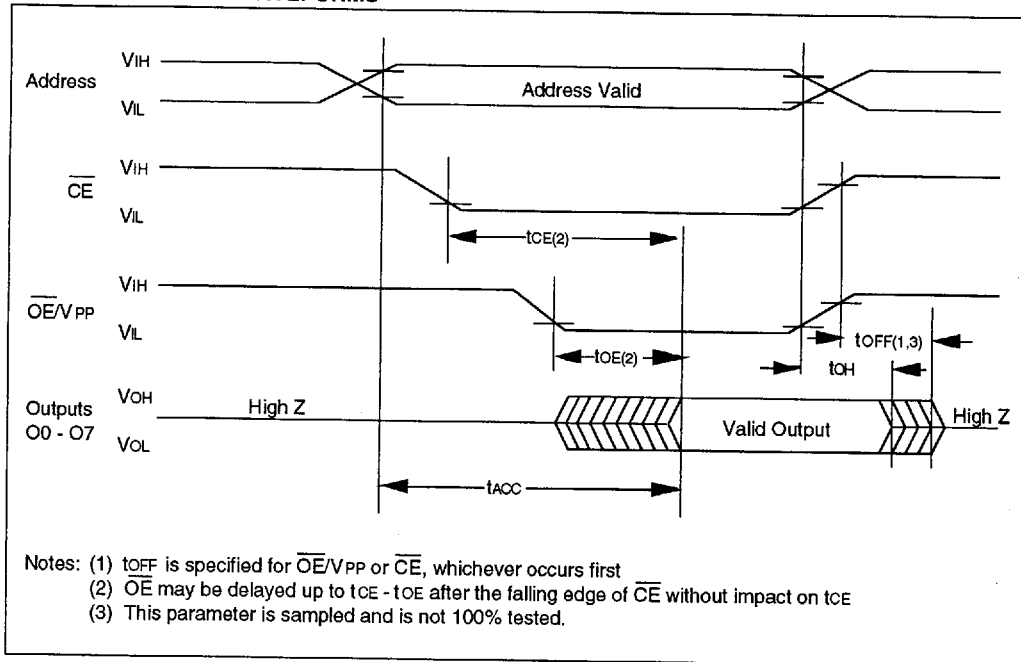


TABLE 1-4: PROGRAMMING DC CHARACTERISTICS

Ambient Temperature: $T_{amb} = 25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ $V_{CC} = 6.5\text{V} \pm 0.25\text{V}$, $\overline{\text{OE}}/V_{PP} = V_H = 13.0\text{V} \pm 0.25\text{V}$						
Parameter	Status	Symbol	Min.	Max.	Units	Conditions (See Note 1)
Input Voltages	Logic "1"	V_{IH}	2.0	$V_{CC}+1$	V	
	Logic "0"	V_{IL}	-0.1	0.8	V	
Input Leakage	—	I_{LI}	-10	10	μA	$V_{IN} = 0\text{V to } V_{CC}$
Output Voltages	Logic "1"	V_{OH}	2.4		V	$I_{OH} = -400\ \mu\text{A}$ $I_{OL} = 2.1\ \text{mA}$
	Logic "0"	V_{OL}	—	0.45	V	
VCC Current, program & verify	—	I_{CC2}	—	35	mA	
$\overline{\text{OE}}/V_{PP}$ Current, program	—	I_{PP2}	—	25	mA	$\overline{\text{OE}} = V_{IL}$
A9 Product Identification	—	V_{ID}	11.5	12.5	V	

Note 1: V_{CC} must be applied simultaneously or before V_{PP} voltage on $\overline{\text{OE}}/V_{PP}$ and removed simultaneously or after the V_{PP} voltage on $\overline{\text{OE}}/V_{PP}$.

TABLE 1-5: PROGRAMMING AC CHARACTERISTICS

for Program, Program Verify and Program Inhibit Modes		AC Testing Waveform: $V_{IH}=2.4\text{V}$ and $V_{IL}=0.45\text{V}$; $V_{OH}=2.0\text{V}$; $V_{OL}=0.8\text{V}$ Ambient Temperature: $T_{amb}=25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ $V_{CC} = 6.5\text{V} \pm 0.25\text{V}$, $\overline{\text{OE}}/V_{PP} = V_H = 13.0\text{V} \pm 0.25\text{V}$				
Parameter	Symbol	Min.	Max.	Units	Remarks	
Address Set-Up Time	t_{AS}	2	—	μs		
Data Set-Up Time	t_{DS}	2	—	μs		
Data Hold Time	t_{DH}	2	—	μs		
Address Hold Time	t_{AH}	0	—	μs		
Float Delay (2)	t_{DF}	0	130	ns		
VCC Set-Up Time	t_{VCS}	2	—	μs		
Program Pulse Width (1)	t_{PW}	95	105	μs	100 μs typical	
$\overline{\text{OE}}$ Set-Up Time	t_{CES}	2	—	μs		
$\overline{\text{OE}}$ Set-Up Time	t_{OES}	2	—	μs		
$\overline{\text{OE}}$ Hold Time	t_{OEH}	2	—	μs		
$\overline{\text{OE}}$ Recovery Time	t_{OR}	2	—	μs		
$\overline{\text{OE}}/V_{PP}$ Rise Time During Programming	t_{PRT}	50	—	ns		

Note 1: For express algorithm, initial programming width tolerance is 100 $\mu\text{s} \pm 5\%$.

Note 2: This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

FIGURE 1-2: PROGRAMMING WAVEFORMS

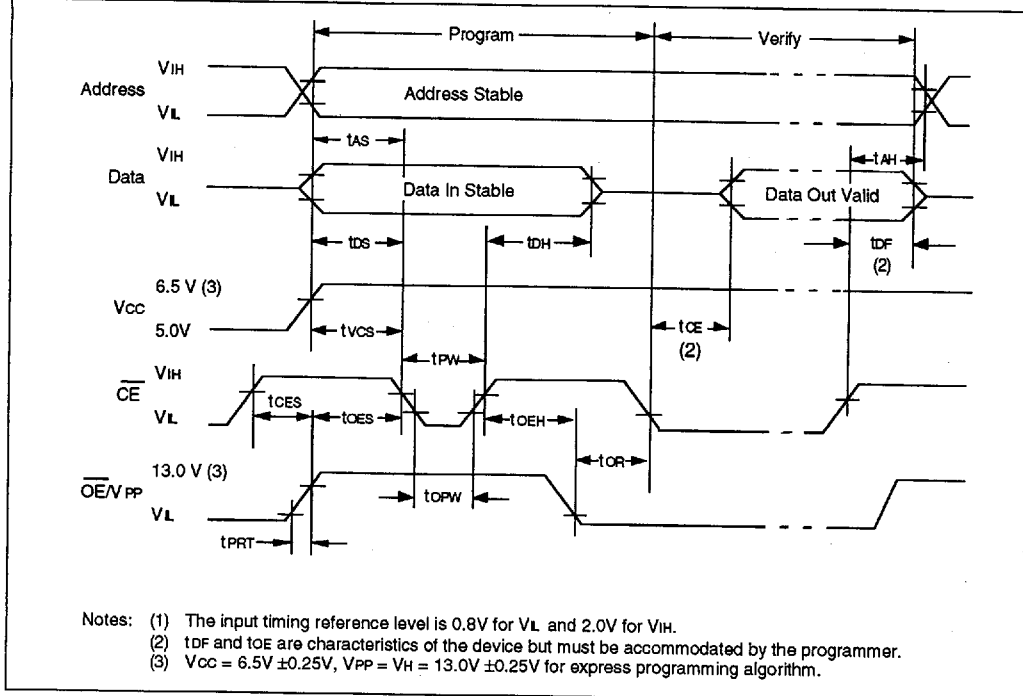


TABLE 1-6: MODES

Operation Mode	CE	OE/VPP	A9	O0 - O7
Read	V _L	V _L	X	DOUT
Program	V _L	V _H	X	DIN
Program Verify	V _L	V _L	X	DOUT
Program Inhibit	V _{IH}	V _H	X	High Z
Standby	V _{IH}	X	X	High Z
Output Disable	V _L	V _{IH}	X	High Z
Identity	V _L	V _L	V _H	Identity Code

X = Don't Care

1.2 Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when

- the \overline{CE} pin is low to power up (enable) the chip
- the $\overline{OE/VPP}$ pin is low to gate the data to the output pins.

For Read operations, if the addresses are stable, the address access time (t_{ACC}) is equal to the delay from \overline{CE} to output (t_{CE}). Data is transferred to the output after a delay (t_{OE}) from the falling edge of $\overline{OE/VPP}$.

1.3 Standby Mode

The standby mode is defined when the \overline{CE} pin is high and a program mode is not identified.

1.4 Output Enable \overline{OE}/V_{PP}

This multifunction pin eliminates bus connection in microprocessor based systems in which multiple devices may drive the bus. The outputs go into a high impedance state when:

- the \overline{OE}/V_{PP} pin is high (V_{IH}).

When a V_H input is applied to this pin, it supplies the programming voltage (V_{PP}) to the device.

1.5 Programming Mode

The Express algorithm has been developed to improve on the programming throughput times in a production environment. Up to ten 100-microsecond pulses are applied until the byte is verified. A flowchart of the Express algorithm is shown in Figure 1-3.

Programming takes place when:

- V_{CC} is brought to the proper voltage,
- \overline{OE}/V_{PP} is brought to the proper V_H level, and
- \overline{CE} line is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0 - A15 and the data to be programmed is presented to pins O0 - O7. When data and address are stable, a low going pulse on the \overline{CE} line programs that location.

1.6 Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

- V_{CC} is at the proper level,
- the \overline{OE}/V_{PP} pin is low, and
- the \overline{CE} line is low.

1.7 Inhibit

When programming multiple devices in parallel with different data, only \overline{CE} needs to be under separate control to each device. By pulsing the \overline{CE} line low on a particular device, that device will be programmed; all other devices with \overline{CE} held high will not be programmed with the data (although address and data will be available on their input pins).

1.8 Identity Mode

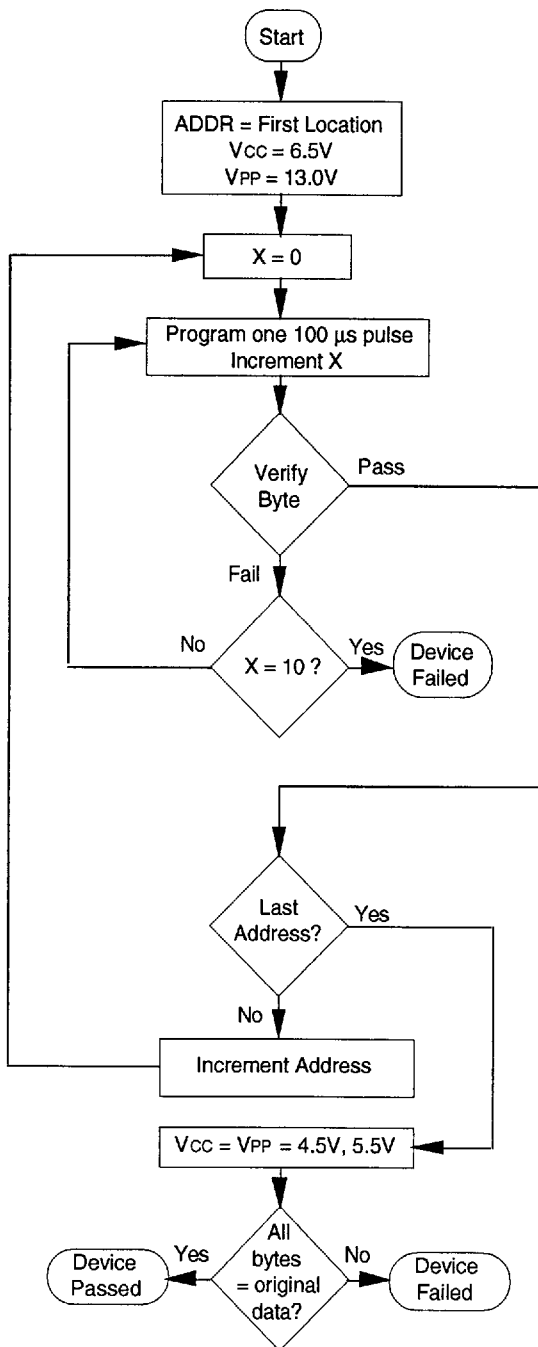
In this mode specific data is output which identifies the manufacturer as Microchip Technology Inc. and the device type. This mode is entered when Pin A9 is taken to V_H (11.5V to 12.5V). The \overline{CE} and \overline{OE}/V_{PP} lines must be at V_{IL} . A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin →	Input	Output									
		A0	07	06	05	04	03	02	01	00	Hex
Identity ↓	A0	0	0	1	0	1	0	0	1	0	29
Manufacturer	V_{IL}	0	0	1	0	1	0	0	1	29	
Device Type*	V_{IH}	0	0	0	0	1	1	0	1	0D	

* Code subject to change

FIGURE 1-3: PROGRAMMING EXPRESS ALGORITHM

Conditions:
 $T_{amb} = 25^{\circ}\text{C} \pm 5^{\circ}\text{C}$
 $V_{CC} = 6.5 \pm 0.25\text{V}$
 $V_{PP} = 13.0 \pm 0.25\text{V}$



27LV512

27LV512 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

