TMM24256AP/AF 32,763 WORD × 8 BIT
ONE TIME PROGRAMMABLE READ ONLY MEMORY
SILICON STACKED GATE MOS

TMM24256AP/AF

DESCRIPTION

The TMM24256AP/AF is a 32,768 word × 8 bit one time programmable read only memory, and molded in a 28 pin plastic Package.

The TMM24256AP/AF's access time is 200ns and has low power standby mode which reduces the power dissipation without increasing access time.

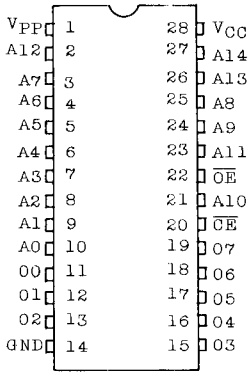
The electrical characteristics and programming method are the same as U.V. EPROM TMM27256AD's.

Once programmed, the TMM24256AP/AF can not be erased because of using plastic DIP without transparent window.

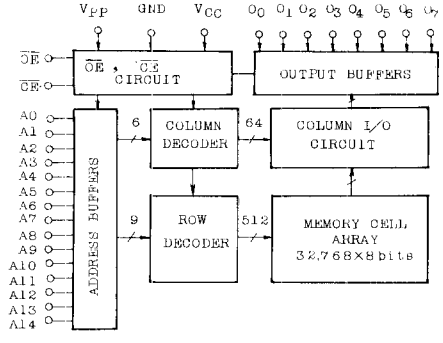
FEATURES

- Fast access time : 200ns
- Low power dissipation
  Active : 100mA
  Standby : 30mA
- Single 5V power supply
- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with ROM TC53257P, TMM23256P, EPROM TMM27256D/AD and TC57256D
- Standard 28 pin DIP plastic package : TMM24256AP
- Plastic Flat Package : TMM24256AF

PIN CONNECTION



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_{14}$	Address Inputs
$O_0 \sim O_7$	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{PP}	Program Supply Voltage
V_{CC}	Power Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	$O_0 \sim O_7$ (11~13, 15~19)	POWER
Read	L	L	5V	5V	Data Out	Active
Output Deselect	*	H			High Impedance	
Standby	H	*			High Impedance	Standby
Program	L	H	12.5V	6V	Data In	Active
Program Inhibit	H	H			High Impedance	
Program Verify	*	L			Data Out	

* H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~14.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
$V_{I/O}$	Input/Output Voltage	−0.6~7.0	V
P_D	Power Dissipation	1.0/0.6*	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
T_{STG}	Storage Temperature	−55~150	°C
T_{OPR}	Operating Temperature	0~70	°C

* : Plastic Flat Package

READ OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.00	5.25	V
V_{PP}	V_{PP} Power Supply Voltage	2.0	V_{CC}	V_{CC}+0.6	V

D. C. and OPERATING CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±5%,)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}	—	—	±10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE}$=V_{IH}	—	—	30	mA
I_{CC2}	Supply Current (Active)	$\overline{CE}$=V_{IL}	—	—	100	mA
V_{OH}	Output High Voltage	I_{OH}=−400μA	2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	—	—	0.4	V
I_{PP1}	V_{PP} Current	V_{PP}=0~V_{CC}+0.6V	—	—	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4V~V_{CC}	—	—	±10	μA

A. C. CHARACTERISTICS

(T_a = 0 ~ 70°C, V_{CC} = 5V ± 5%, V_{PP} = 2.0V ~ V_{CC} + 0.6V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
t_{ACC}	Address Access Time	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE}$ = V_{IL}	–	200	ns
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}$ = V_{IL}	–	70	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}$ = V_{IL}	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$ = V_{IL}	0	60	ns
t_{OH}	Output Data Hold Time	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0	–	ns

A. C. TEST CONDITIONS

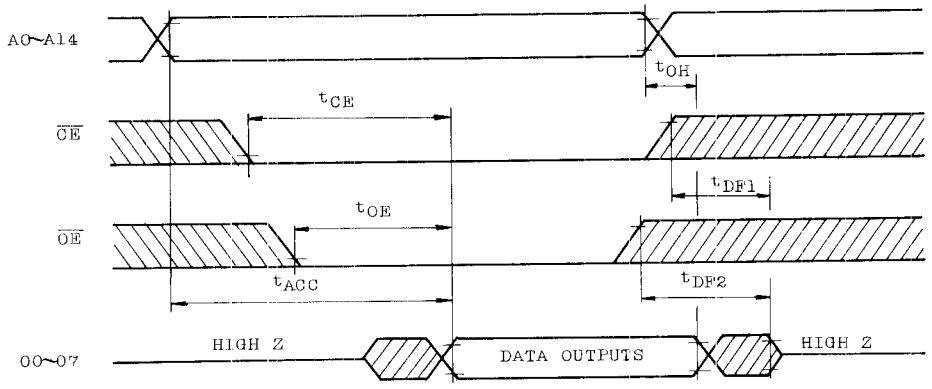
- Output Load : 1 TTL Gate and C_L = 100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

CAPACITANCE * (T_a = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	–	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	–	8	12	pF

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



High speed PROGRAM OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	—	$V_{CC}+1.0$	V
V_{IL}	Input Low Voltage	-0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	V

D. C. and OPERATING CHARACTERISTICS

($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0\sim V_{CC}$	—	—	±10	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	120	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=13.0V$	—	—	50	mA

A. C. PROGRAMMING CHARACTERISTICS

($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	0	—	—	ns
t_{CEH}	$\overline{CE}$ Hold Time	—	0	—	—	ns
t_{OES}	$\overline{OE}$ Setup Time	—	2	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VPS}	V_{PP} Setup Time	—	2	—	—	μs
t_{VCS}	V_{CC} Setup Time	—	2	—	—	μs
t_{PW}	Initial Program Pulse Width	$\overline{CE}=V_{IL}$, $\overline{OE}=V_{IH}$	0.95	1.0	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	2.85	3.0	78.75	ms
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IH}$	—	—	150	ns
t_{DFP}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IH}$	—	—	130	ns

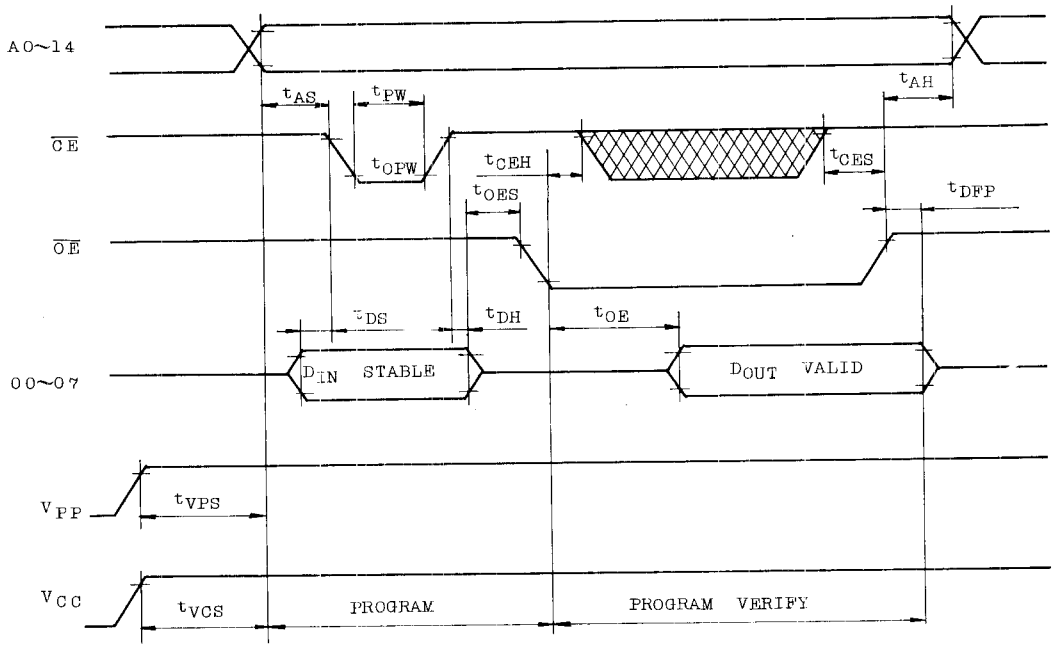
A. C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L(100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note 1 : The length of the overprogram pulse may very as a fumction of the counter value X.

TIMING WAVEFORMS (HIGH SPEED PROGRAM)

(V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.5V)



Note : 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.
2. Removing the device from socket and setting the device in socket with V_{PP} = 12.5V may cause permanent damage to the device.
3. The V_{PP} supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the V_{PP} terminal.
When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

OPERATION INFORMATION

The TMM24256AP/AF's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN NAMES(NUMBER)		$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	$O_0 \sim O_7$ (11~13, 15~19)	POWER
Read Operation (Ta=0~70°C)	Read	L	L	5V	5V	Data Out	Active
	Output Deselect	*	H			High Impedance	Active
	Standby	H	*			High Impedance	Standby
Program Operation (Ta=25±5°C)	Program	L	H	12.5V	6V	Data In	Active
	Program Inhibit	H	H			High Impedance	Active
	Program Verify	*	L			Data Out	Active

Note : H ; V_{IH}, L ; V_{IL}, * ; V_{IH} or V_{IL}

READ MODE

The TMM24256AP/AF has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) control the output buffers, independent of device selection.

Assuming the $\overline{CE}=\overline{OE}=V_{IL}$, the output data is valid at the outputs after address access time from stabilizing of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}=V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in a high impedance state. So two or more TMM24256AP/AF's can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM24256AP/AF has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TMM24256AP/AF is placed in the standby mode which reduce the operating current to 30mA from 100mA (about 70% reduction) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ at V_{IL} and $\overline{CE}$ at V_{IH} or V_{IL}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to V_{PP} terminal, a TTL high level $\overline{CE}$ input inhibits the TMM24256AP/AF from being programmed.

Programming of two or more TMM24256AP/AF's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGMAMMING MODE

The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the V_{PP} terminal with V_{CC}=6V.

The programming is achieved by applying a single TTL low level 1ms pulse the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, the additional program pulse with pulse width 3 times that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with V_{CC}=V_{PP}=5V.

ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TMM24256AP/AF which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TMM24256AP/AF by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

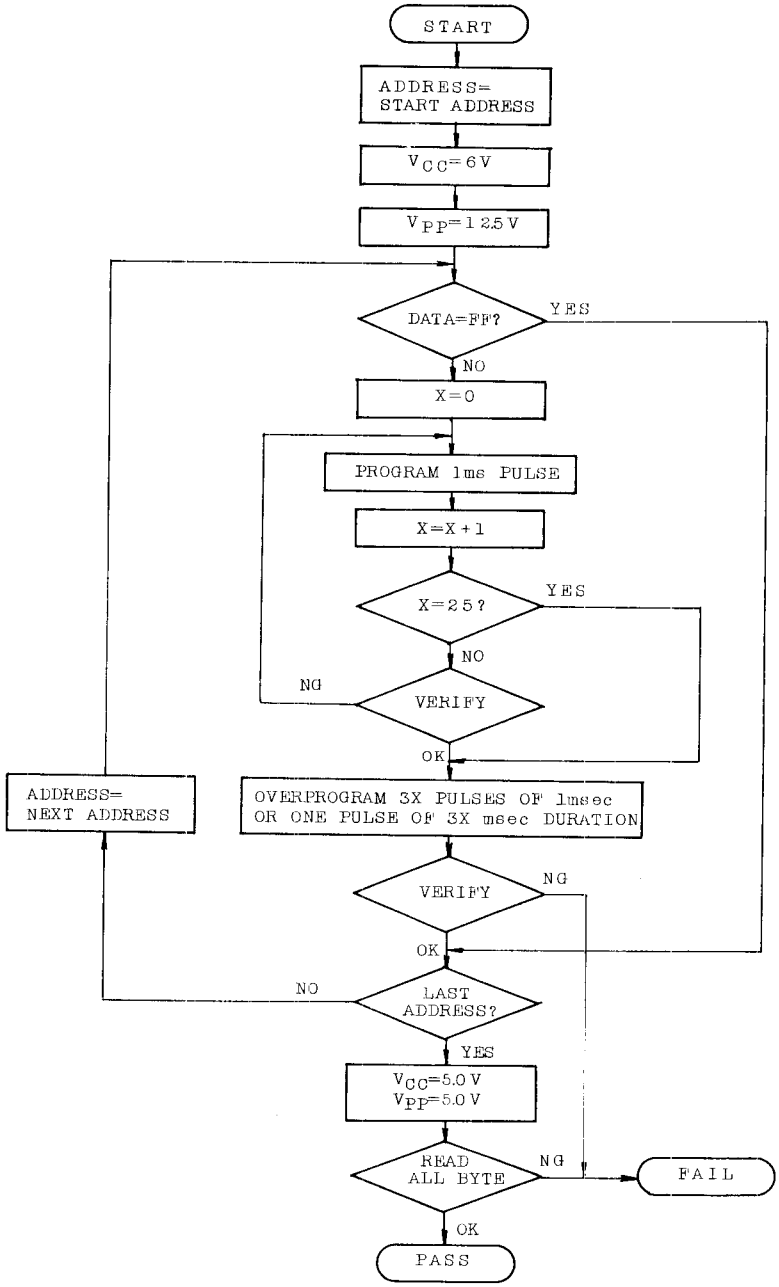
Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (O7).

The following table shows electric signature of TMM24256AP/AF.

PINS / SIGNATURE	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	0	1	0	1	0	1	0	0	54

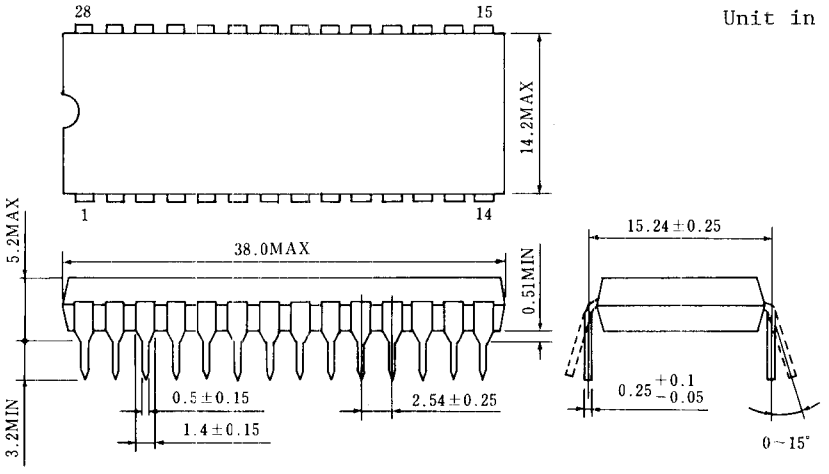
Notes: A9=12V±0.5V
A1~A8, A10~A14, $\overline{CE}$, $\overline{OE}$=V_{IL}

HIGH SPEED PROGRAM MODE FLOW CHART



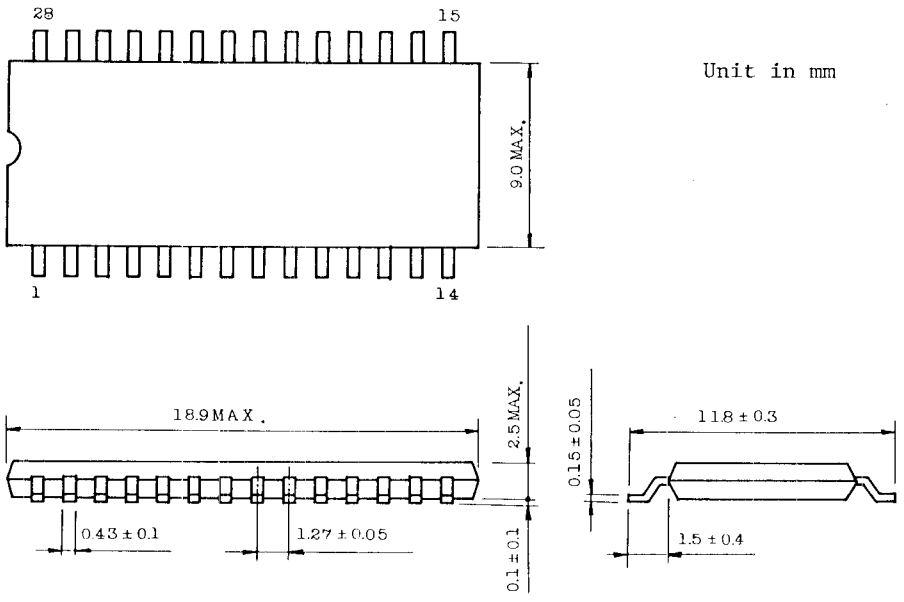
OUTLINE DRAWINGS (TMM24256AP)

Unit in mm



Note : 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in millimeters.

OUTLINE DRAWINGS (TMM24256AF)



Unit in mm

Note: Lead picth is 1.27 and to erance is±0.12 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.