National Semiconductor

August 1996

NM25C040
4096-Bit Serial CMOS EEPROM
(Serial Peripheral Interface (SPI™) Synchronous Bus)

NM25C040 4096-Bit Serial CMOS EEPROM (Serial Peripheral Interface (SPI) Synchronous Bus)

General Description

The NM25C040 is a 4096-bit serial interface CMOS EEPROM with a SPI compatible serial interface. The NM25C040 is designed for data storage in applications requiring both nonvolatile memory and in-system data updates. This EEPROM is well suited for applications using the 68HC11 series of microcontrollers that support the SPI interface for high speed communication with peripheral devices via a serial bus to reduce pin count. The NM25C040 is implemented in National Semiconductor's floating gate CMOS process that provides superior endurance and data retention.

The serial data transmission of this device requires four signal lines to control the device operation: Chip Select ($\overline{CS}$), Clock (SCK), Serial Data In (SI), and Serial Data Out (SO). All programming cycles are completely self-timed and do not require an erase before WRITE.

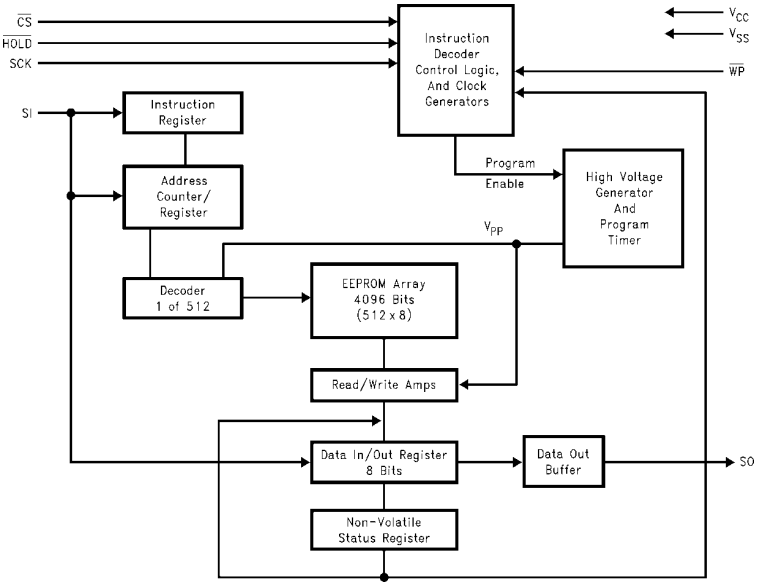
BLOCK WRITE protection is provided by programming the STATUS REGISTER with one of four levels of write protection. Additionally separate write enable and write disable instructions are provided for data protection.

Hardware data protection is provided by the $\overline{WP}$ pin to protect against accidental data changes. The $\overline{HOLD}$ pin allows the serial communications to be suspended without resetting the serial sequence.

Features

- 2.1 MHz clock rate
- 4096 bits organized as 512 x 8
- Multiple chips on the same 3-wire bus with separate chip select lines
- Self-timed programming cycle
- Simultaneous programming of 1 to 4 bytes at a time
- Status register can be polled during programming to monitor READY/BUSY
- Write Protect ($\overline{WP}$) pin and write disable instruction for both hardware and software write protection
- Block write protect feature to protect against accidental writes
- Endurance: 10^6 data changes
- Data retention greater than 40 years
- Packages available: 8-pin DIP, 8-pin SO or 8-pin TSSOP

Block Diagram



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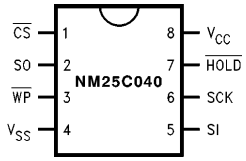
SPI™ is a trademark of Motorola, Inc.

Connection Diagrams

Dual-In-Line Package (N), SO Package (M8) and TSSOP Package (MT8)



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Top View
See NS Package Number
N08E (N), M08A (M8) and MTC08 (MT8)

Pin Names

$\overline{CS}$	Chip Select Input
SO	Serial Data Output
$\overline{WP}$	Write Protect
V_{SS}	Ground
SI	Serial Data Input
SCK	Serial Clock Input
$\overline{HOLD}$	Suspends Serial Input
V_{CC}	Power Supply

Ordering Information

Commercial Temperature Range (0°C to +70°C)

Order Number
NM25C040N/LN/LZN NM25C040M8/LM8/LZM8 NM25C040MT8/LMT8/LZMT8

Extended Temperature Range (−40°C to +85°C)

Order Number
NM25C040EN/LEN/LZEN NM25C040EM8/LEM8/LZEM8 NM25C040EMT8/LEMT8/LZEMT8

Automotive Temperature Range (−40°C to +125°C)

Order Number
NM25C040VN/LVN/LZVN NM25C040VM8/LVM8/LZVM8 NM25C040VMT8/LVMT8/LZVMT8

Standard Voltage 4.5 ≤ V_{CC} ≤ 5.5V Specifications

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM25C040	0°C to +70°C
NM25C040E	−40°C to +85°C
NM25C040V	−40°C to +125°C
Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics 4.5V ≤ V_{CC} ≤ 5.5V unless otherwise specified

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC}	Operating Current	NM25C040	$\overline{CS} = V_{IL}$		3	mA
I_{CCSB}	Standby Current		$\overline{CS} = V_{CC}$		50	μA
I_{IL}	Input Leakage		V_{IN} = 0 to V_{CC}	−1	+1	μA
I_{OL}	Output Leakage	NM25C040	V_{OUT} = GND to V_{CC}	−1	+1	μA
V_{IL}	Input Low Voltage			−0.3	0.3*V_{CC}	V
V_{IH}	Input High Voltage			0.7*V_{CC}	V_{CC} +0.3	V
V_{OL}	Output Low Voltage	NM25C040	I_{OL} = 1.6 mA		0.4	V
V_{OH}	Output High Voltage		I_{OH} = −0.8 mA	V_{CC} − 0.8		V
f_{OP}	SCK Frequency	NM25C040 NM25C040E			2.1 1	MHz
t_{RI}	Input Rise Time				2.0	μs
t_{FI}	Input Fall Time				2.0	μs
t_{CLH}	Clock High Time	NM25C040 NM25C040E	(Note 2)	190 410		ns

DC and AC Electrical Characteristics $4.5V \leq V_{CC} \leq 5.5V$ unless otherwise specified (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{CLL}	Clock Low Time	NM25C040	(Note 2)	190		ns
t_{CSH}	Minimum $\overline{CS}$ High Time	NM25C040	(Note 3)	240		ns
t_{CSS}	$\overline{CS}$ Setup Time Time	NM25C040		240		ns
t_{DIS}	Data Setup Time	NM25C040		100		ns
t_{HDS}	$\overline{HOLD}$ Setup Time			90		ns
t_{CSN}	$\overline{CS}$ Hold Time	NM25C040		240		ns
t_{DIN}	Data Hold Time			100		ns
t_{HDN}	$\overline{HOLD}$ Hold Time			90		ns
t_{PD}	Output Delay	NM25C040	$C_L = 200$ pF		240	ns
t_{LZ}	$\overline{HOLD}$ Output Low Z	NM25C040			100	ns
t_{DF}	Output Disable Time	NM25C040	$C_L = 200$ pF		240	ns
t_{HZ}	$\overline{HOLD}$ to Output High Z	NM25C040			100	ns
t_{WP}	Write Cycle Time		1–4 Bytes		10	ms

Capacitance $T_A = 25°C$, $f = 1$ MHz

Symbol	Test	Type	Max	Units
C_{OUT}	Output Capacitance	3	8	pF
C_{IN}	Input Capacitance	2	6	pF

AC Test Conditions

Output Load	$C_L = 200$ pF
Input Pulse Levels	$0.1 * V_{CC} - 0.9 * V_{CC}$
Timing Measurement Reference Level	$0.3 * V_{CC} - 0.7 * V_{CC}$

Note 1: Stress above those listed under ''Absolute Maximum Ratings'' may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SCK frequency specification specifies a minimum clock period of 476 ns; therefore, in a SCK clock cycle, $t_{CLH} + t_{CLL}$ must be ≥ 476 ns. For example, if $t_{CLL} = 190$ ns, then the minimum $t_{CLH} = 286$ ns in order to meet the SCK frequency specification.

Note 3: $\overline{CS}$ must be brought high for a minimum of 240 ns (t_{CSH}) between consecutive instruction cycles.

Low Voltage 2.7V $\leq V_{CC} \leq$ 5.5V Specifications

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM25C040L	0°C to +70°C
NM25C040LE	−40°C to +85°C
NM25C040LV	−40°C to +125°C
Power Supply (V_{CC})	2.7V to 5.5V

DC and AC Electrical Characteristics 4.5V $\leq V_{CC} \leq$ 5.5V unless otherwise specified

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC}	Operating Current		CS = V_{IL}		3	mA
I_{CCSB}	Standby Current	L LZ	CS = V_{CC}		10 1	μA
I_{IL}	Input Leakage		V_{IN} = 0 to V_{CC}	−1	+1	μA
I_{OL}	Output Leakage		V_{OUT} = GND to V_{CC}	−1	+1	μA
V_{IL}	Input Low Voltage			−0.3	0.3*V_{CC}	V
V_{IH}	Input High Voltage			0.7*V_{CC}	V_{CC} +0.3	V
V_{OL}	Output Low Voltage	NM25C040 NM25C040E	I_{OL} = 0.8 mA		0.4 0.4	V
V_{OH}	Output High Voltage		I_{OH} = −0.4 mA	V_{CC} − 0.8		V
f_{OP}	SCK Frequency				1	MHz
t_{RI}	Input Rise Time				2.0	μs
t_{FI}	Input Fall Time				2.0	μs
t_{CLH}	Clock High Time		(Note 2)	410		ns
t_{CLL}	Clock Low Time		(Note 2)	410		ns
t_{CSH}	Minimum $\overline{CS}$ High Time		(Note 3)	500		ns
t_{CSS}	$\overline{CS}$ Setup Time			500		ns
t_{DIS}	Data Setup Time			100		ns

Capacitance T_A = +25°C, f = 1 MHz

Symbol	Test	Type	Max	Units
C_{OUT}	Output Capacitance	3	8	pF
C_{IN}	Input Capacitance	2	6	pF

AC Conditions of Test

Output Load	C_L = 200 pF
Input Pulse Levels	0.1 * V_{CC} – 0.9 * V_{CC}
Timing Measurement Reference Level	0.3 * V_{CC} – 0.7 * V_{CC}

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Note 2: The SCK frequency specification specifies a minimum clock period of 476 ns; therefore, in an SCK clock cycle t_{CLH} + t_{CLL} must be greater than or equal to 476 ns. For example, if t_{CLL} = 190 ns, then the minimum t_{CLH} = 286 ns in order to meet the SCK frequency specification.

Note 3: $\overline{CS}$ must be brought high for a minimum of 240 ns (t_{CSH}) between consecutive instruction cycles.

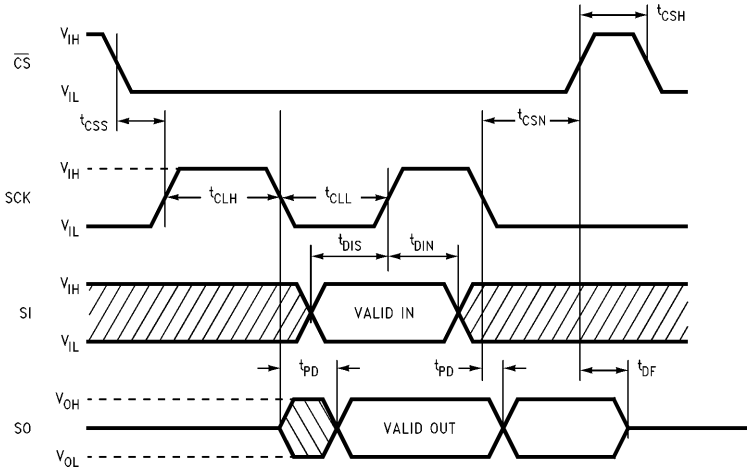

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FIGURE 1. Synchronous Data Timing Diagram

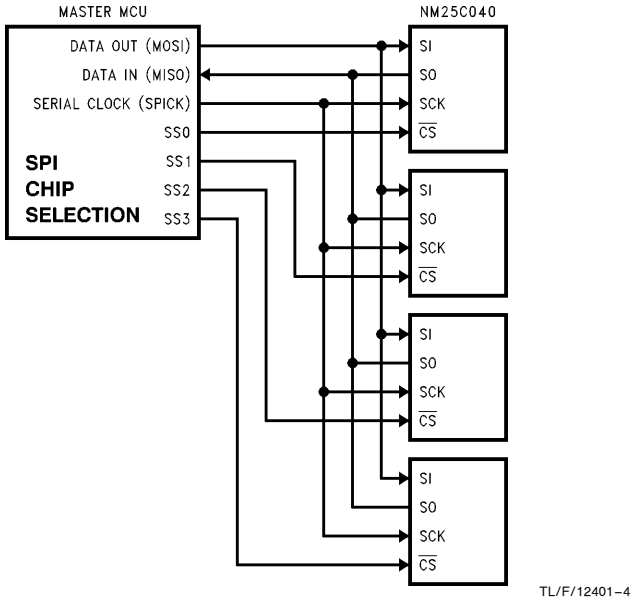

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FIGURE 2. SPI Serial Interface

Note: When connected to the SPI port of a 68HC11 microcontroller, the NM25C040 accepts a clock phase of 0 and a clock parity of 0.

Functional Description

MASTER: The device that generates the serial clock is designated as the master. The NM25C040 can never function as a master.

SLAVE: The NM25C040 always operates as a slave as the serial clock pin is always an input.

TRANSMITTER/RECEIVER: The NM25C040 has separate pins for data transmission (SO) and reception (SI).

MSB: The Most Significant Bit is the first bit transmitted and received.

CHIP SELECT: The chip is selected when pin $\overline{CS}$ is low. When the chip is not selected, data will not be accepted from pin SI, and the output pin SO is in high impedance.

SERIAL OP-CODE: The first byte transmitted after the chip is selected with $\overline{CS}$ going low contains the opcode that defines the operation to be performed. In the READ and WRITE instructions the op-code also contains address bit A8.

PROTOCOL: When connected to the SPI port of a 68HC11 microcontroller, the NM25C040 accepts a clock phase of 0 and a clock polarity of 0. The SPI protocol for this device defines the byte transmitted on the SI and SO data lines for proper chip operation. See *Figure 3*.

HOLD: The $\overline{Hold}$ pin is used in conjunction with the $\overline{CS}$ to select the device. Once the device is selected and a serial sequence is underway, $\overline{HOLD}$ may be forced low to suspend further serial communication with the device without resetting the serial sequences. Note that $\overline{HOLD}$ must be brought low while the SCK pin is low. The device must remain selected during this sequence. To resume serial communication $\overline{HOLD}$ is brought high while the SCK pin is low. Pins SI, SCK, and SO are at a high impedance state during $\overline{HOLD}$. See *Figure 4.*

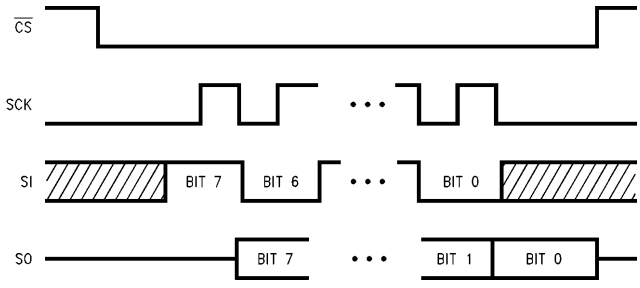

FIGURE 3. SPI Protocol

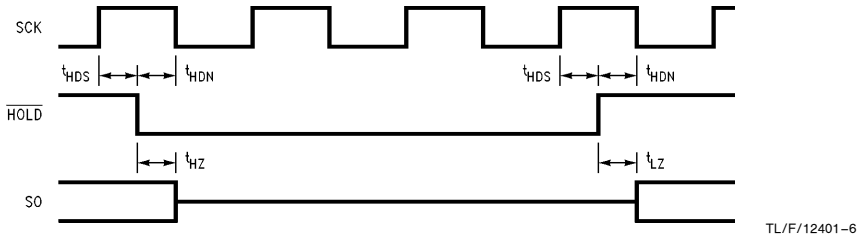

FIGURE 4. $\overline{HOLD}$ Timing

Functional Description (Continued)

TABLE I

Instruction Name	Instruction Format	Operation
WREN	0000X110	Set Write Enable Latch
WRDI	0000X100	Reset Write Enable Latch
RDSR	0000X101	Read Status Register
WRSR	0000X001	Write Status Register
READ	0000A011	Read Data from Memory Array
WRITE	0000A010	Write Data to Memory Array

Note: "A" represents MSB address bit A8.
"X" = don't care.

INVALID OP-CODE: After an invalid code is received, no data is shifted into the NM25C040, and the SO data output pin remains high impedance until new $\overline{CS}$ falling edge re-initializes the serial communication. See *Figure 5*.

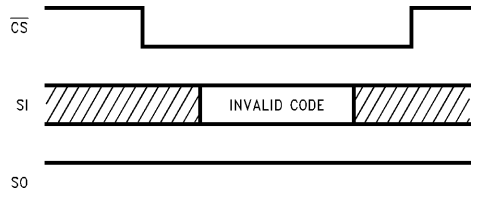

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FIGURE 5. Invalid Op-Code

READ SEQUENCE (One or More Bytes): Reading the memory via the SPI link requires the following sequence. The $\overline{CS}$ line is pulled low to select the device. The READ op-code (which includes A8) is transmitted on the SI line followed by the byte address (A7–A0) to be read. After this is done, data on the SI line becomes don't care. The data (D7–D0) at the address specified is then shifted out on the SO line. If only one byte is to be read, the $\overline{CS}$ line can be pulled back to the high level. It is possible to continue the READ sequence as the byte address is automatically incremented and data will continue to be shifted out. When the highest address is reached (1FF), the address counter rolls over to lowest address (000) allowing the entire memory to be read in one continuous READ cycle. See *Figure 6*.

READ STATUS REGISTER (RDSR): The Read Status Register (RDSR) instruction provides access to the status register which is used to interrogate the READY/BUSY and WRITE ENABLE status of the chip, Two nonvolatile status register bits are used to select one of our levels of BLOCK WRITE PROTECTION. The status register format is shown in Table II.

TABLE II. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	1	1	BP1	BP0	WEN	$\overline{RDY}$

Status register Bit 0 = 0 ($\overline{RDY}$) indicates that the device is READY; Bit 0 = 1 indicates that a program cycle is in progress. Bit 1 = 0 (WEN) indicates that the device is not WRITE ENABLED; Bit 1 = 1 indicates that the device is WRITE ENABLED. Nonvolatile status register Bits 2 and 3 (BP0 and BP1) indicate the level of BLOCK WRITE PROTECTION selected. The block write protection levels and corresponding status register control bits are shown in Table III. Note that if a RDSR instruction is executed during a programming cycle only the $\overline{RDY}$ bit is valid. All other bits are 1s. See *Figure 7*.

TABLE III. Block Write Protection Levels

Level	Status Register Bits		Array Addresses
	BP1	BP0	Protected
0	0	0	None
1	0	1	180–1FF
2	1	0	100–1FF
3	1	1	000–1FF

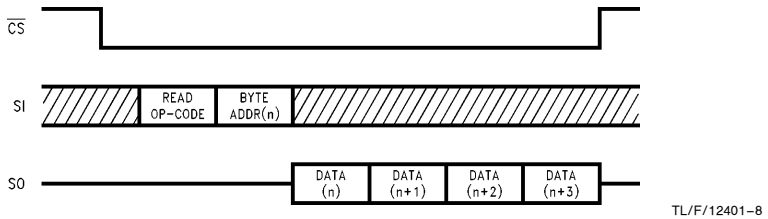

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FIGURE 6. Read Sequence

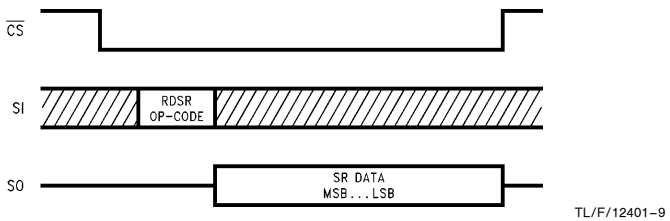

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FIGURE 7. Read Status

Functional Description (Continued)

WRITE ENABLE (WREN): When V_{CC} is applied to the chip it ''powers up'' in the write disable state. Therefore, all programming modes must be preceded by a WRITE ENABLE (WREN) instruction. Additionally the $\overline{WP}$ pin must be held high during a WRITE ENABLE instruction. At the completion of a WRITE or WRSR cycle the device is automatically returned to the write disable state. Note that a WRITE DISABLE (WRDI) instruction or forcing the $\overline{WP}$ pin low will also return the device to the write disable state. See *Figure 8*.

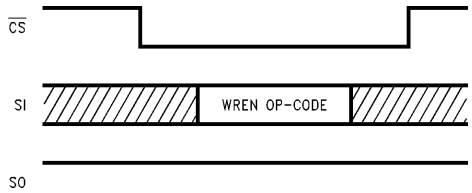

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FIGURE 8. Write Enable

WRITE DISABLE (WRDI): To protect against accidental data disturbance the WRITE DISABLE (WRDI) instruction disables all programming modes. See *Figure 9*.

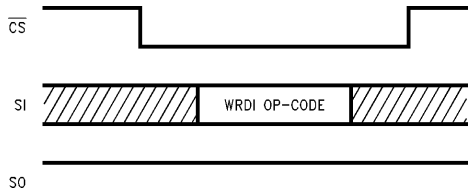

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FIGURE 9. Write Disable

WRITE SEQUENCE: To program the device the WRITE PROTECT ($\overline{WP}$) pin must be held high and two separate instructions must be executed. The chip must first be write enabled via the WRITE ENABLE instruction and then a WRITE instruction must be executed. Moreover, the address of the memory location(s) to be programmed must be outside the protected address field selected by the Block Write Protection Level. See Table III.

A WRITE command requires the following sequence. The $\overline{CS}$ line is pulled low to select the device, then the WRITE op-code (which includes A8) is transmitted on the SI line followed by the byte address (A7–A0) and the corresponding data (D7–D0) to be written. Programming will start after the $\overline{CS}$ pin is forced back to a high level. Note that the LOW to HIGH transition of the $\overline{CS}$ pin must occur during the SCK low time immediately after clocking in the D0 data bit. See *Figure 10*.

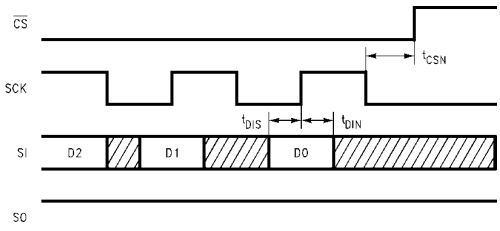

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FIGURE 10. Start WRITE Condition

The READY/BUSY status of the device can be determined by executing a READ STATUS REGISTER (RDSR) instruction, Bit 0 = 1 indicates that the WRITE cycle is still in progress and Bit 0 = 0 indicates that the WRITE cycle has ended. During the WRITE programming cycle (Bit 0 = 1) only the READ STATUS REGISTER instruction is enabled.

The NM25C040 is capable of a 4 byte PAGE WRITE operation. After receipt of each byte of data the two low order address bits are internally incremented by one. The seven high order bits of the address will remain constant. If the master should transmit more than 4 bytes of data, the address counter will ''roll over'', and the previously loaded data will be reloaded.

At the completion of a WRITE cycle the device is automatically returned to the write disable state.

If the $\overline{WP}$ pin is forced low or the device is not WRITE enabled, the device will ignore the WRITE instruction and return to the standby state when $\overline{CS}$ is forced high. A new $\overline{CS}$ falling edge is required to re-initialize the serial communication. See *Figure 11*.

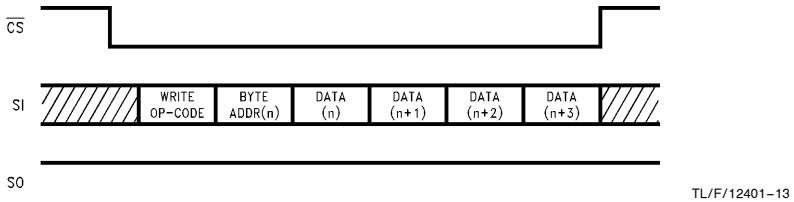

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FIGURE 11. Start Write Condition

Functional Description (Continued)

WRITE STATUS REGISTER (WRSR): The WRITE STATUS REGISTER (WRSR) instruction is used to program the non-volatile status register Bits 2 and 3 (BP0 and B1). The WRITE PROTECT ($\overline{WP}$) pin must be held high and two separate instructions must be executed. The chip must first be write enabled via the WRITE ENABLE instruction and then WRSR instruction must be executed.

The WRSR command requires the following sequence. The $\overline{CS}$ line is pulled low to select the device and then the WRSR op-code is transmitted on the SI line followed by the data to be programmed. See *Figure 12*.

Note that the first four bits are don't care bits followed by BP1 and BP0 then two additional don't care bits. Programming will start after the $\overline{CS}$ pin is forced back to a high level. As in the WRITE instruction the LOW to HIGH transition of the $\overline{CS}$ pin must occur during the SCK low time immediately after clocking in the last don't care bit. See *Figure 13*.

The READY/BUSY status of the device can be determined by executing a READ STATUS REGISTER (RDSR) instruction. Bit 0 = 1 indicates that the WRSR cycle is still in progress and Bit 0 = 0 indicates that the WRSR cycle has ended.

At the completion of a WRSR cycle the device is automatically returned to the write disable state.

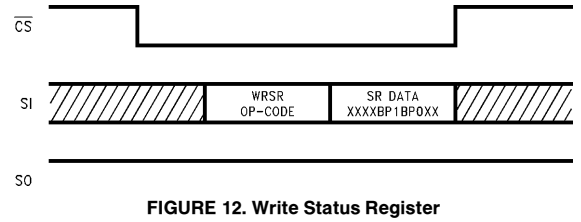

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FIGURE 12. Write Status Register

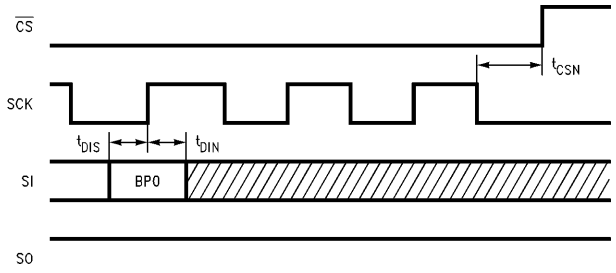

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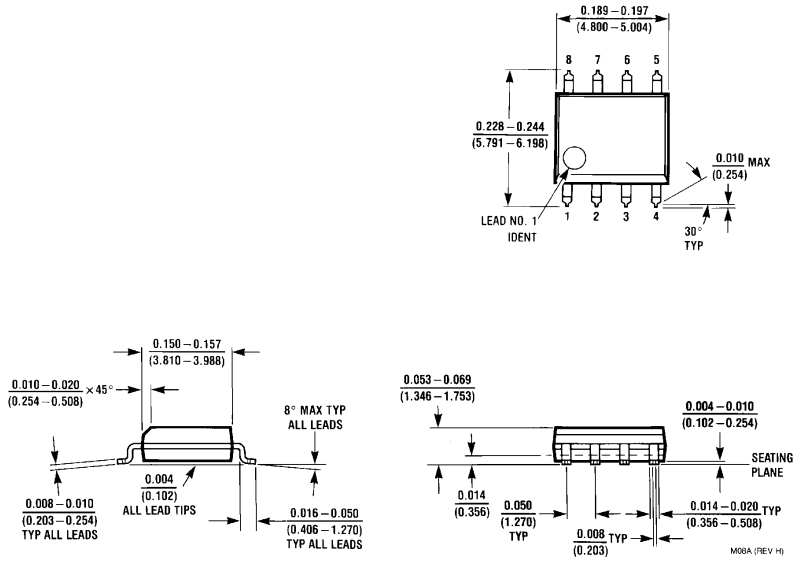
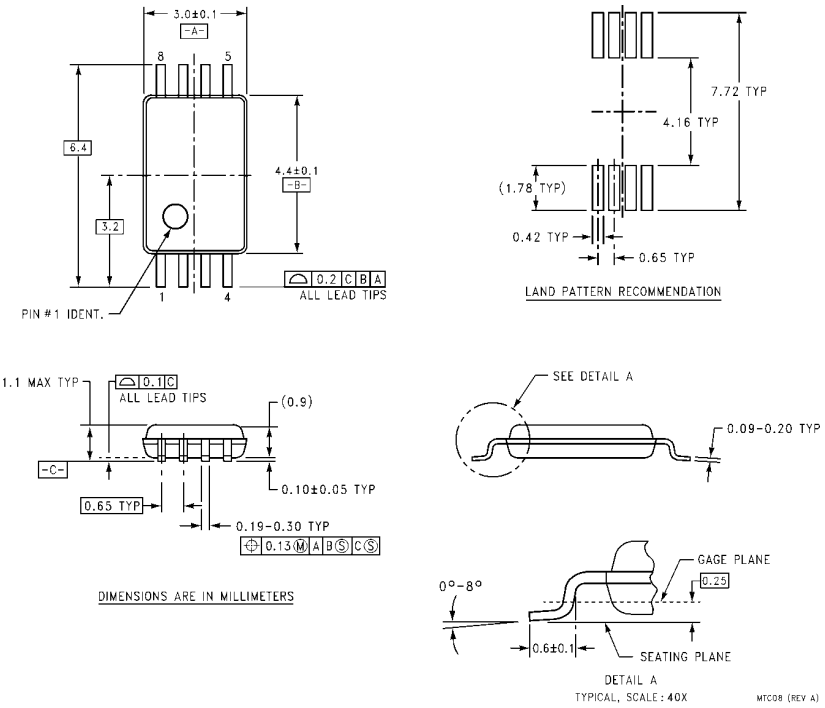
FIGURE 13. Start WRSR Condition

Physical Dimensions inches (millimeters) unless otherwise noted

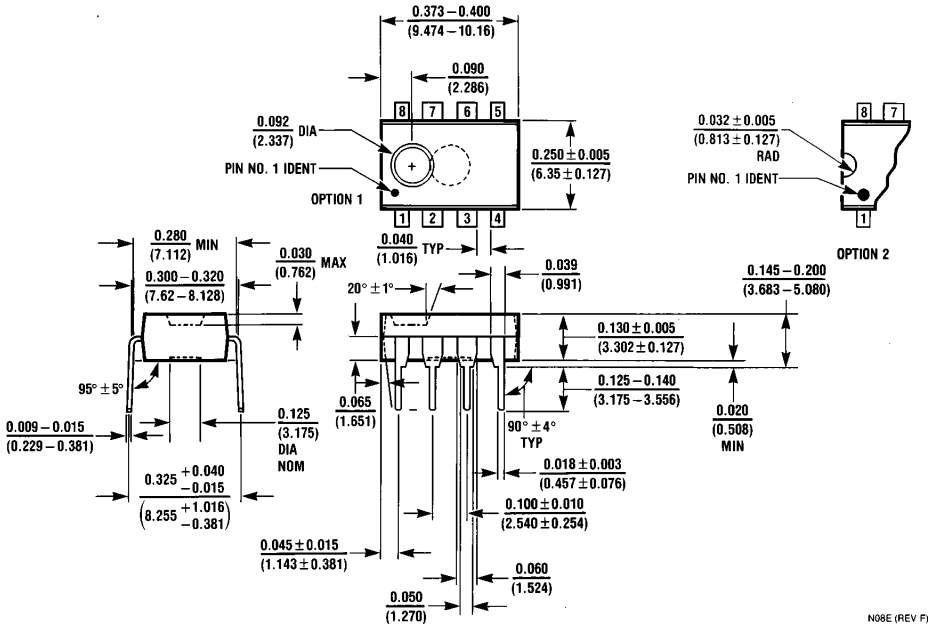


Molded Small Out-Line Package (M8)
NS Package Number M08A



8-Pin Molded TSSOP, JEDEC (MT8)
NS Package Number MTC08

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Molded Dual-In-Line Package (N)
NS Package Number N08E

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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